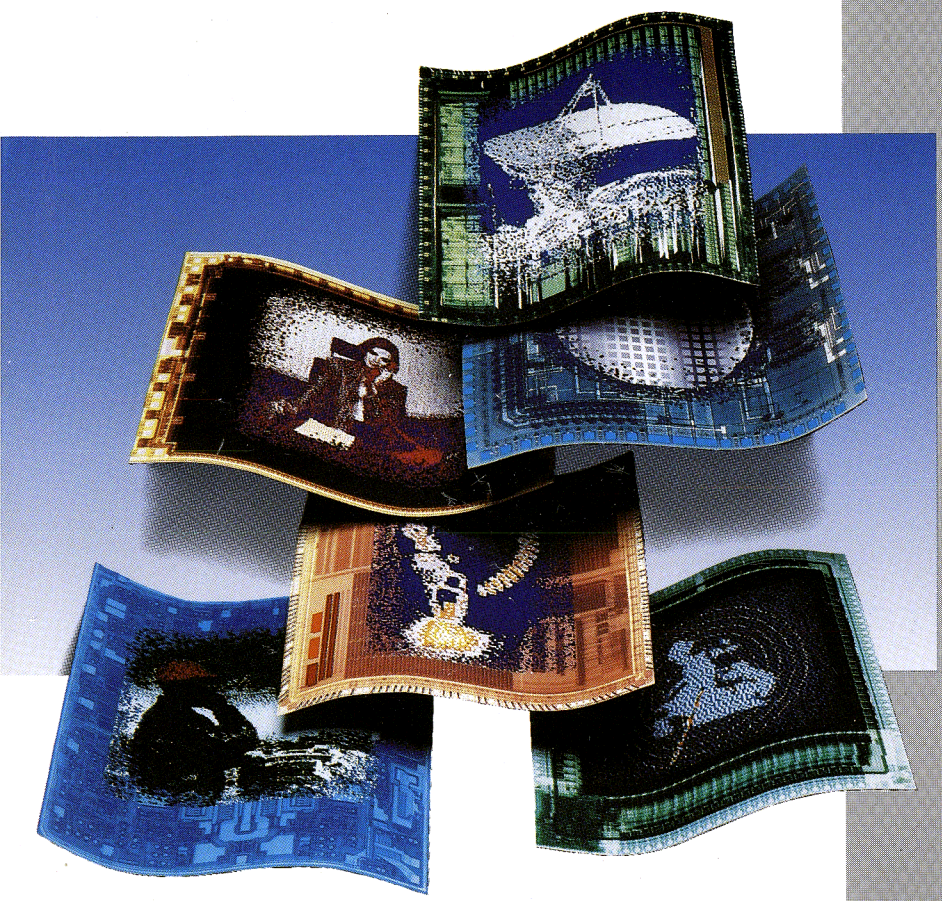
Consumer

IC Handbook

April 1994



GEC PLESSEY
SEMICONDUCTORS

CONSUMER

IC Handbook

GEC PLESSEY

SEMICONDUCTORS

Foreword

The two main areas in Consumer in which GEC Plessey Semiconductors specialise are the RF Front End of TV/Cable/VCR/Satellite Receivers and Teletext.

In the RF Front End of TV/Cable/VCR/Satellite Receivers, GEC Plessey Semiconductors has traditional strengths in high speed bipolar technology and it is on these strengths that our current and future product offerings will be based.

We offer a wide selection of single chip PLL ICs - both I^2C and 3-wire - with FM Demodulators and Modulators to complement the system requirements. With Digital transmission soon to make an impact, work on ICs required for this new application is well underway with very low phase noise PLLs, Digital Demodulators, RF Converters, etc. well into the design phase.

For Teletext applications, GEC Plessey Semiconductors provide innovative solutions which enable Intelligent Page Capture or IPC. IPC stores all pages likely to have a related subject to the chosen page - the result is an information system which helps reduce a customer's frustration when using the teletext service.

GEC Plessey Semiconductors' EVA Family helps the VCR manufacturer to differentiate their product by:

- Always receiving the correct and complete programme.
- Automatic VCR tuning.
- Automatic Clock and Calendar setting.

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TV/Cable/Satellite Tuner PLL Circuits[1]

Type No.	Function	Frequency	Page
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SP5511[2]	Bi-directional I²C bus controlled synthesiser	1.3GHz	112
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SP5524[2]	Bi-directional I²C bus controlled synthesiser	1.3GHz	134
SP5610[2]	Bi-directional I²C bus controlled synthesiser	1.3GHz	142
SP5611[2]	Bi-directional I²C bus controlled synthesiser	1.3GHz	150
SP5655[2]	Bi-directional I²C bus controlled synthesiser	2.7GHz	158

NOTES
1. All are bipolar ICs and operate from a single +5V supply.
2. Purchase of GEC Plessey Semiconductors' I²C components conveys a licence under the Philips I²C Patent Rights to use these components in I²C systems, provided that the systems conform to the I²C Standard Specification as defined by Philips.

Video Modulation

Type No.	Function	Frequency	Process	Page
SL5067	Multi-standard video modulator	900MHz	Bipolar	169

Product index (continued)

Teletext and TV Signal Generators

Type No.	Function	Supply	Process	Page
MV1815	625-line single chip teletext decoder, 14 languages [3]	5V	CMOS	207
MV1817	625-line single chip teletext decoder	5V	CMOS	224
MV1820	Video programme delivery control interface circuit	5V	CMOS	247
MV1821	Video cassette recorder PDS and VPS interface circuit	5V	CMOS	252

NOTES

3. English, German, Swedish/Finnish, Italian, French (Belgian), Spanish, Czech, Polish, Romanian, Hungarian, Turkish, Serbo-Croat, Danish, American.

Remote Control

Type No.	Function	Supply voltage (V) (typ)	Supply current (mA) (typ)	Process	Page
SL486	Infra-red preamplifier	4.5-9.5	6.5	Bipolar	261
SL490B	32-code PPM transmitter, infra-red, ultrasonic or radio	4.5-9.5	9.5	Bipolar	266

Power Control

Type No.	Function	Supply voltage (V) (typ)	Supply current (mA) (typ)	Process	Page
SL441C	Zero voltage switch	15	7.5	Bipolar	299
TDA2088	Phase control IC for current feedback applications	-15	2.8	Bipolar	302

PWM Waveform Generator Circuits

The GEC Plessey Semiconductors range of PWM generator chips are designed to meet all PWM waveform synthesis needs to AC Motor Control and Uninterruptible Power Supply (UPS) applications. The devices generate fully-digital asynchronous PWM, implementing any power waveform read either from an external ROM/EPROM or from an on-chip ROM.

Full programmability via a simple micro interface (the MOTEL™ interface) allows use with any chosen power electronics. Once programmed, the devices run without intervention until parameters, for example, motor speed, need to be changed.

Useful features such as forward/reverse control, zero power frequency setting for DC injection braking, selectable minimum pulse width and underlap are also provided.

Type No.	No. of phases	Power waveform storage	Standard waveform options	Power frequency range	Carrier frequency range	Package options	Page
MA818	3	External ROM/ EPROM	Any waveform, user-programmable in external ROM/EPROM	0 to 4kHz 12-bit accuracy	0 to 24kHz	DIL and Quad J-Lead	271
MA828-1	3	On-chip ROM	$x(t) = A[\sin(\omega t) + {}^{1}/_{6}\sin(3\omega t)]$	0 to 4kHz 12-bit accuracy	0 to 24kHz	DIL and Small Outline	283
MA828-2			$x(t) = A\sin(\omega t)$				
MA828-X			Any waveform to order				
MA838-1	1	On-chip ROM	$x(t) = A[\sin(\omega t) + {}^{1}/_{6}\sin(3\omega t)]$	0 to 4kHz 12-bit accuracy	0 to 24kHz	DIL and Small Outline	295
MA838-2			$x(t) = A\sin(\omega t)$				
MA838-X			Any waveform to order				

MOTEL is a registered trademark of Motorola Corp. and Intel Corp.

Product List - Alpha numeric

Section 1
High Speed Dividers

GEC PLESSEY
SEMICONDUCTORS

SP4633

1GHz÷64 NON SELF OSCILLATING PRESCALER

The SP4633 ÷64 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a low supply current, giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4633 incorporates a two-stage preamplifier which gives good low frequency sensitivity and prevents self-oscillation.

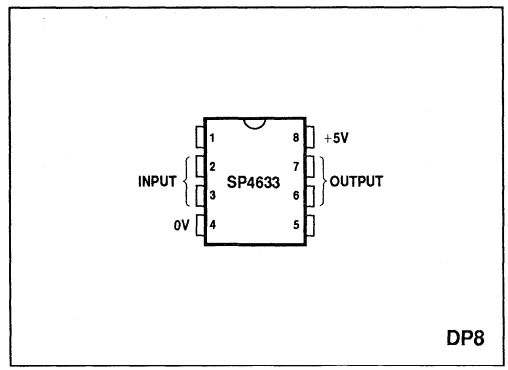


Fig 1. Pin connections - top view

FEATURES

- Does Not Self Oscillate
- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection †

† ESD precautions must be observed

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Operating temperature range	0°C to+80°C

ORDERING INFORMATION

SP4633 NA DP

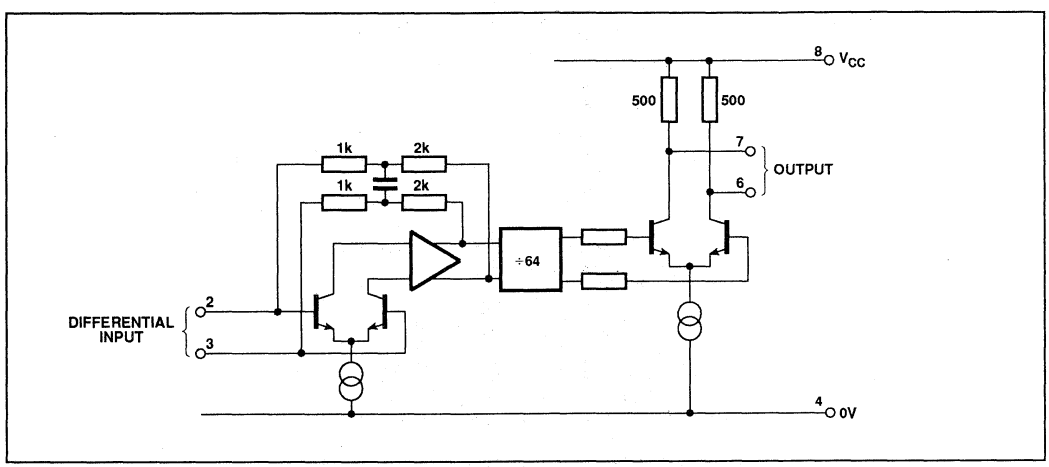


Fig. 2 SP4633 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = 0°C to +70°C, V_{CC} = 4·5V to 5·5V (Test circuit see Fig. 3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	8		32	45	mA	V_{CC} = +5V
Input sensitivity	2,3					RMS sinewave (50Ω system)
50MHz to 400MHz			1·5	5	mV	
600MHz			2	7·5	mV	
800MHz			3	10	mV	
1000MHz			5	15	mV	
Input overload	2,3	300			mV	50MHz to 1GHz operating frequency
Input impedance	2,3		50		Ω	See Fig. 6
			2		pF	
Output voltage, no load	6	0·8			V p-p	f_{IN} = 1GHz, V_{CC} = +5V
	7	0·8			V p-p	
Output voltage with load as Fig. 3	6	0·55			V	
	7	0·55			V	
Output impedance	6		0·5		kΩ	
	7		0·5		kΩ	
Output imbalance	6,7		0·1		V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltage is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

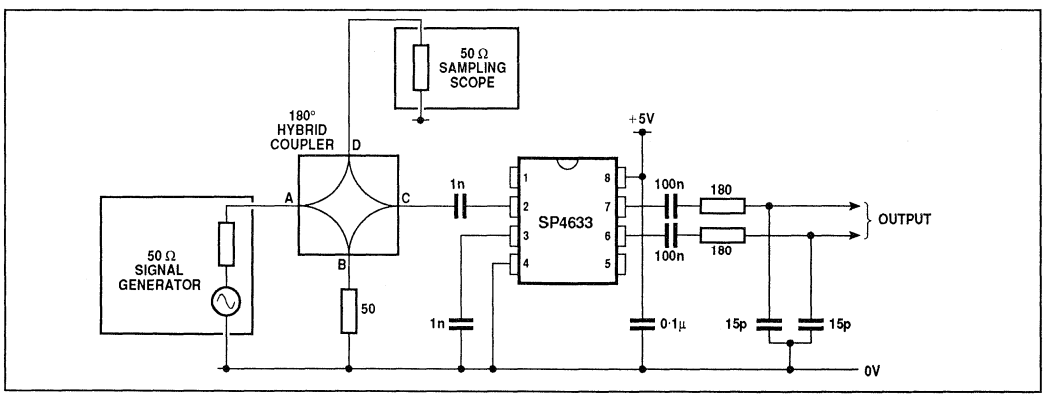


Fig. 3 Test circuit

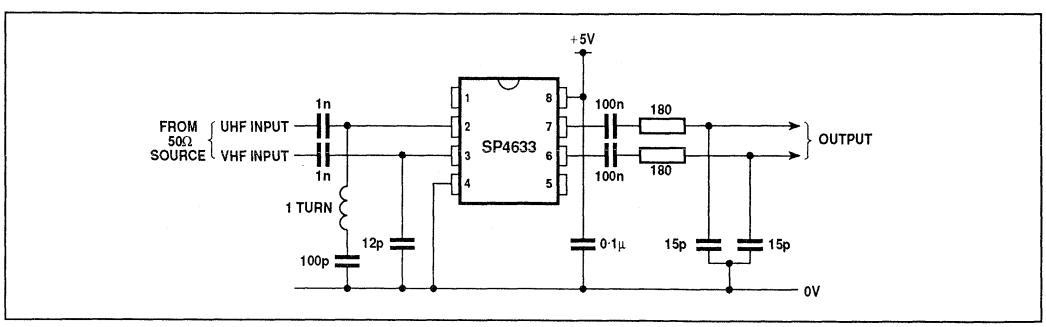


Fig. 4 Application circuit

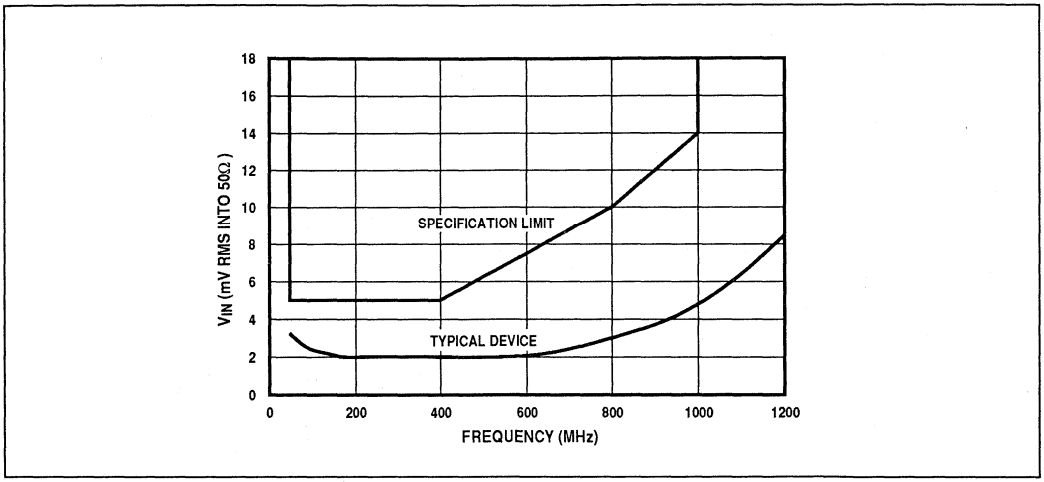


Fig. 5 Typical input sensitivity

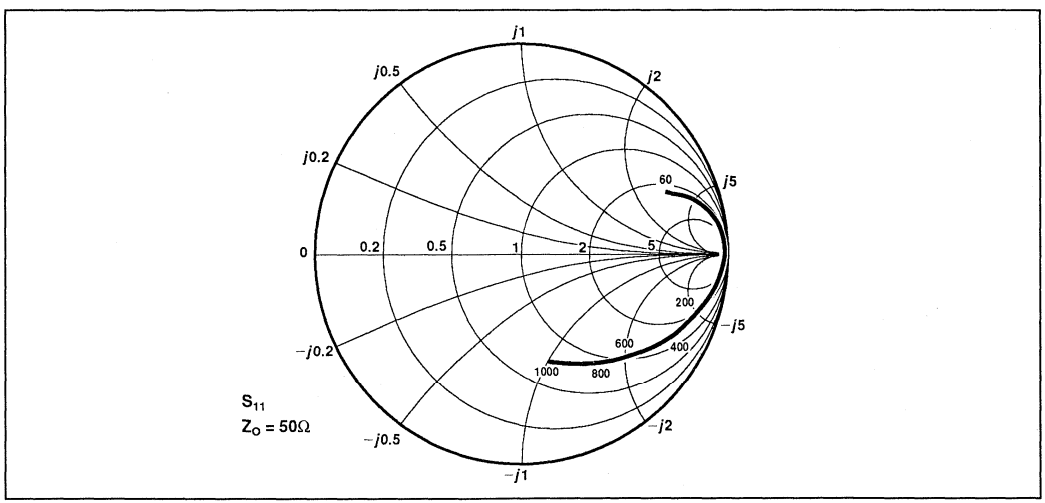


Fig. 6 Typical input impedance (frequencies in MHz)

SP4660

1GHz÷256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4660 ÷256 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a low supply current, giving reduced dissipation and operating temperatures in an 8-pin plastic DIL package. Spurious radiation has been reduced from all stages.

The SP4660 incorporates an on-chip preamplifier with differential inputs and has balanced ECL outputs.

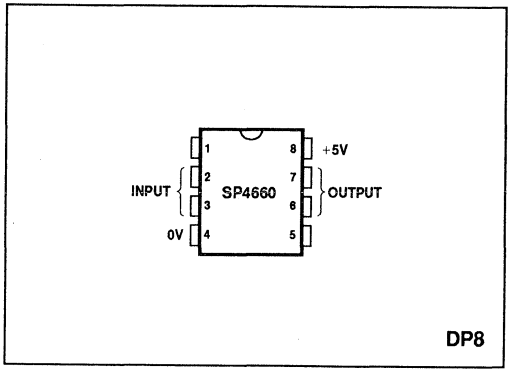


Fig 1. Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity from 50MHz to 1GHz
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection †

† ESD precautions must be observed

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Operating temperature range	0°C to+80°C

ORDERING INFORMATION

SP4660 NA DP

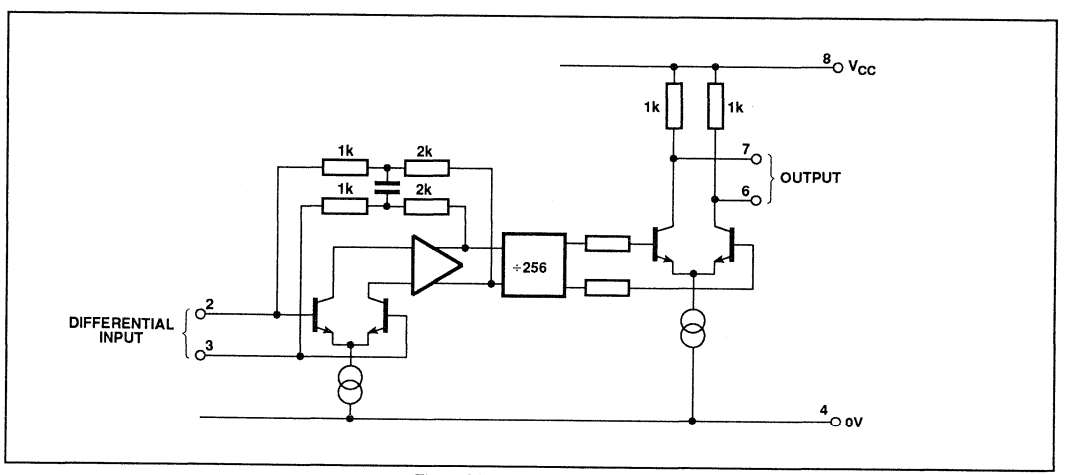


Fig. 2 SP4660 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = 0°C to +70°C, V_{CC} = 4·5V to 5·5V (Test circuit see Fig. 3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	8		32	45	mA	V_{CC} = +5V
Input sensitivity	2,3					RMS sinewave (50Ω system)
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
Input overload	2,3	300			mV	50MHz to 1GHz operating frequency
Input impedance	2,3		50		Ω	See Fig. 6
			2		pF	
Output voltage, no load	6	0·8			V p-p	
	7	0·8			V p-p	
Output voltage with load as Fig. 3	6	0·6			V	f_{IN} = 1GHz, V_{CC} = +5V
	7	0·6			V	
Output impedance	6		1		kΩ	
	7		1		kΩ	
Output imbalance	6,7			0·1	V	

NOTE
The difference between the maximum input sensitivity and minimum overload voltage is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

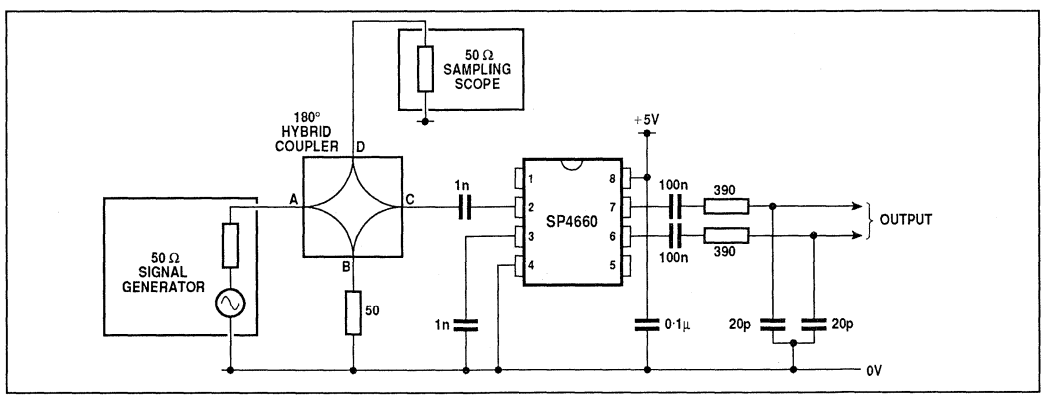


Fig. 3 Test circuit

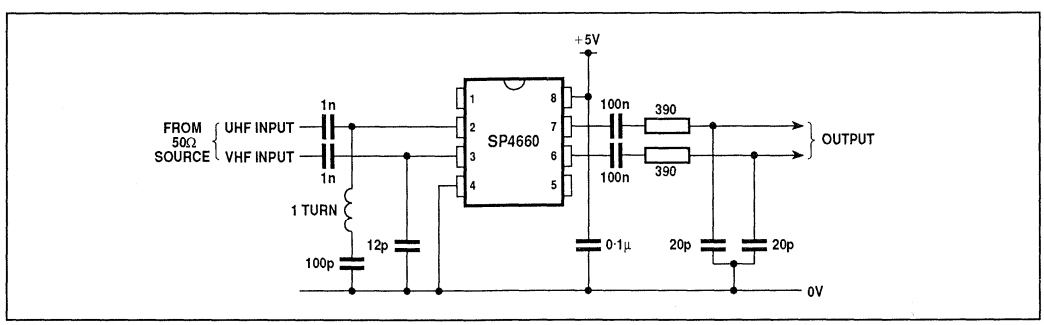


Fig. 4 Application circuit

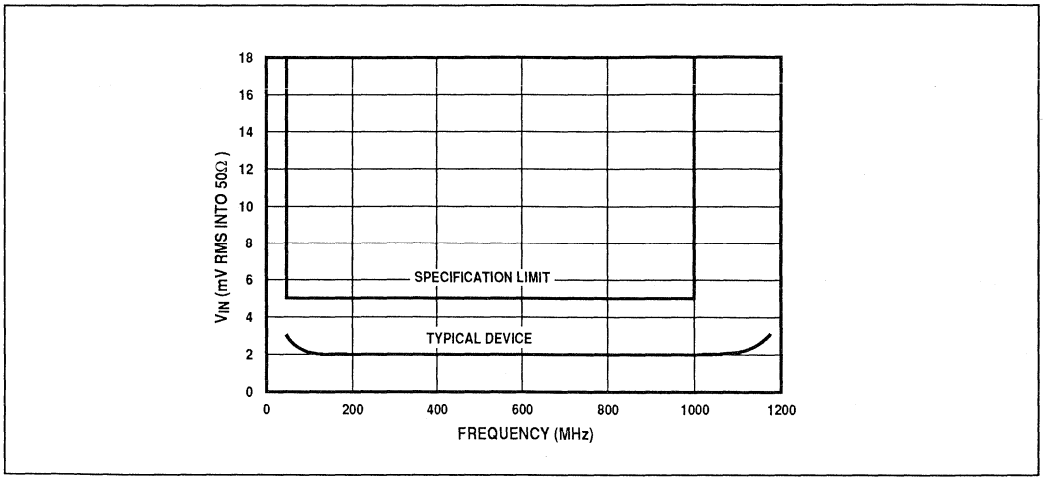


Fig. 5 Typical input sensitivity

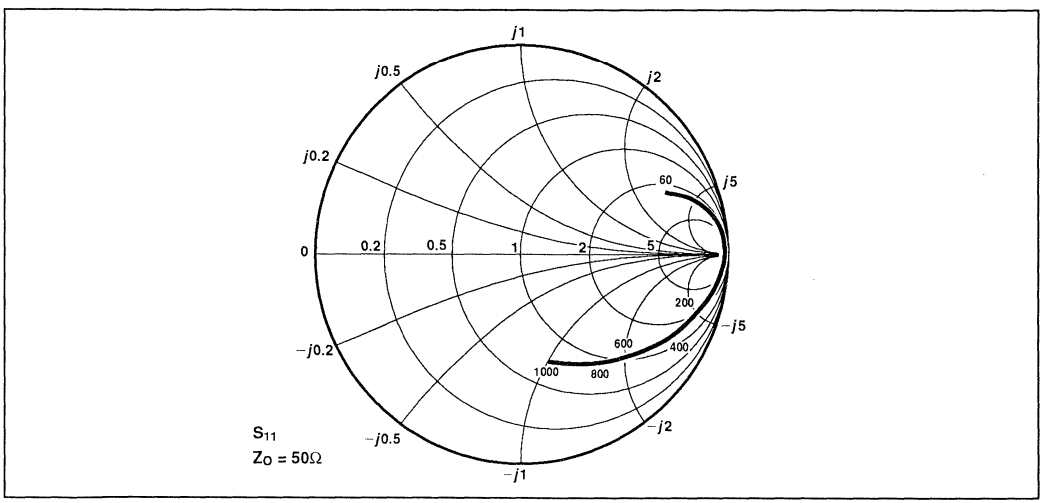


Fig. 6 Typical input impedance (frequencies in MHz)

SP4666

1·3GHz÷64/256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4666 is a selectable division ratio high speed divider capable of replacing separate fixed ratio ECL prescalers with a single part in applications with alternative ÷64 and ÷256 division requirements.

A switched low pass filter with −3dB points at 5·3MHz and 15·6MHz is connected before the output stage to reduce the harmonic content to a very low level.

FEATURES

- Switched Low Pass Filter for Very Low Output Radiation
- Low Supply Current
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- Balanced ECL Outputs
- Electrostatic Protection †

† ESD precautions must be observed

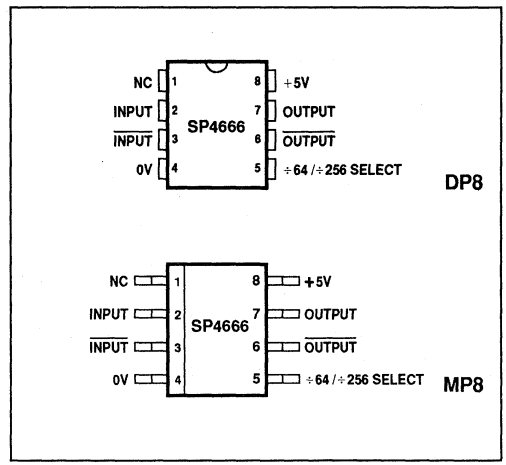


Fig 1. Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Operating temperature range	0°C to+80°C

ORDERING INFORMATION

SP4666 NA DP
SP4666 NA MP

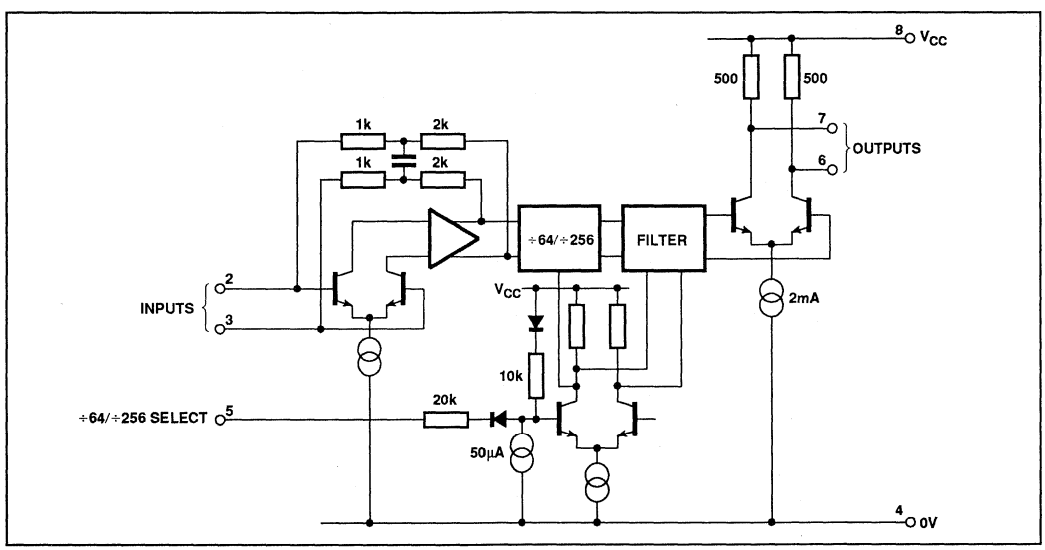


Fig. 2 SP4666 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = 0°C to +80°C, V_{CC} = 4·5V to 5·5V (Test circuit see Fig. 3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	8		23	30	mA	V_{CC} = +5V
Input sensitivity	2,3					RMS sinewave (50Ω system)
50MHz			2·5	10	mV	
200MHz to 1050MHz			0·5	5	mV	
1050MHz to 1300MHz				10	mV	
Input overload	2,3	500			mV	
Input impedance	2,3		50		Ω	See Fig. 6
			2		pF	
Output voltage with 12pF load	6,7	0·8	1		V p-p	÷64 mode, f_{IN} = 100MHz
		0·8	1		V p-p	÷256 mode, f_{IN} = 100MHz
		0·4	0·5		V p-p	÷64 mode, f_{IN} = 1000MHz
		0·7	0·9		V p-p	÷256 mode, f_{IN} = 1000MHz
		0·25	0·35		V p-p	÷64 mode, f_{IN} = 1300MHz
		0·6	0·7		V p-p	÷256 mode, f_{IN} = 1300MHz
Output impedance	6,7		500		Ω	
Output imbalance	6,7		0·1		V	
Voltage for ÷256 operation	5			0·5	V	
Voltage for ÷64 operation	5	3·5			V	See note 1
Sink current for ÷256 operation	5			250	µA	Vpin5 = 0V

NOTES

1. Pin 5 has an internal pull-up and may be left open-circuit for ÷64 operation.
2. The difference between the maximum input sensitivity and minimum overload voltage is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

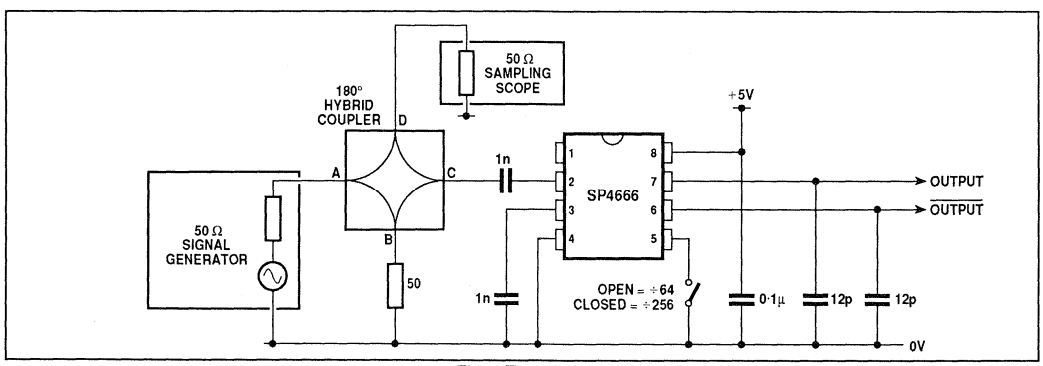


Fig. 3 Test circuit

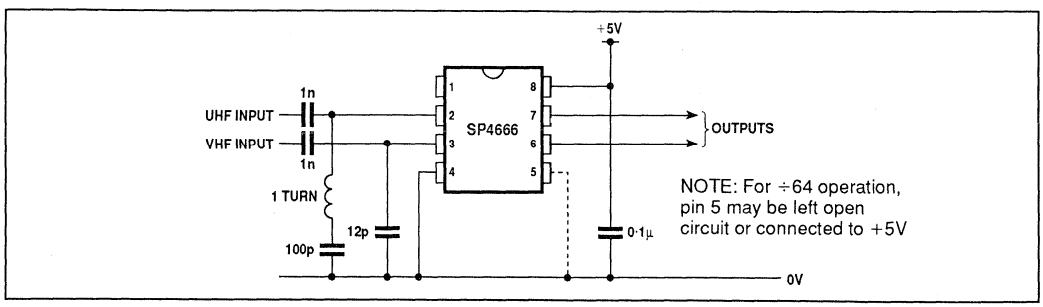


Fig. 4 Application circuit

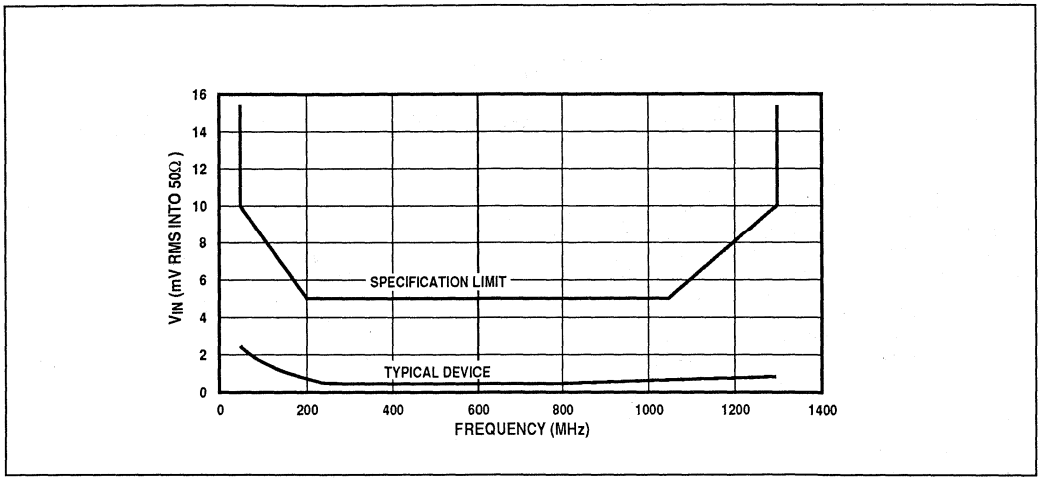


Fig. 5 Typical input sensitivity

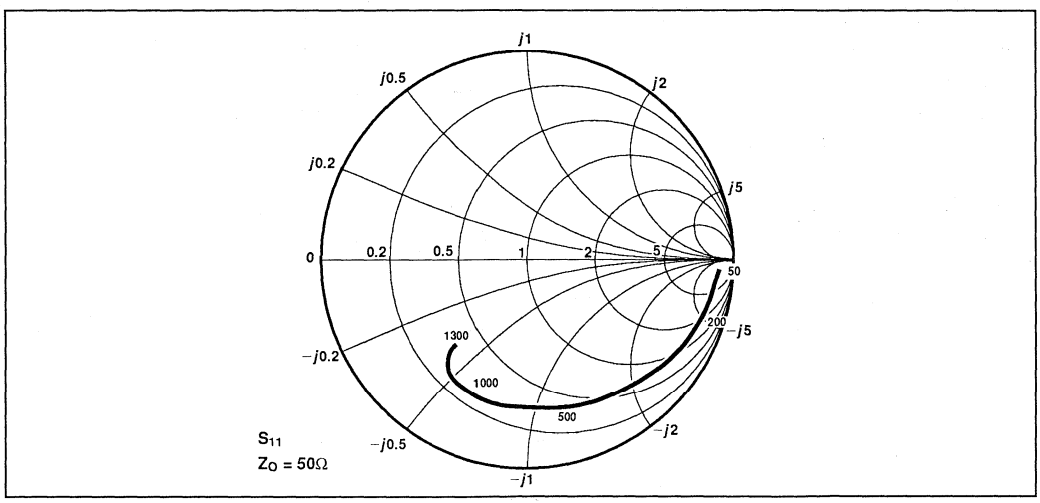


Fig. 6 Typical input impedance (frequencies in MHz)

SP4740

1·3GHz ÷256 PRESCALER WITH LOW CURRENT AND LOW RADIATION

The SP4740 ÷256 prescaler is one of GPS' range of high speed dividers for consumer frequency synthesis and measurement systems. It has a low supply current, giving reduced dissipation and operating temperatures in an 8-pin plastic DIL (DP8) or miniature plastic DIL (MP8) package. Spurious radiation has been reduced from all stages.

The SP4740 incorporates an on-chip preamplifier with differential inputs and has a TTL/CMOS compatible output.

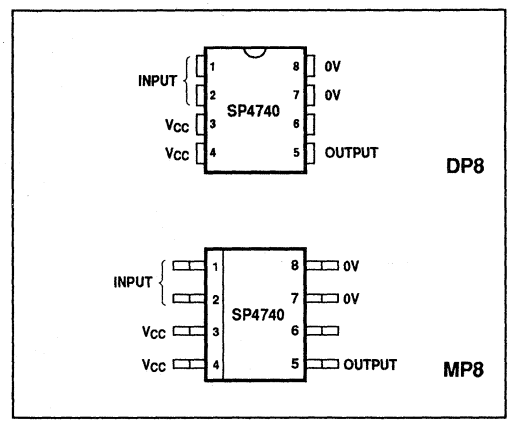


Fig 1. Pin connections - top view

FEATURES

- Low Supply Current
- Low Radiation
- Input Wideband Amplifier
- High Input Sensitivity
- High Input Impedance
- TTL/CMOS Output
- Electrostatic Protection †

† ESD precautions must be observed

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Operating temperature range	0°C to+80°C

ORDERING IFORMATION

SP4740 NA DP
SP4740 NA MP

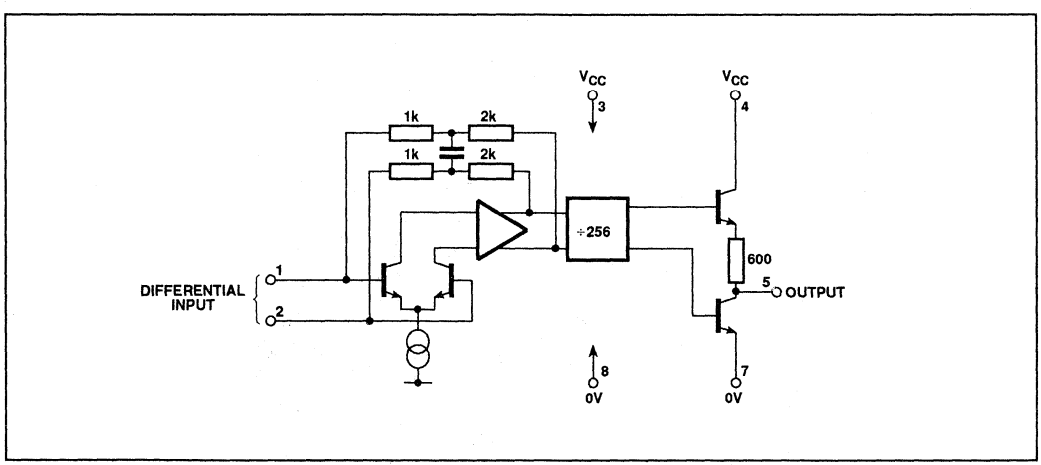


Fig. 2 SP4740 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = 0°C to +70°C, V_{CC} = 4·5V to 5·5V (Test circuit see Fig. 3)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	8		35	50	mA	V_{CC} = +5V
Input sensitivity	2,3					RMS sinewave
50MHz			3	5	mV	
150MHz to 1000MHz			1	5	mV	
1·1GHz			1·5		mV	
1·2GHz			2		mV	
1·3GHz			4		mV	
Input overload	2,3	300			mV	50MHz to 500MHz
		400			mV	500MHz to 1·3GHz
Input impedance	2,3		50		Ω	See Fig. 6
			2		pF	
Output voltage						
High	5	3·3			V	Sourcing 0·2mA
Low	5			0·1	V	Sinking 2mA

NOTE
The difference between the maximum input sensitivity and minimum overload voltage is the guaranteed dynamic range. Input signal levels should be maintained within these limits at all frequencies.

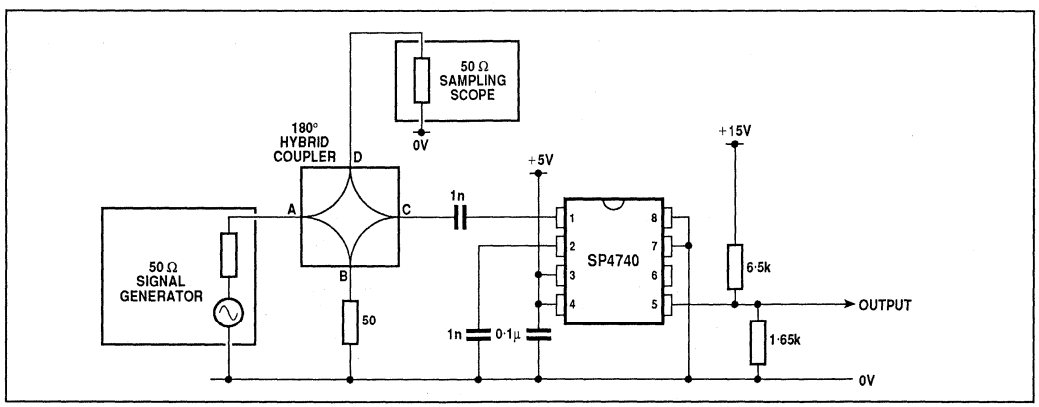


Fig. 3 Test circuit

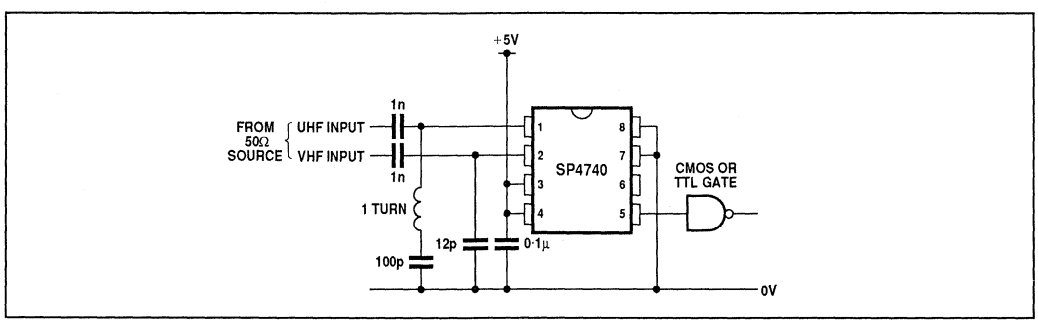


Fig. 4 Application circuit

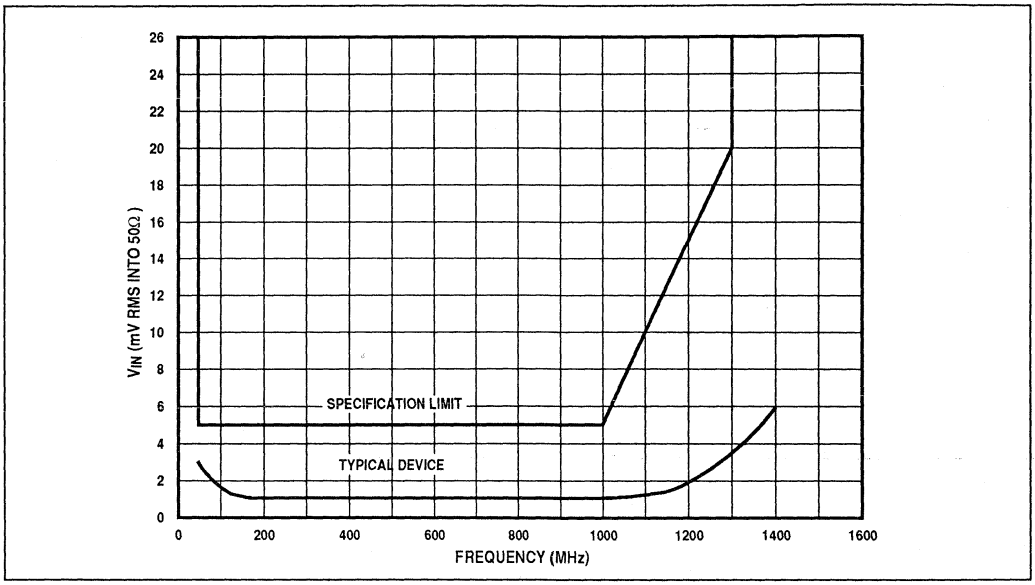


Fig. 5 Typical input sensitivity

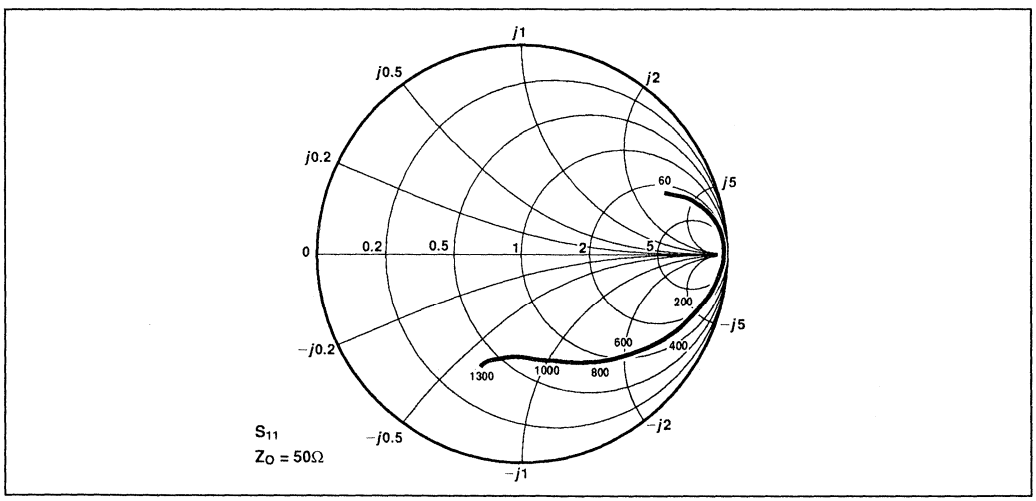


Fig. 6 Typical input impedance (frequencies in MHz)

SP4902

2·5GHz ÷2 PRESCALER

The SP4902 prescaler is one a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2·5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 300mW
- Single 5V Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Electrostatic Protection †

† ESD precautions must be observed

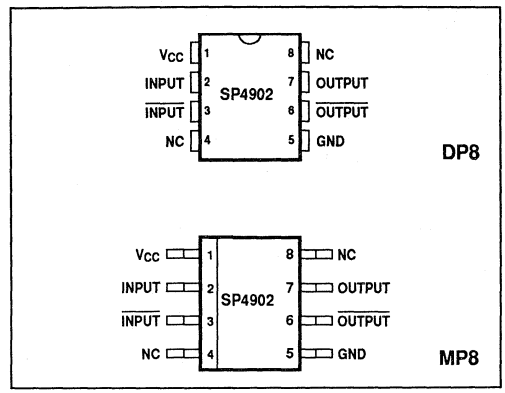


Fig 1. Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+6·5V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP4902 NA DP
SP4902 NA MP

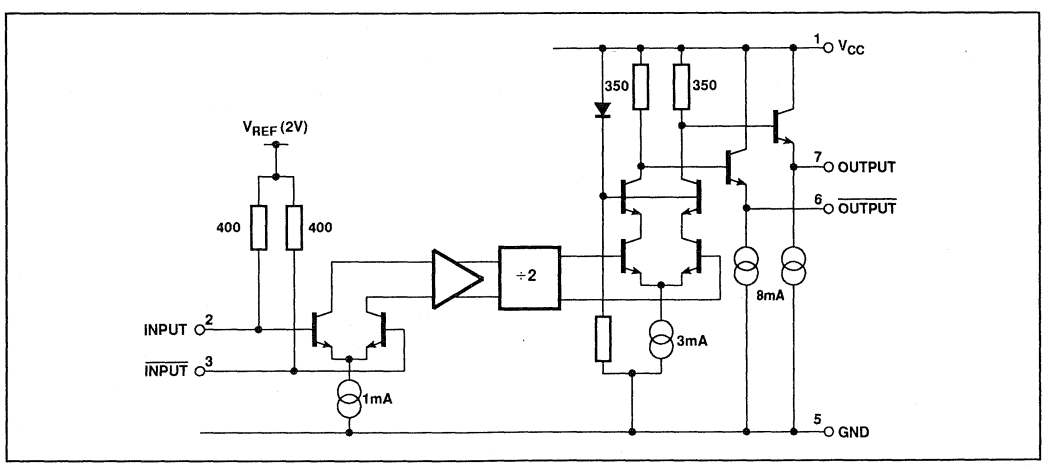


Fig. 2 SP4902 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = −10°C to +85°C, V_{CC} = +4·75V to +5·25V (Test circuit see Fig. 4)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	1		60	75	mA	V_{CC} = +5V
Input sensitivity	2,3					
500MHz to 1800MHz				50	mV	RMS sinewave, measured in 50Ω system,
2500MHz				100	mV	see Figs 3 and 4.
Input impedance (series equivalent)	2,3		50		Ω	See Fig. 5
			2		pF	
Output voltage with fIN = 500MHz	6,7	0·45	0·55		V p-p	V_{CC} = +5V, load as Fig. 4
Output voltage with fIN = 2500MHz	6,7	0·15	0·2		V p-p	V_{CC} = +5V, load as Fig. 4

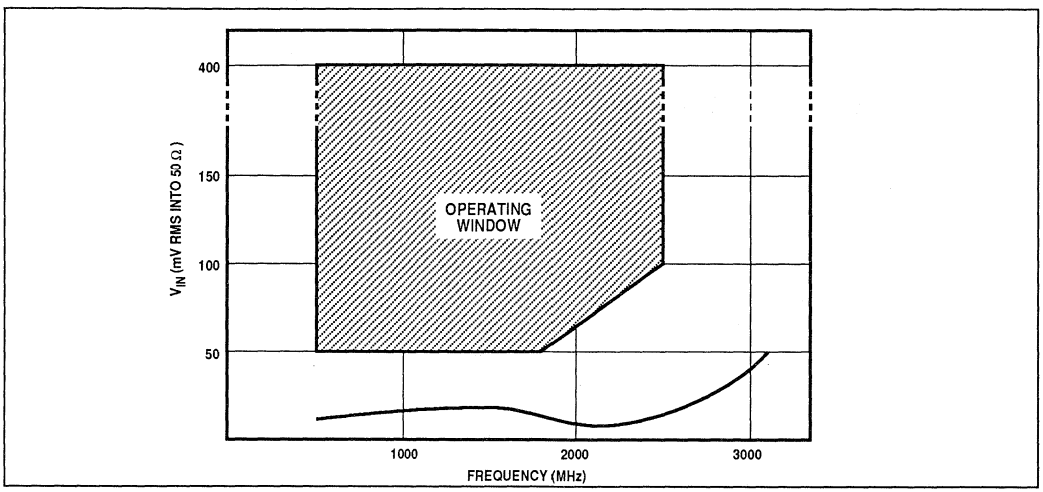


Fig. 3 Typical input sensitivity

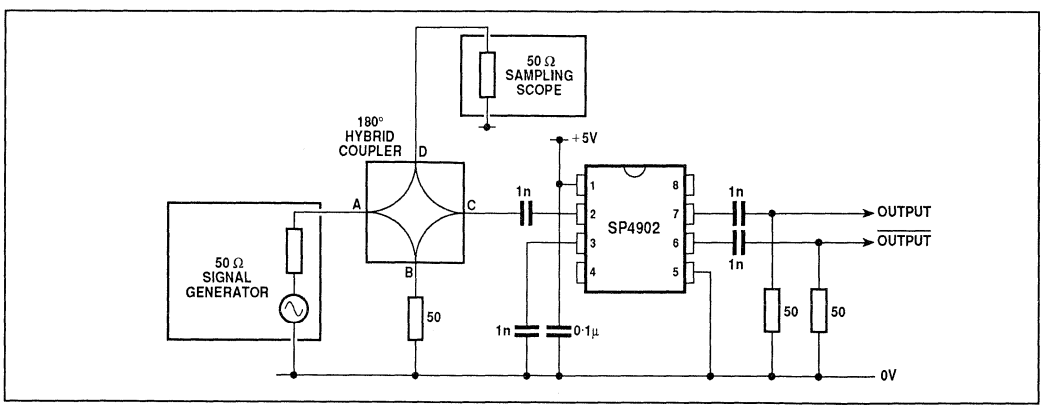


Fig. 4 Test circuit

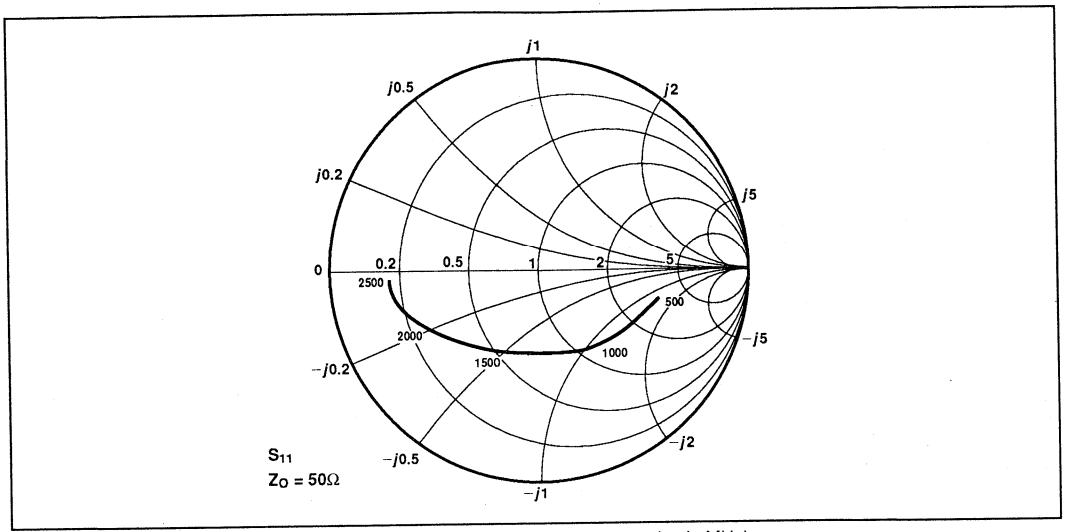


Fig. 5 Typical input impedance (frequencies in MHz)

SP4904

2·5GHz ÷4 PRESCALER

The SP4904 prescaler is one a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2·5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 300mW
- Single 5V Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Electrostatic Protection †

† ESD precautions must be observed

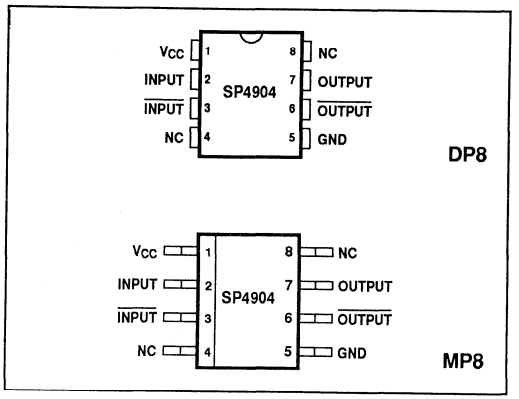


Fig 1. Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+6·5V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP4904 NA DP
SP4904 NA MP

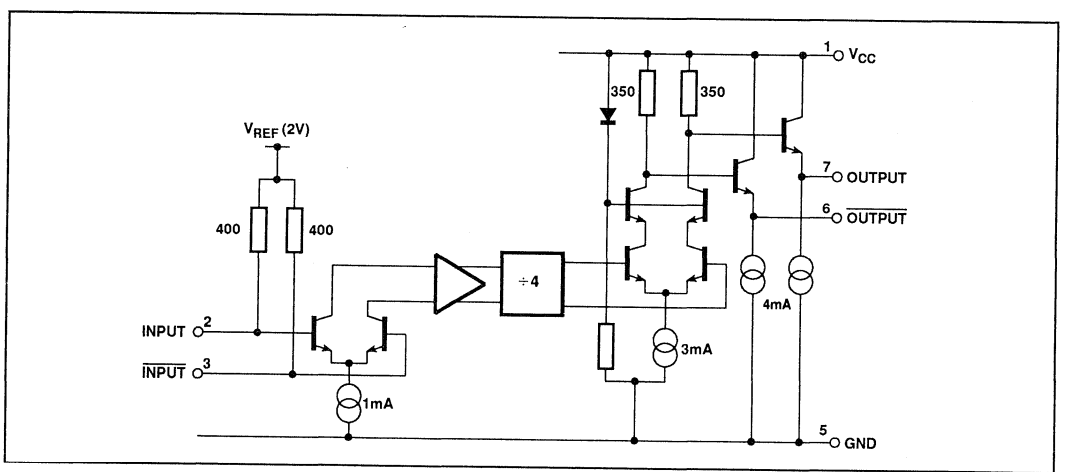


Fig. 2 SP4904 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = −10°C to +85°C, V_{CC} = +4·75V to +5·25V (Test circuit see Fig. 4)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	1		60	75	mA	V_{CC} = +5V
Input sensitivity	2,3					
500MHz to 1800MHz				50	mV	RMS sinewave, measured in 50Ω system,
2500MHz				100	mV	see Figs 3 and 4.
Input impedance (series equivalent)	2,3		50		Ω	See Fig. 5
			2		pF	
Output voltage with fIN = 500MHz	6,7	0·45	0·55		V p-p	V_{CC} = +5V, load as Fig. 4

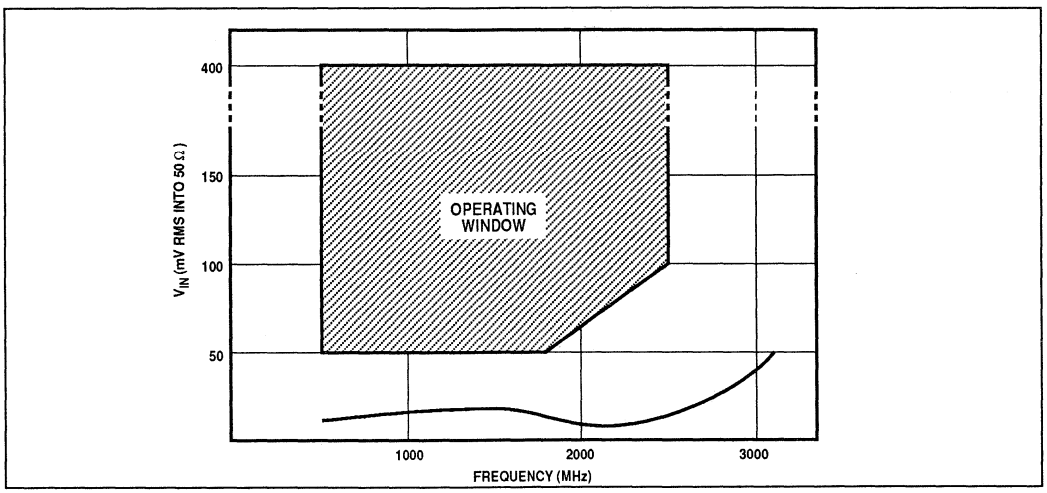


Fig. 3 Typical input sensitivity

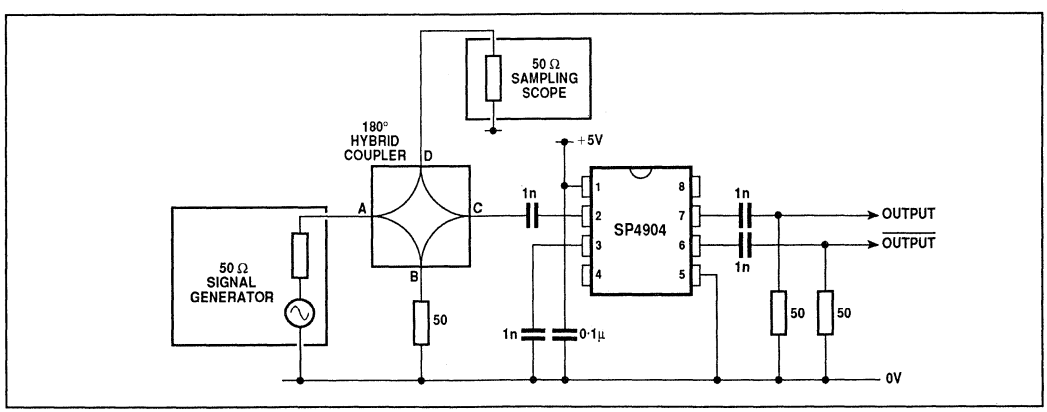


Fig. 4 Test circuit

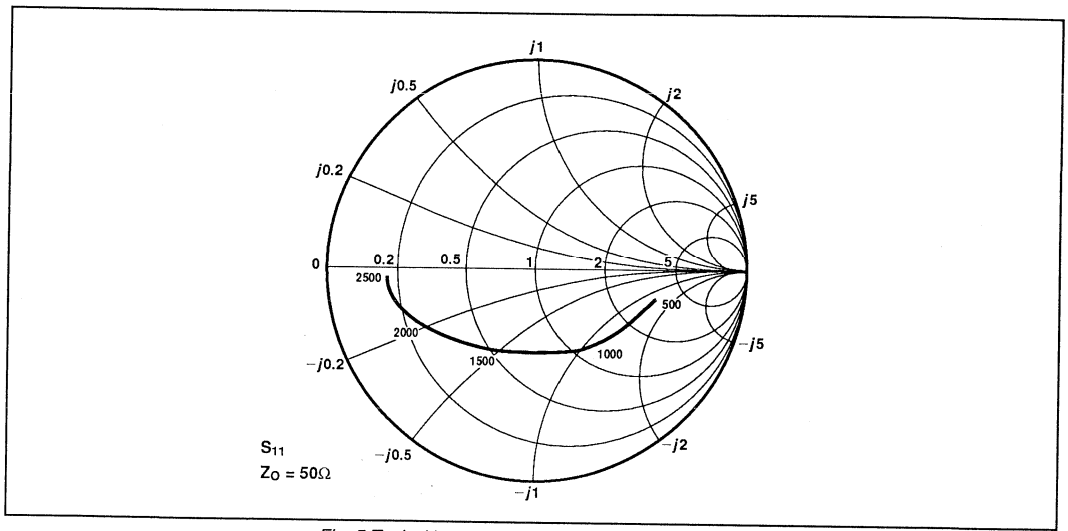


Fig. 5 Typical input impedance (frequencies in MHz)

SP4908

2·5GHz ÷8 PRESCALER

The SP4908 prescaler is one a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage with on-chip current sources for the emitter follower outputs.

FEATURES

- High Speed Operation 2·5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 300mW
- Single 5V Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Electrostatic Protection †

† ESD precautions must be observed

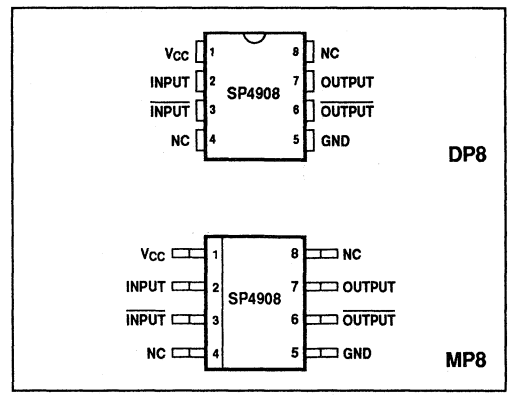


Fig 1. Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+6·5V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP4908 NA DP
SP4908 NA MP

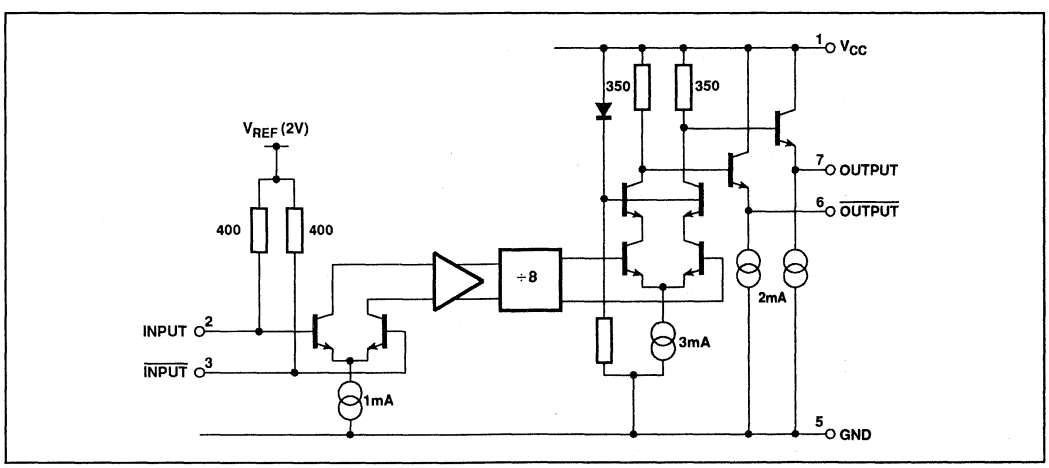


Fig. 2 SP4908 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = −10°C to +85°C, V_{CC} = +4·75V to +5·25V (Test circuit see Fig. 4)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	1		60	75	mA	V_{CC} = +5V
Input sensitivity	2,3					
500MHz to 1800MHz				50	mV	RMS sinewave, measured in 50Ω system,
2500MHz				100	mV	see Figs 3 and 4.
Input impedance (series equivalent)	2,3		50		Ω	See Fig. 5
			2		pF	
Output voltage with fIN = 500MHz	6,7	0·45	0·55		V p-p	V_{CC} = +5V, load as Fig. 4

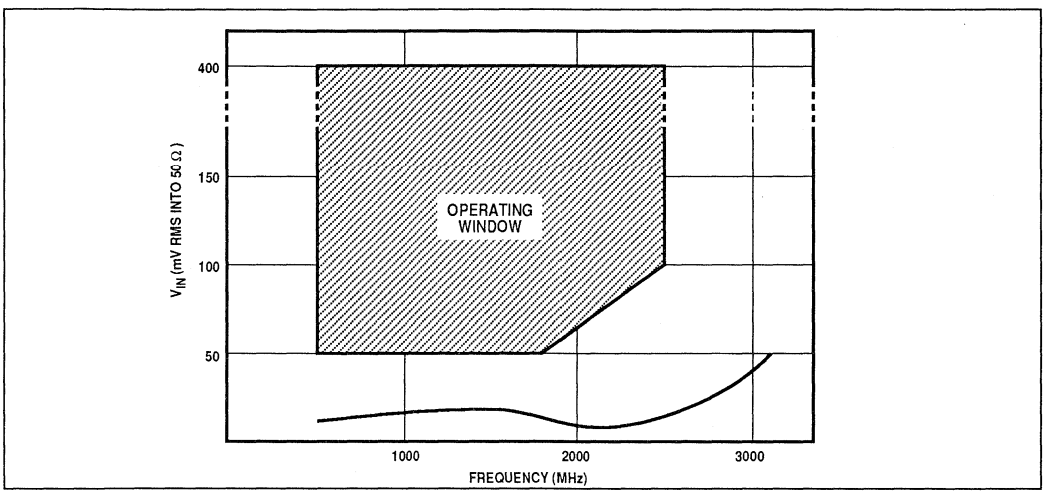


Fig. 3 Typical input sensitivity

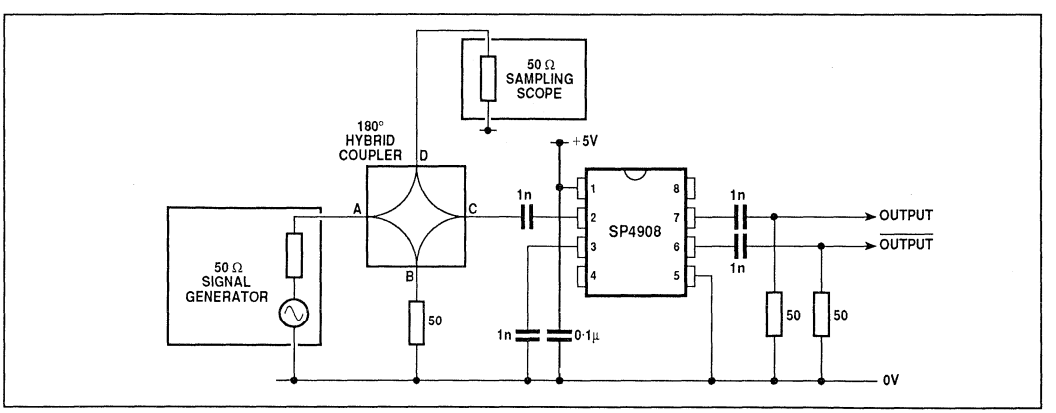


Fig. 4 Test circuit

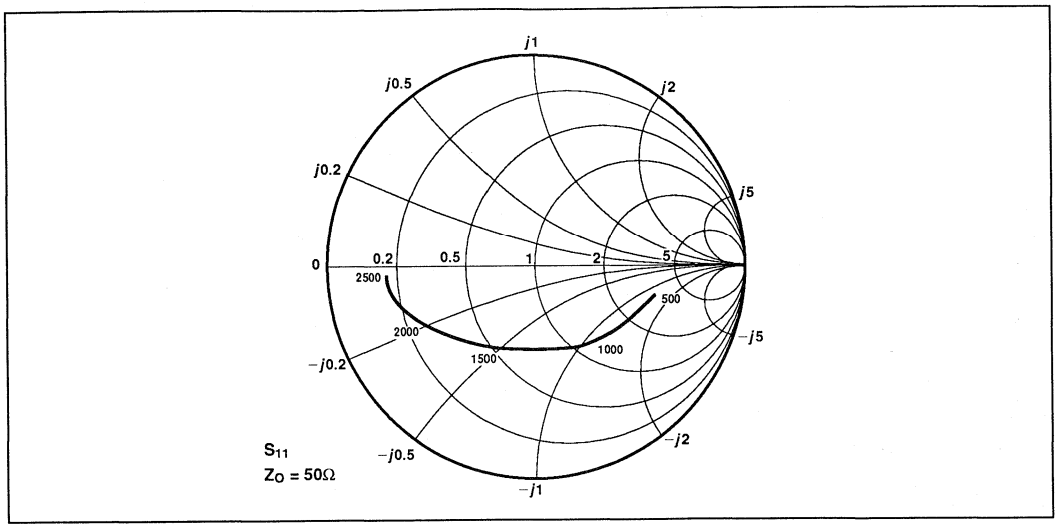


Fig. 5 Typical input impedance (frequencies in MHz)

SP4914

2·5GHz ÷128 PRESCALER

The SP4914 prescaler is one a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage.

FEATURES

- High Speed Operation 2·5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 250mW
- Single 5V Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Electrostatic Protection †

† ESD precautions must be observed

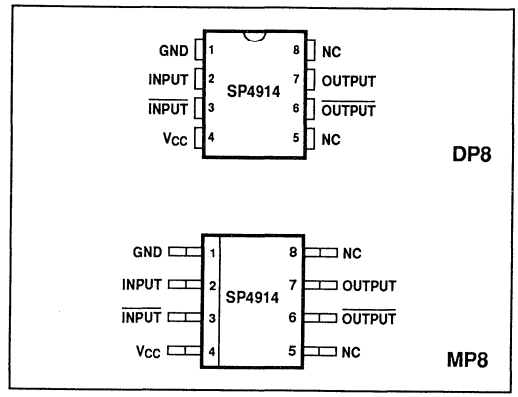


Fig 1. Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+6·5V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP4914 NA DP
SP4914 NA MP

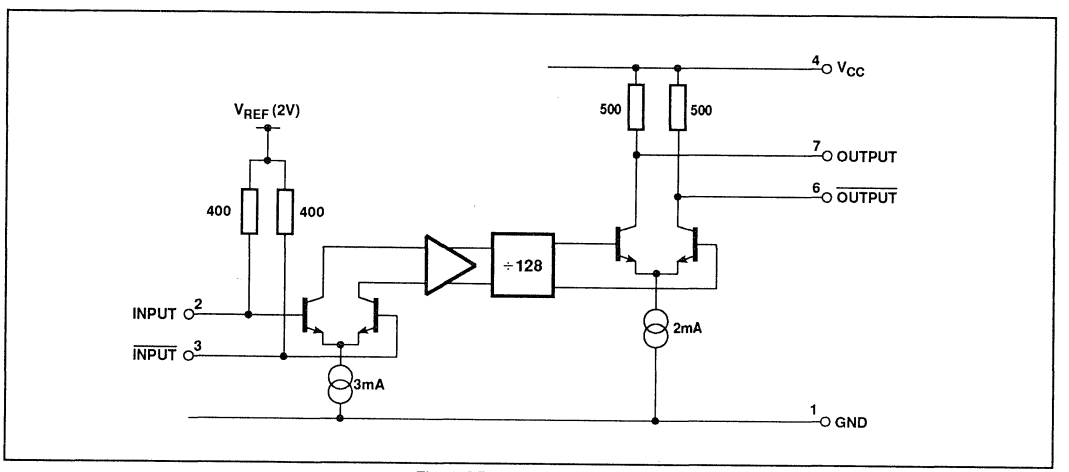


Fig. 2 SP4914 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = −10°C to +85°C, V_{CC} = +4·75V to +5·25V (Test circuit see Fig. 4)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	4		50	65	mA	V_{CC} = +5V
Input sensitivity	2,3					
500MHz to 1800MHz				50	mV	RMS sinewave, measured in 50Ω system,
2500MHz				100	mV	see Figs 3 and 4.
Input impedance (series equivalent)	2,3		50		Ω	See Fig. 5
			2		pF	
Output voltage with f_{IN} = 2500MHz	6,7	0·8	1		V p-p	V_{CC} = +5V, no load
		0·5	0·8		V p-p	V_{CC} = +5V, load as Fig. 4

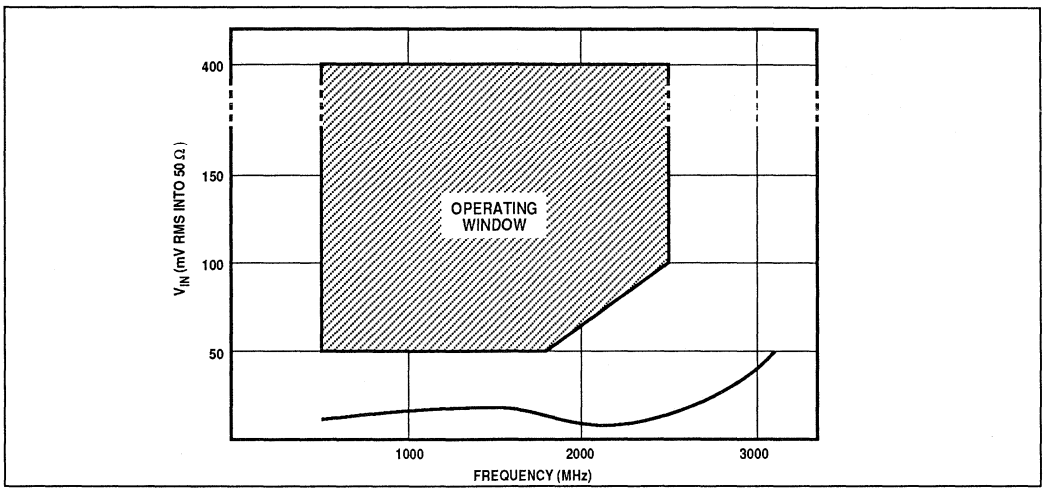


Fig. 3 Typical input sensitivity

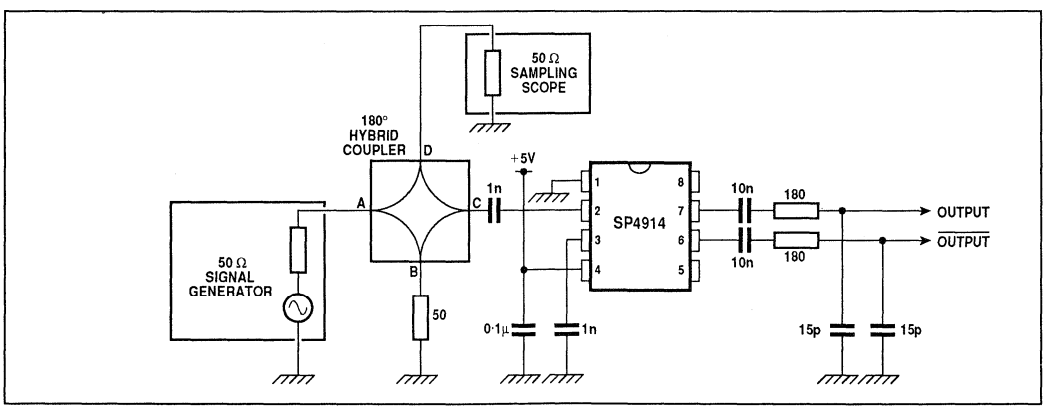


Fig. 4 Test circuit

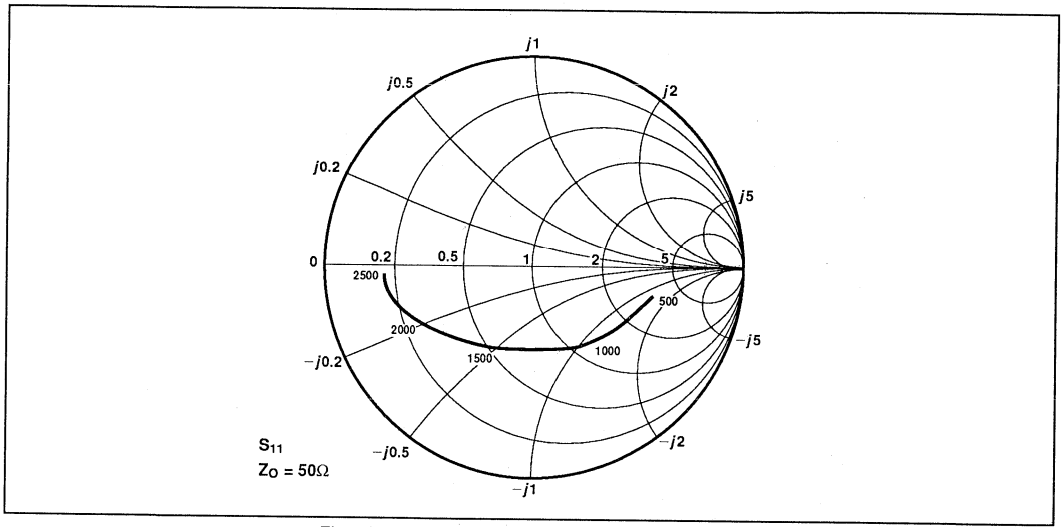


Fig. 5 Typical input impedance (frequencies in MHz)

SP4916

2·5GHz ÷512 PRESCALER

The SP4916 prescaler is one a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a complementary output stage.

FEATURES

- High Speed Operation 2·5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 250mW
- Single 5V Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Electrostatic Protection †

† ESD precautions must be observed

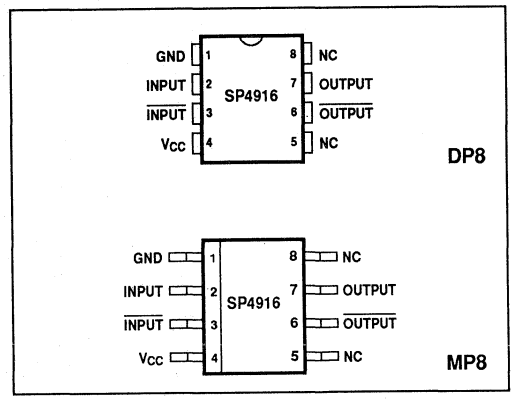


Fig 1. Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+6·5V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP4916 NA DP
SP4916 NA MP

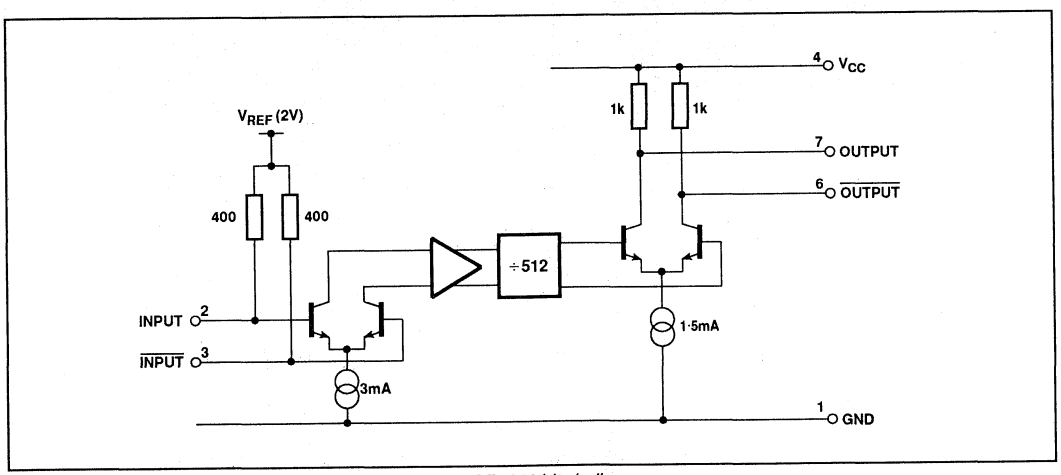


Fig. 2 SP4916 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = −10°C to +85°C, V_{CC} = +4·75V to +5·25V (Test circuit see Fig. 4)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	4		50	65	mA	V_{CC} = +5V
Input sensitivity	2,3					
500MHz to 1800MHz				50	mV	RMS sinewave, measured in 50Ω system,
2500MHz				100	mV	see Figs 3 and 4.
Input impedance (series equivalent)	2,3		50		Ω	See Fig. 5
			2		pF	
Output voltage with f_{IN} = 2500MHz	6,7	1·2	1·5		V p-p	V_{CC} = +5V, no load
		0·8	1·3		V p-p	V_{CC} = +5V, load as Fig. 4

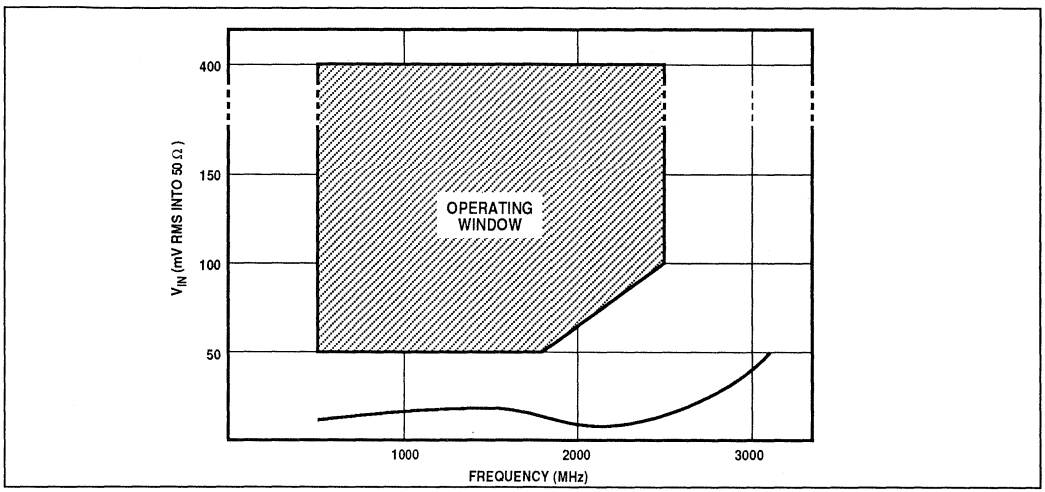


Fig. 3 Typical input sensitivity

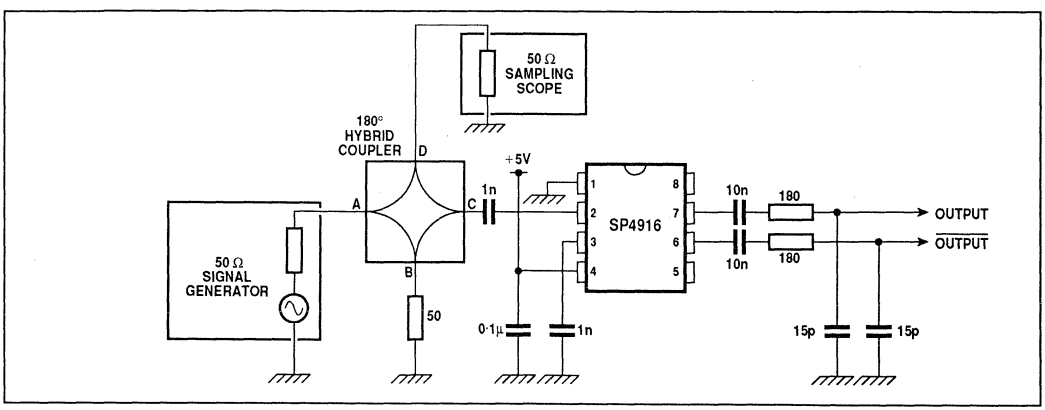


Fig. 4 Test circuit

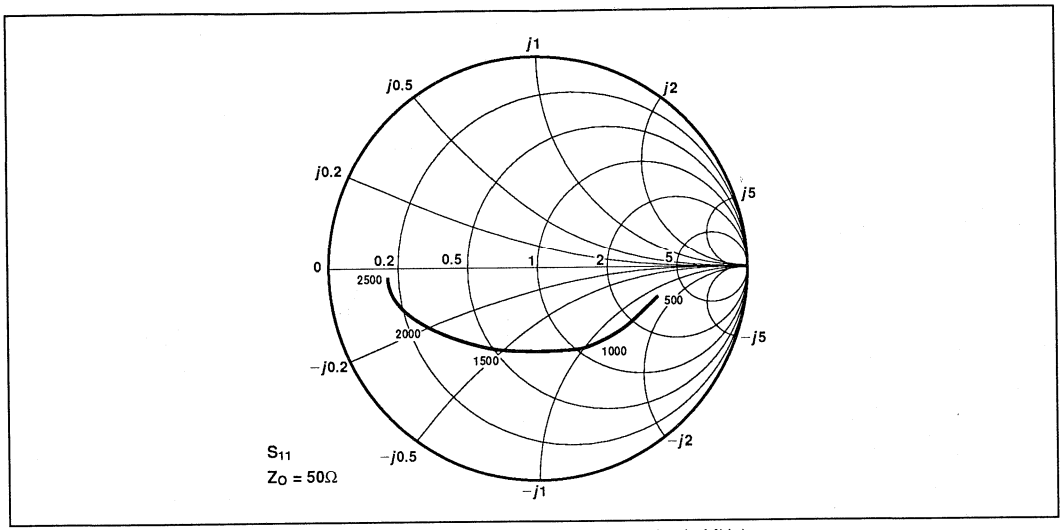


Fig. 5 Typical input impedance (frequencies in MHz)

SP4982

2·5GHz ÷8192 PRESCALER

The SP4982 prescaler is one a range of very high speed low power prescalers for use in consumer applications such as satellite TV receivers. The device features a CMOS compatible output stage.

FEATURES

- High Speed Operation 2·5GHz
- Silicon Technology for Low Phase Noise
- Very Low Power Dissipation 220mW
- Single 5V Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Electrostatic Protection †

† ESD precautions must be observed

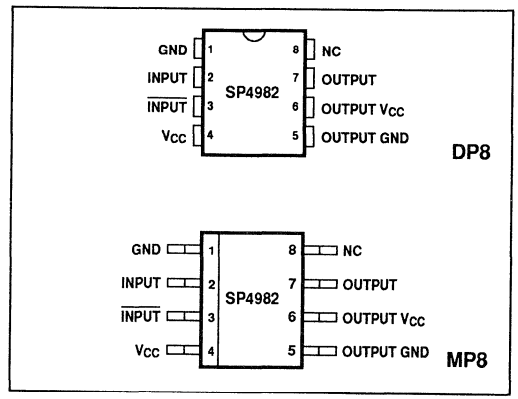


Fig 1. Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+6·5V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP4982 NA DP
SP4982 NA MP

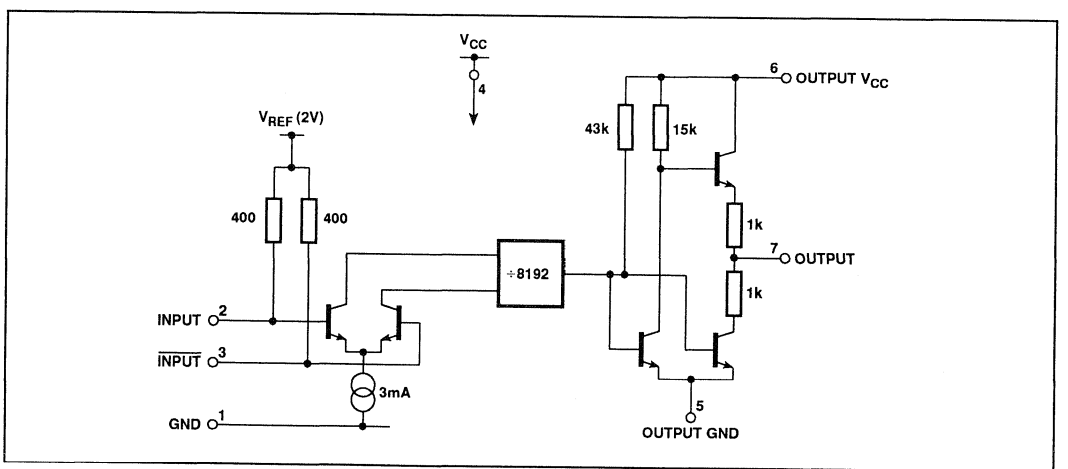


Fig. 2 SP4982 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = −10°C to +85°C, V_{CC} = +4·75V to +5·25V (Test circuit see Fig. 4)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	4		44	65	mA	V_{CC} = +5V
Input sensitivity	2,3					
500MHz to 1800MHz				50	mV	RMS sinewave, measured in 50Ω system,
2500MHz				100	mV	see Figs 3 and 4.
Input impedance (series equivalent)	2,3		50		Ω	See Fig. 5
					pF	
Output voltage high, f_{IN} = 2500MHz	7	V_{CC}−0·75			V p-p	V_{CC} = +5V, load as Fig. 4
Output voltage low, f_{IN} = 2500MHz	7			0·5	V p-p	V_{CC} = +5V, load as Fig. 4

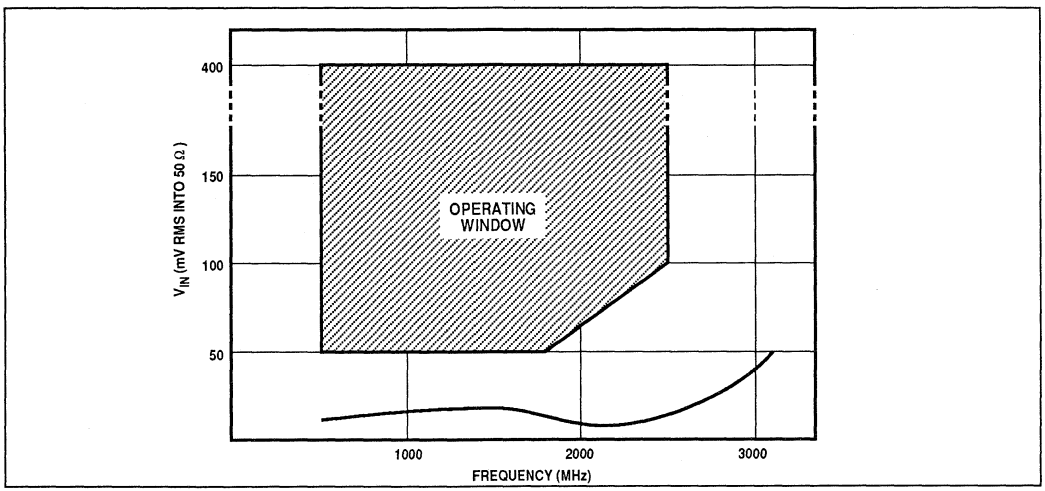


Fig. 3 Typical input sensitivity

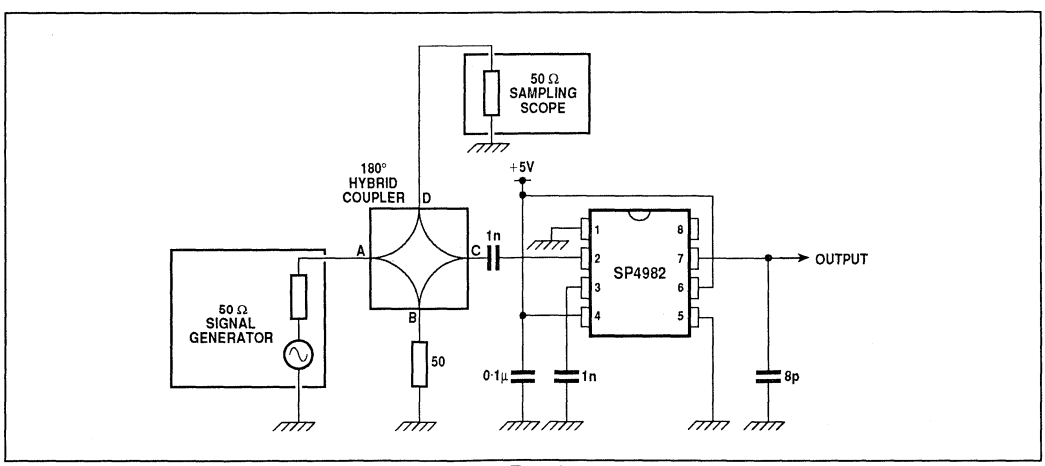


Fig. 4 Test circuit

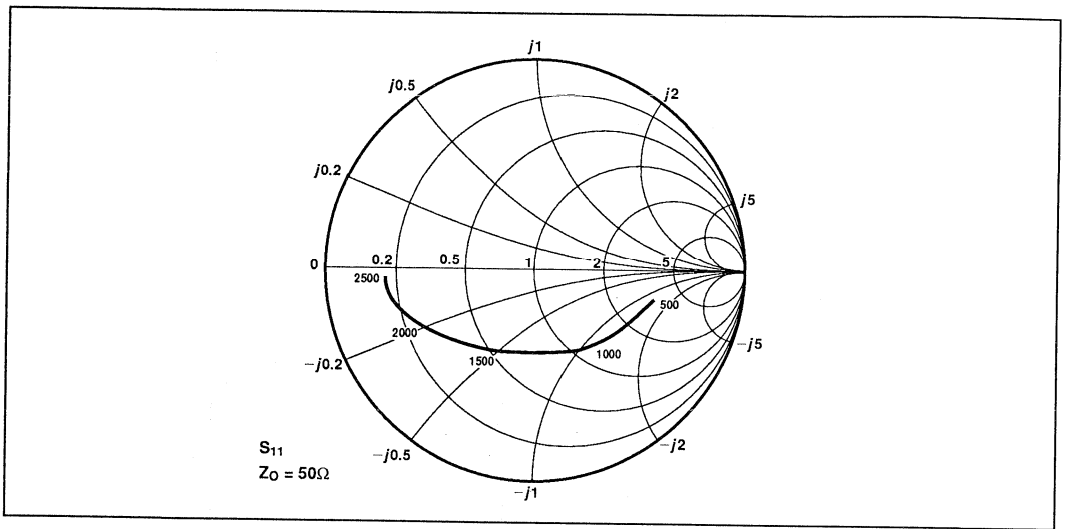


Fig. 5 Typical input impedance (frequencies in MHz)

Section 2

TV/Cable/Satellite Tuner PLL Circuits

GEC PLESSEY
SEMICONDUCTORS

SP5022

1.6GHz 3–WIRE BUS SYNTHESISER

The SP5022 is a single chip frequency synthesiser designed for tuning systems requiring local oscillator frequencies up to 1.6GHz.

The circuit consists of a divide by 8 prescaler with its own preamplifier and a 15 bit programmable divider. Comparison frequencies are obtained either from a crystal controlled on–chip oscillator or from an external source. Four reference oscillator divider ratios are available, programmed by 2 bits within the data word.

The phase comparator has a charge pump output with an amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

Three independently programmable open collector outputs are included which may be used for band selection.

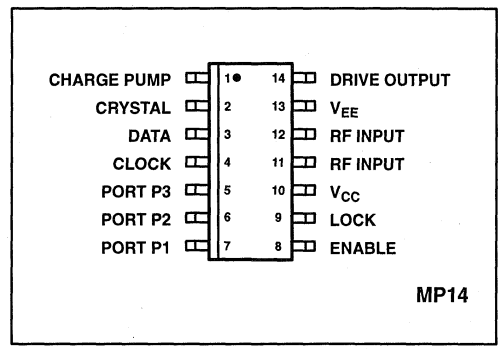


Fig 1. Pin connections – top view

FEATURES

- Complete 1.6GHz Single Chip System
- User Defined Step Size
- Low Power Consumption
- Phase Lock Detector
- Varactor Drive Amplifier Disable
- Charge Pump Disable
- Low Radiation
- 20 Bit Serial Data Entry
- Three Controllable High Current Outputs
- Full ESD Protection†

† Normal ESD handling procedures must be observed

APPLICATIONS

- Double Conversion Tuners
- TV Tuners
- Cable TV Systems
- VCRs
- Satellite TV when used with SP4902 2.5GHz Prescaler

ORDERING INFORMATION

SP5022F/KG/MPAS – (14 lead Miniature Plastic Package)

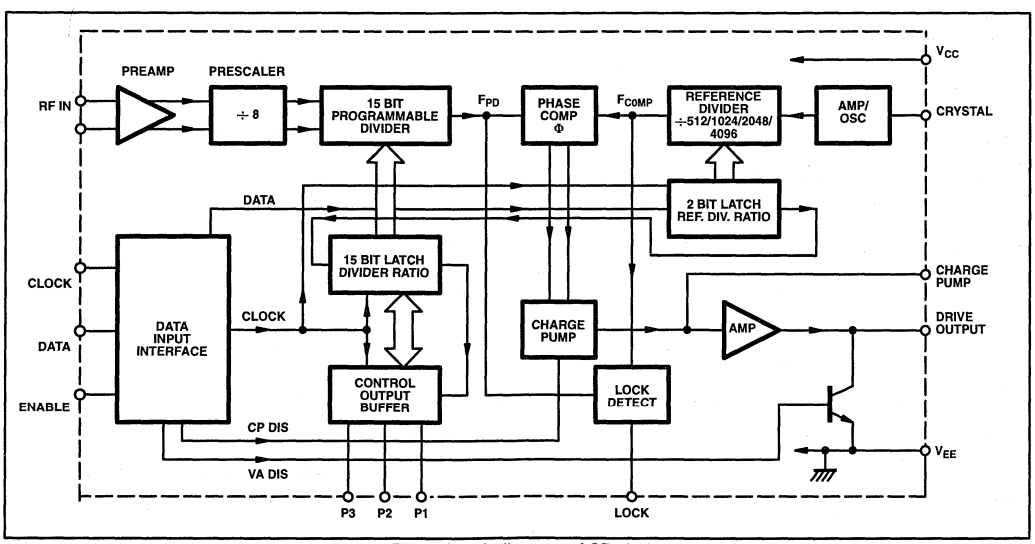


Fig. 2 Block diagram of SP5022

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	10		55	68	mA	V_{CC}=5V
Prescaler input voltage		11, 12	12.5		400	mV_{RMS}	80MHz to 1GHz sinewave
Prescaler input voltage		11, 12	30		400	mV_{RMS}	1.3GHz
Prescaler input voltage		11, 12	70		400	mV_{RMS}	1.6GHz See Fig.4
Prescaler input impedance		11, 12		50		Ω	
Input capacitance				2		pF	
High level input voltage		3, 4, 8	3		V_{CC}	V	
Low level input voltage		3, 4, 8	0		0.7	V	
High level input sink current		3, 4, 8			1	µA	V_{IN}=5.5V V_{CC}=5.5V
Low level input source current		4			5	µA	V_{IN}=0V V_{CC}=5.5V
Low level input source current		3, 8			250	µA	V_{IN}=0V V_{CC}=5.5V
Clock input hysteresis		4		0.4		V	
Clock rate		4			0.5	MHz	
Data setup time	t2	3	300			ns	See Fig. 6
Data hold time	t3	3	600			ns	See Fig. 6
Enable setup time	t1	8	300			ns	See Fig. 6
Enable hold time	t5	8	600			ns	See Fig. 6
Clock–to–Enable time	t4	8	300			ns	See Fig. 6
Charge pump output current		1	±200	±300		µA	V pin 1=2.0V
Charge Pump Output Leakage Current				±1	±5	nA	V pin 1=2.0V
Drift Due to Leakage					5	mV/s	At collector of external varicap drive transistor
Charge Pump Drive Output current		14	1			mA	V pin 14=0.7V
Charge Pump Amplifier Gain				6400			Pin 14 current=100µA
Oscillator Temperature Stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Comparison Frequency (at phase detector)					16	kHz	
External Reference Input Frequency		2	3.5		16	MHz	
External Reference Input Amplitude		2	200		500	mVp–p	AC coupled sinewave
Reference Crystal Frequency		2	3.5		8	MHz	"Parallel Resonant" Crystal

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Port and Lock Sink Current		5–7, 9	10			mA	V_{OUT}=0.7V
Port Leakage Current		5–7			10	µA	V_{OUT}=13.2V
Lock Leakage Current		9			10	µA	$V_{OUT}=V_{CC}$
Varactor Drive Amplifier Disable		8	–350			µA	V_{IN} <0V
Charge Pump Disable		3	–350			µA	V_{IN} <0V
Test Mode		4	–350			µA	V_{IN} <0V

ABSOLUTE MAXIMUM RATINGS (All voltages are referred to V_{EE}=0V)

Prescaler input signal	11, 12			2.5	V_{PP}
DC VOLTAGES					
Supply	10	–0.3		7	V
Output ports:–	5–7				
Off state		–0.3		14	V
On state		–0.3		6	V
Loop amplifier DC offset	1, 14	–0.3		V_{CC}+0.3	V
Reference/Crystal input	2	–0.3		V_{CC}+0.3	V
Data bus inputs	3, 4, 8	–0.3		V_{CC}+0.3	V
Prescaler DC offset	11, 12	–0.3		V_{CC}+0.3	V
THERMAL RESISTANCE MP14					
Die to ambient				123	°C/W
Die to case				45	°C/W
Power consumption (@ V_{CC}=5.5V)				375	mW
INPUT/OUTPUT PROTECTION MIL STD–883B METHOD 3015	All pins except 14				
Electrostatic discharge		2.0			kV
INPUT/OUTPUT PROTECTION MIL STD–883B METHOD 3015Electrostatic discharge	14	1.5			kV

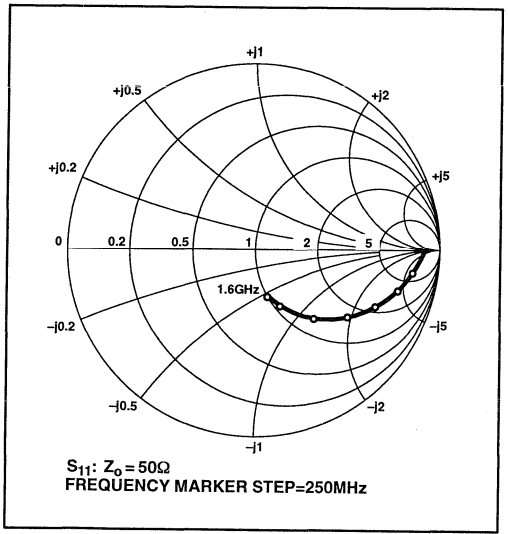


Fig. 3 Typical input impedance

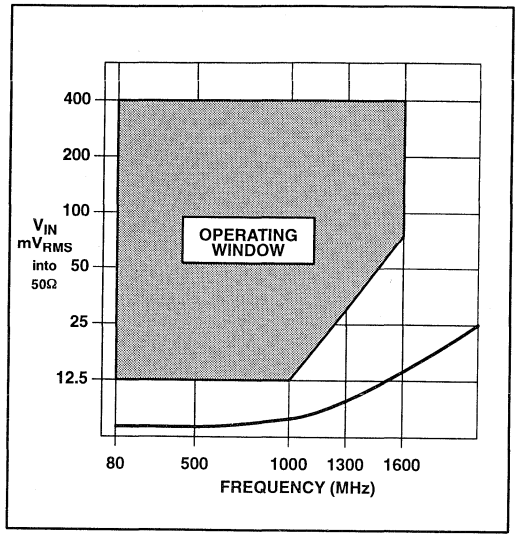


Fig. 4 Typical input sensitivity

FUNCTIONAL DESCRIPTION

The SP5022 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source.

The system is controlled by a standard 3–wire bus comprising data, clock and enable inputs. The programming word consists of 20 bits, three of which are used for port selection, 15 to set the programmable divider, and the remaining two to select the reference division ratio. The programming format is shown in Fig. 6.

Data is only transferred to the internal shift register during enable high periods. The clock input is disabled when the enable is low. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable.

The local oscillator output frequency is input to the prescaler/programmable divider where it is divided down by the ratio programmed. The output of the programmable divider, F_{pd}, is fed to the phase comparator where it is compared in both phase and frequency to the comparison frequency, F_{comp}.

F_{comp} may be obtained by two means, either by feeding in an external reference, or by the use of an on–board crystal controlled oscillator. The programmable reference divider between the reference oscillator and the phase comparator gives a choice of comparison frequency. As an example the comparison frequencies and related LO step sizes for a 8MHz crystal are shown in Table 1 below :

Comparison Frequency	15.625 kHz	7.8125 kHz	3.90625 kHz	1.953125 kHz
Local Osc. Step Size	125 kHz	62.5 kHz	31.25 kHz	15.625 kHz

Table 1 Comparison and step frequencies with an 8MHz crystal

An external oscillator source up to 16MHz may alternatively be used. By careful choice of reference oscillator frequency and divider ratio the local oscillator step size can be optimised for each application. The phase comparator can operate with a comparison frequency up to 16kHz thus giving the choice of a LO step size up to a maximum to128kHz.

The programmable divider is preceded by an input RF preamplifier and a high speed, low radiation prescaler thus giving excellent sensitivity at input frequencies between 80 and 1600MHz.

A 'lock detect' circuit is provided which generates a flag when the loop has obtained lock. 'In lock' is indicated by a high impedance state on the lock output.

The SP5022 also contains three open collector output ports, ports P1–P3. These may be used for a variety of band switching or driving purposes and are programmed by the first three bits in the data word.

VARACTOR LINE/CHARGE PUMP DISABLE AND TEST FEATURES

The SP5022 offers the following facilities to aid testing and alignment of oscillators and tuners.

Varactor Line Disable – set by applying a negative voltage to the ENABLE pin and sourcing greater than 350μA from the device.

Charge Pump Disable – set by applying a negative voltage to the DATA pin.

Test Mode – set by applying a negative voltage to the CLOCK pin.

When in TEST mode the inputs to the Phase Comparator F_{pd} and F_{comp} are available on ports P3 and P2 respectively when the first three MSBs of the data word P1, P2, P3 are set to 010.

DOUBLE CONVERSION TUNER SYSTEMS

The high 1.6GHz max operating frequency of the SP5022 enables the construction of double conversion high IF tuners when used in conjunction with the SP5058, a 2.6GHz frequency synthesiser.

A typical system will use the SP5058 as the first LO control for full band upconversion to an IF of greater than 1GHz; the SP5022 is used to control the 2nd LO which downconverts the 1st IF to either a conventional IF, TV channel or other chosen frequency.

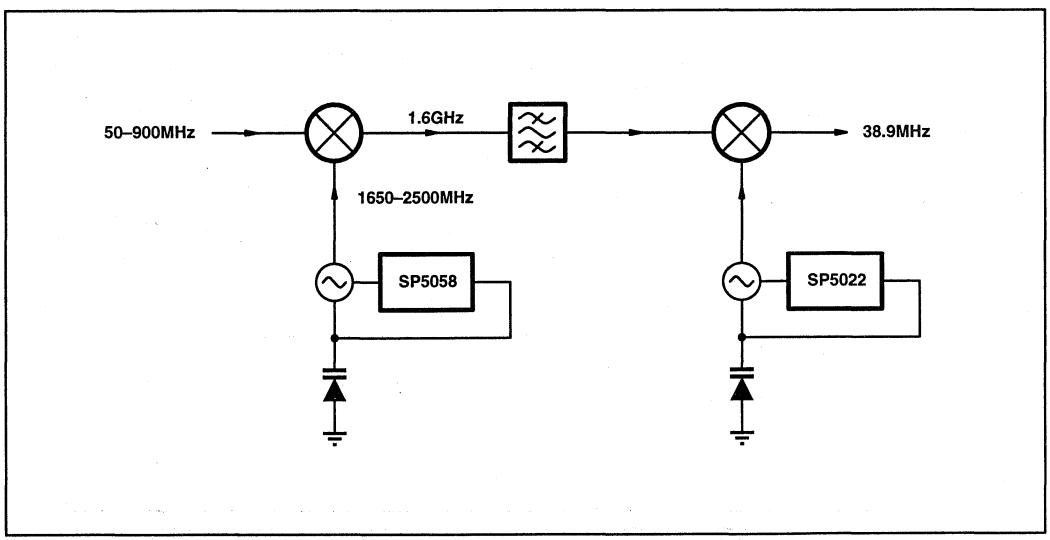
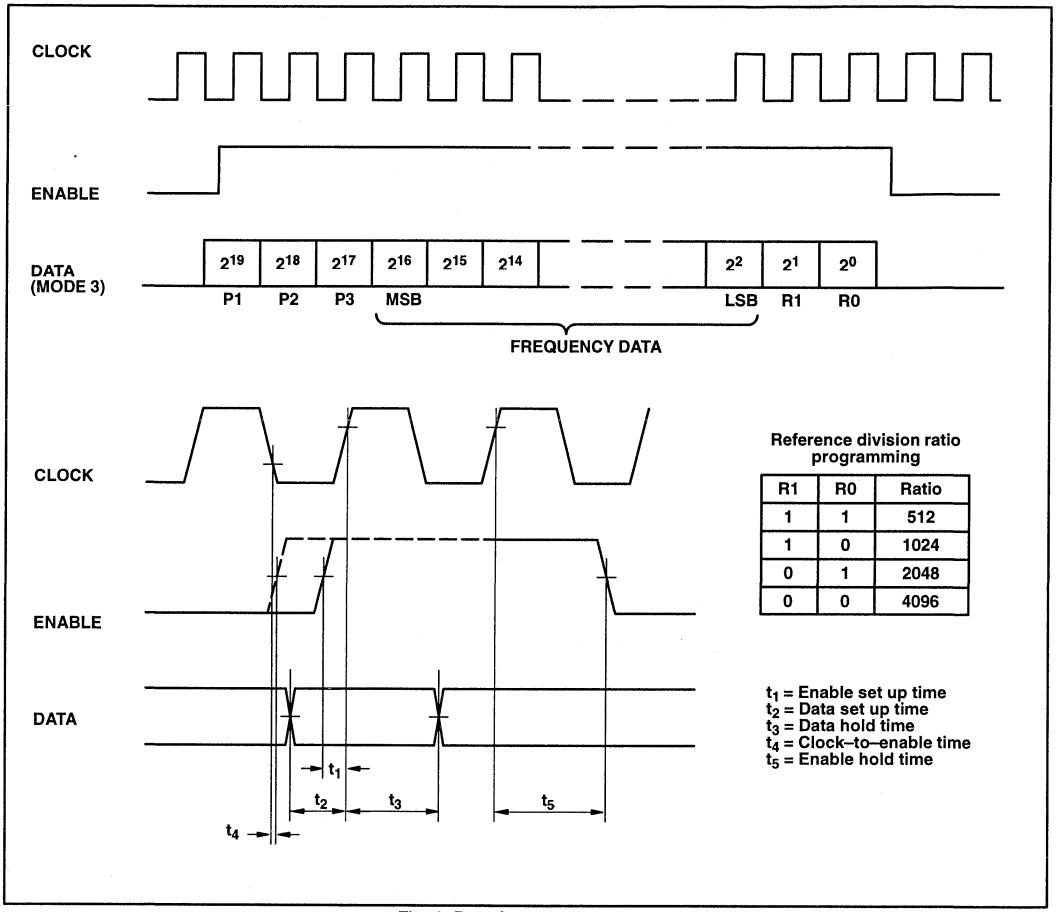


Fig. 5 Example of double conversion from VHF/UHF frequencies to TV IF



Reference division ratio programming

R1	R0	Ratio
1	1	512
1	0	1024
0	1	2048
0	0	4096

t_1 = Enable set up time
t_2 = Data set up time
t_3 = Data hold time
t_4 = Clock–to–enable time
t_5 = Enable hold time

Fig. 6 Data format and timing

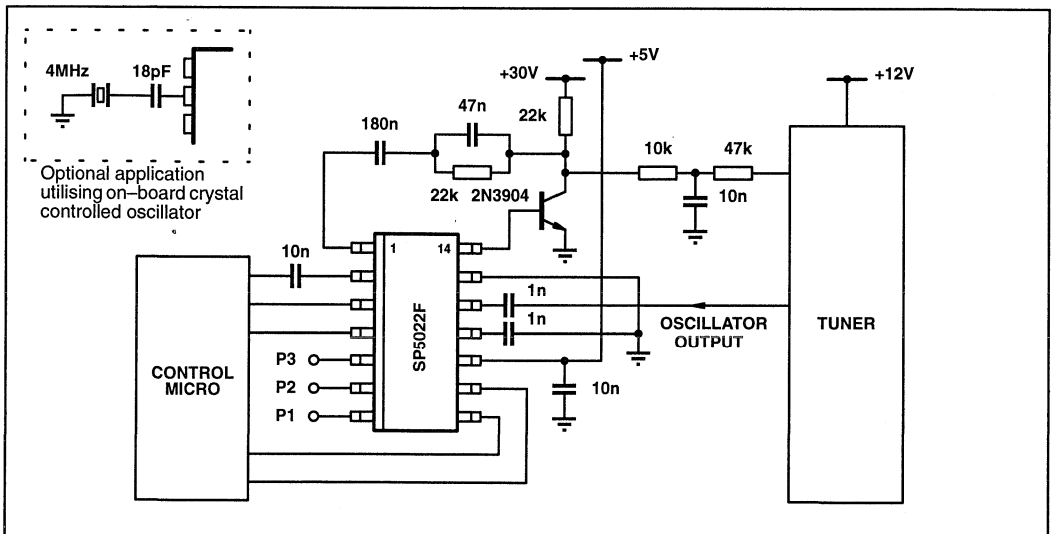
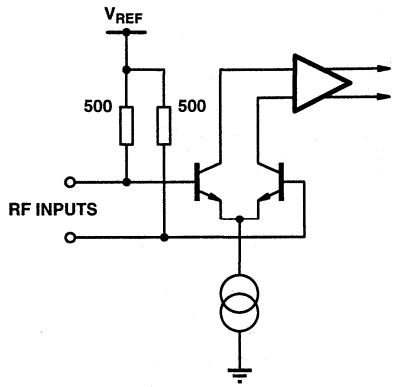
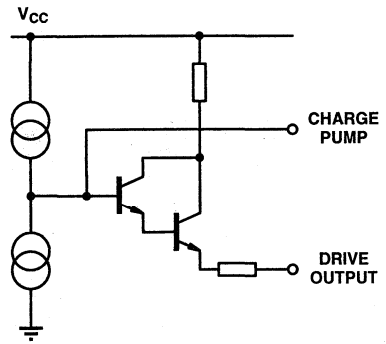


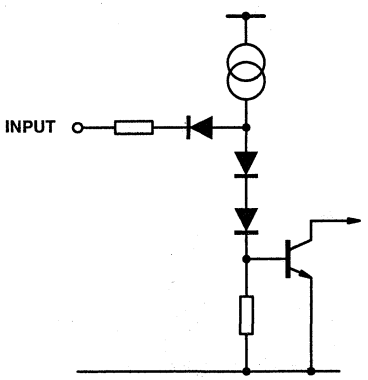
Fig. 7 Typical application



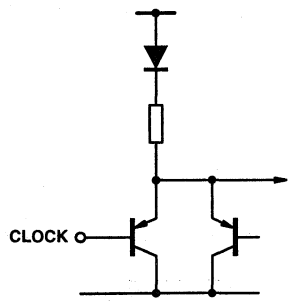
RF input



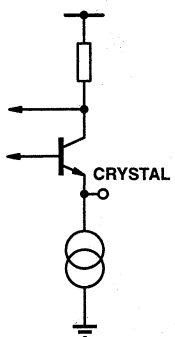
Loop amplifier



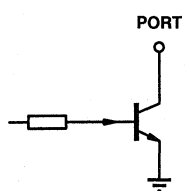
Enable and data inputs



Clock input



Reference oscillator



Output ports P1–P3

Fig.8 Input/Output interface circuits

DS2452 2.1

SP5024

1.3 GHz 3-WIRE BUS CONTROLLED SYNTHESISER

(Supersedes edition in the Consumer IC Handbook, September 1991)

The SP5024 is a programming variant of the SP5510 allowing the design of one tuner with either I²C bus or 3-wire bus format depending on which device is inserted. The SP5024, when used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divide-by-8 prescaler with its own preamplifier and a 15 bit programmable divider controlled by a serially - loaded data register. Four open-collector outputs, each independently programmable, are included. The device has two modes of operation selected by the 'mode select input'. In mode 1 the comparison frequency is 7.8125kHz and the programmable divider MSB is bypassed; mode 2 comparison frequency is 6.25kHz. The comparison frequencies are both obtained from a 4MHz crystal controlled on-chip oscillator. The comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete 1.3GHz Single Chip System
- Dual Standard 50kHz or 62.5kHz Step Size
- Low Power Consumption (5V 40mA)
- Programming Compatible with Toshiba TD6380 and TD6381 *
- Pin Compatible with SP5510 *
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- ESD Protection †

* See notes on pin compatibility, page 4.
† Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV When Combined With SP4902 2.5 GHz Prescaler
- Cable Tuning Systems
- VCRs

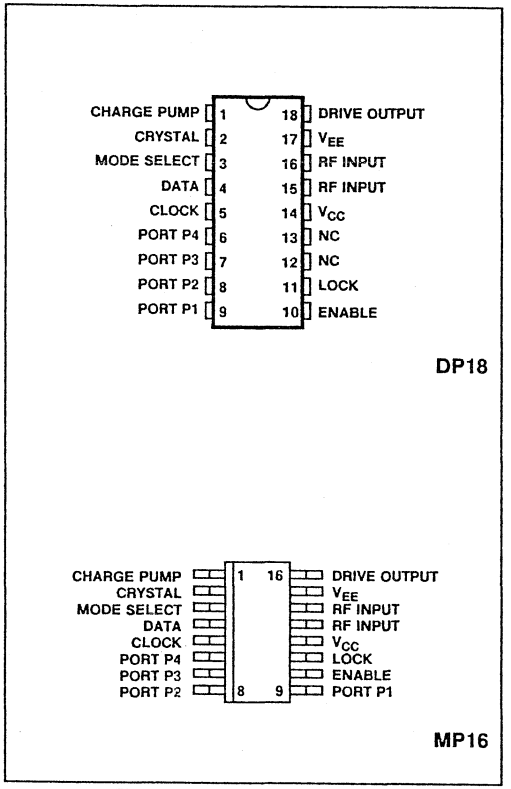


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP5024 DP - (18 lead Plastic Package)
SP5024S MP - (16 lead Miniature Plastic Package)

ELECTRICAL CHARACTERISTICS

T_{amb} = -20°C to +80°C, V_{CC} = +4.5V to 5.5V Reference frequency = 4MHz. Pin numbers refer to SP5024 (DP package) These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	14		40	55	mA	V_{CC} = 5V
Prescaler Input Voltage		15, 16	12.5		300	mV_{RMS}	50MHz to 1GHz sinewave
Prescaler Input Voltage		15, 16	30		300	mV_{RMS}	1.3GHz, see Fig. 5
Prescaler Input Impedance Input Capacitance		15, 16		50 2		Ω pF	
High Level Input Voltage		4,5,10	3		V_{CC}	V	
High Level Input Voltage		3	4		V_{CC}	V	
Low Level Input Voltage		3,4,5,10	0		0.6	V	
High Level Input Current		4,5,10			1	μA	V_{IN} = 5.5V V_{CC} = 5.5V
Low Level Input Current		5			5	μA	V_{IN} = 0V V_{CC} = 5.5V
Low Level Input Current		4,10			-250	μA	V_{IN} = 0V V_{CC} = 5.5V
High Level Input Current		3			150	μA	V_{IN} = 5.5V V_{CC} = 5.5V
Low Level Input Current		3			-1	μA	V_{IN} = 0V V_{CC} = 5.5V
Clock Input Hysteresis		5		0.4		V	
Clock Rate		5			0. 5	MHz	
Data Setup Time	t_2	4	300			ns	See Fig. 3
Data Hold Time	t_3	4	600			ns	See Fig. 3
Enable Setup Time	t_1	10	300			ns	See Fig. 3
Enable Hold Time	t_5	10	600			ns	See Fig. 3
Clock-to-Enable Time	t_4	10	300			ns	See Fig. 3
Charge Pump Output Current		1		±150		μA	V pin 1 = 2.0V
Charge Pump Output Leakage Current		1			±5	nA	V pin 1 = 2.0V
Drift Due to Leakage					5	mV/s	At Collector of External Varicap Drive Transistor
Charge Pump Drive Output Current		18	1			mA	V pin 18 = 0.7V
Charge Pump Amplifier Gain				6400			Pin 18 Current 100μA
Oscillator Temperature Stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Recommended Crystal Series Resistance			10		200	Ω	"Parallel resonant" Crystal
Crystal Oscillator Drive Level		2		40		mV p-p	
Crystal Oscillator Source Impedance		2		-400		Ω	Nominal Spread ±15%

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Port and lock sink current		6 - 9,11	10			mA	$V_{OUT} = 0.7V$
Port leakage current		6-9			10	µA	$V_{OUT} = 13.2V$
Lock leakage current		11			10	µA	$V_{OUT} = V_{CC}$
Varactor Drive Amp Disable		10	-350			µA	$V_{IN} < 0V$
Charge Pump Disable		4	-350			µA	$V_{IN} < 0V$

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to $V_{EE} = 0V$

Parameter	Pin SP5024	Pin SP5024 S	Value		Units	Conditions
			Min	Max		
Supply voltage	14	12	-0.3	6	V	
Prescaler inputs	15, 16	13, 14		2.5	Vp-p	
Output ports	6-9	6 - 9	-0.3 -0.3	14 6	V V	Port in off state Port in on state
Total port output current	6-9	6 - 9		50	mA	
Prescaler DC offset	15, 16	13, 14	-0.3	$V_{CC} + 0.3$	V	
Loop amplifier DC offset	1, 18	1, 16	-0.3	$V_{CC} + 0.3$	V	
Crystal oscillator DC offset	2	2	-0.3	$V_{CC} + 0.3$	V	
Data bus inputs	4, 5, 10	4, 5, 10	-0.7	$V_{CC} + 0.3$	V	With V_{CC} applied
Storage temperature			-55	+125	°C	
Junction temperature				+150	°C	
DP 18 thermal resistance, chip-to-ambient DP 18 thermal resistance, chip-to-case				78 24	°C/W °C/W	
MP 16 thermal resistance, chip-to-ambient MP 16 thermal resistance, chip-to-case				111 41	°C/W °C/W	
Power consumption at 5V				275	mW	All ports off

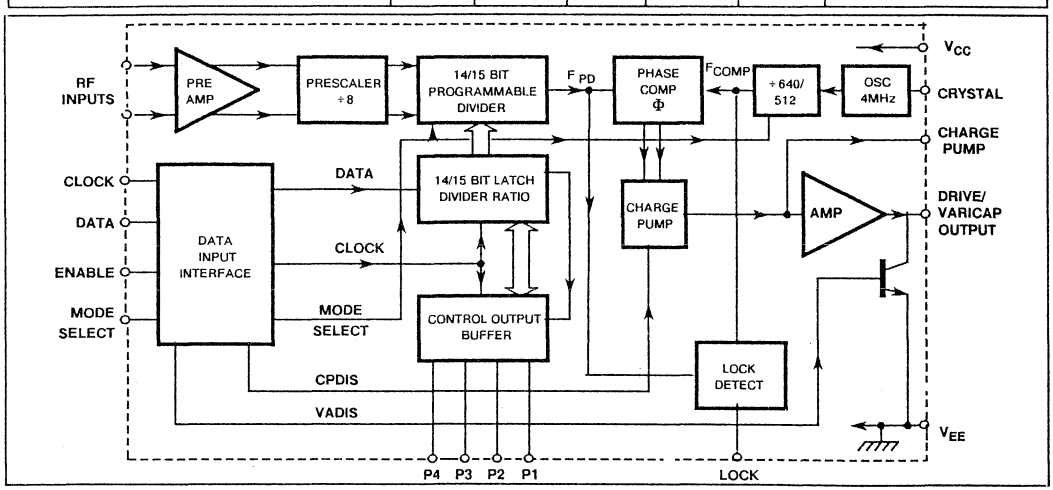


Fig.2. Block diagram

FUNCTIONAL DESCRIPTION

The SP5024 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock, enable, three-wire data bus. The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period. The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format as shown in Fig. 3.

The frequency is set by loading the programmable divider with the required 14/15 bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

The F_{COMP} is obtained by dividing the output of an on-chip crystal controlled oscillator. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 6.25kHz/7.8125kHz and, when multiplied back up to the synthesised LO, gives a minimum step size of 50kHz/62.5kHz, respectively.

The programmable divider is preceded by an input RF preamplifier and high speed, low radiation prescaler. The preamplifier is arranged to be self oscillating so giving excellent input sensitivity. The input sensitivity and impedance are shown in Figs. 5 and 7, respectively.

The SP5024 contains an improved lock detect circuit which generates a flag when the loop has attained lock. "Out of lock" is indicated by high impedance state.

The SP5024 contains four general purpose open collector outputs, ports P1-P4, which are capable of sinking at least 10mA. These outputs are set by the remaining four bits within the data word.

PIN COMPATIBILITY

The SP5024 may be used in SP5510 applications which require 3-wire bus as opposed to I²C bus data format. In SP5510 applications where the reference crystal is connected to pin 3, a small modification is required to ground the crystal as shown in Fig. 4.

Appropriate connections to the mode select input (pin 3) must also be made.

In mode 1 (pin 3 'HIGH') the SP5024 is programming and step size compatible with the Toshiba TD6380, and in mode 2 (pin 3 'LOW') it is compatible with the TD6381. In both modes a 4MHz crystal is used to derive F_{COMP}, unlike the TD6381 which requires a 3.2MHz crystal.

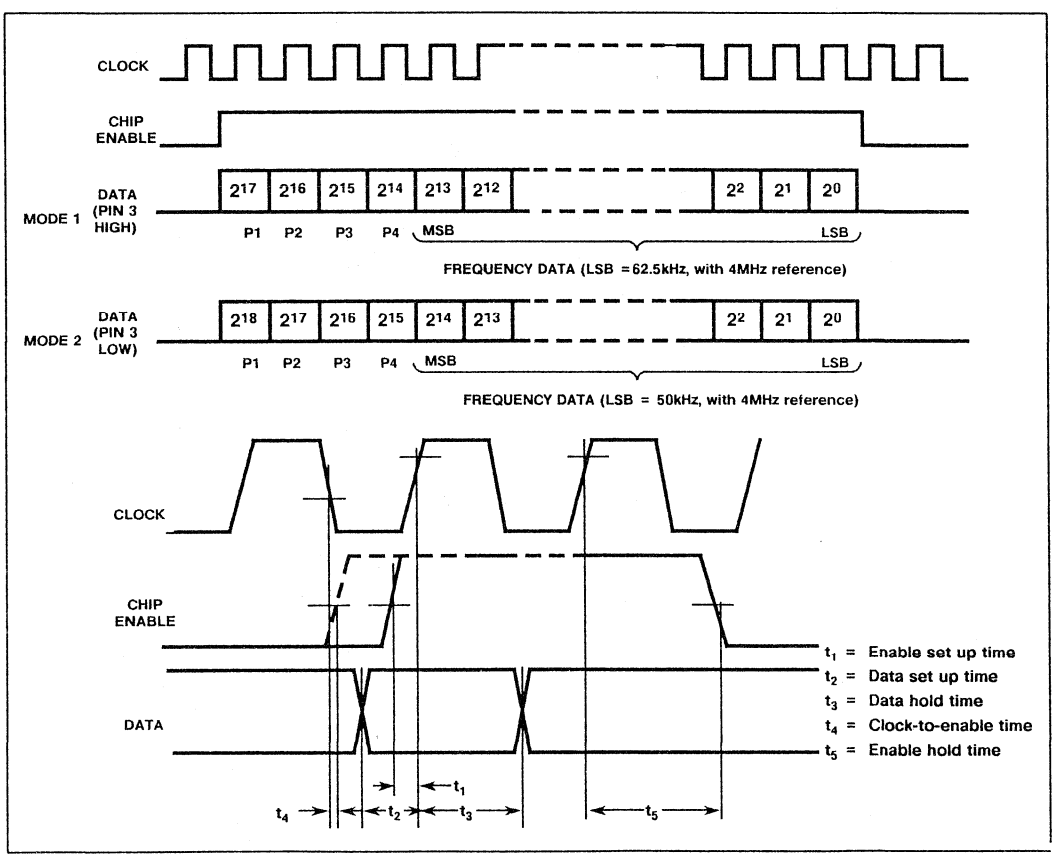


Fig.3. Data format and timing

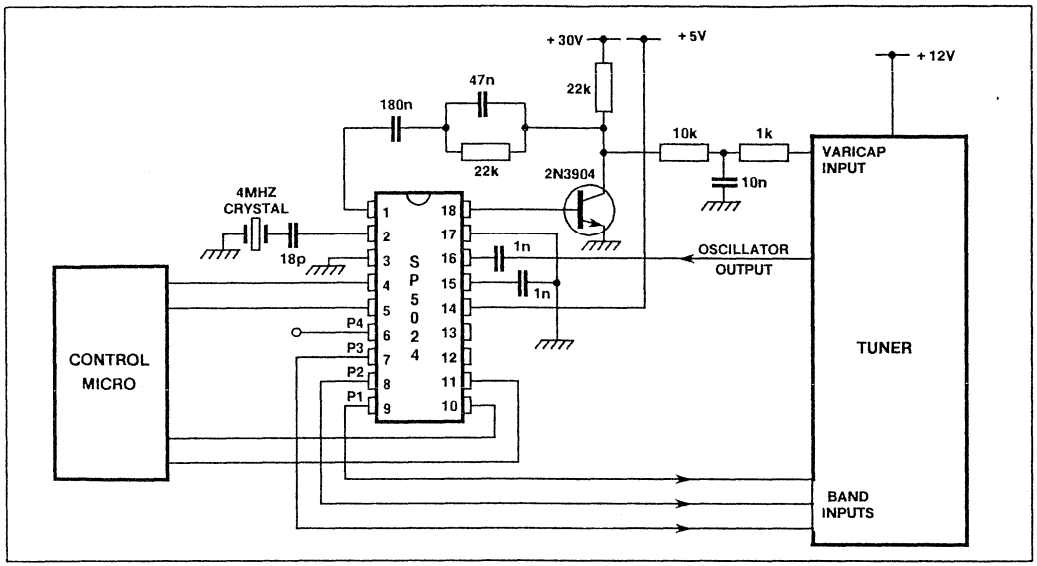


Fig.4. Typical application (F_{STEP} = 50kHz)

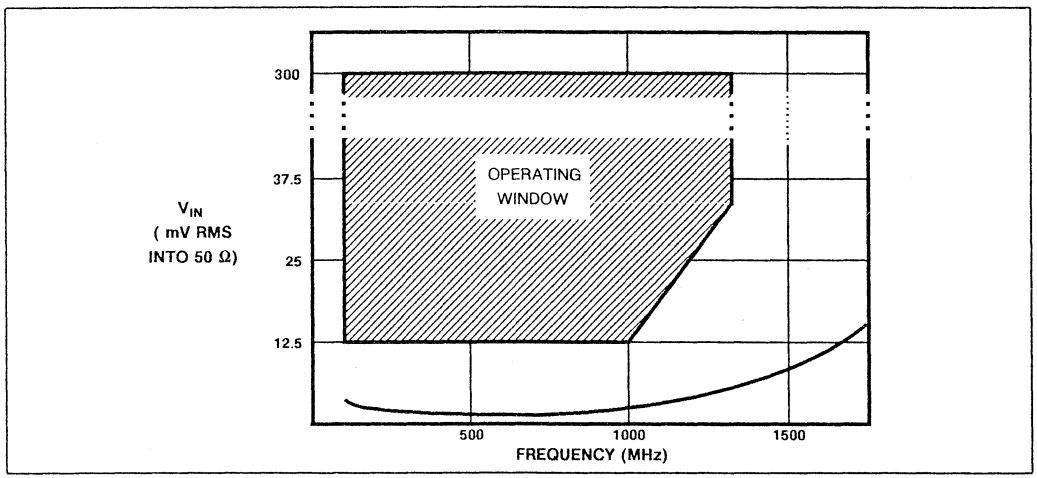


Fig.5. Typical input sensitivity

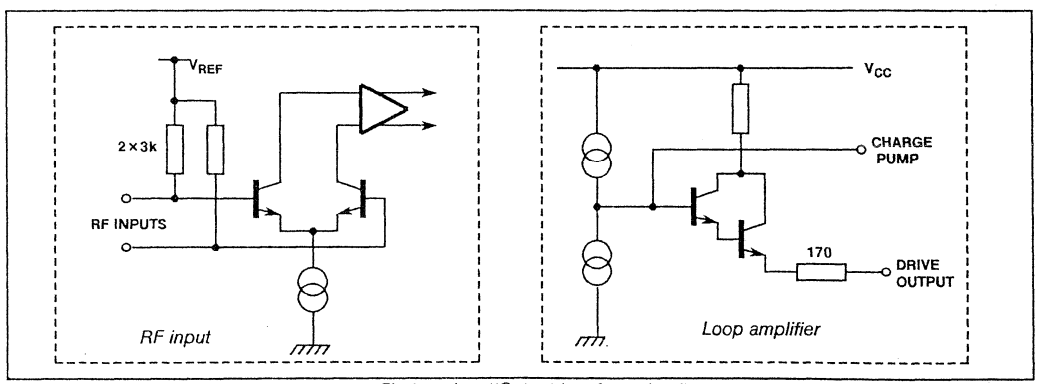


Fig.6a Input/Output interface circuits

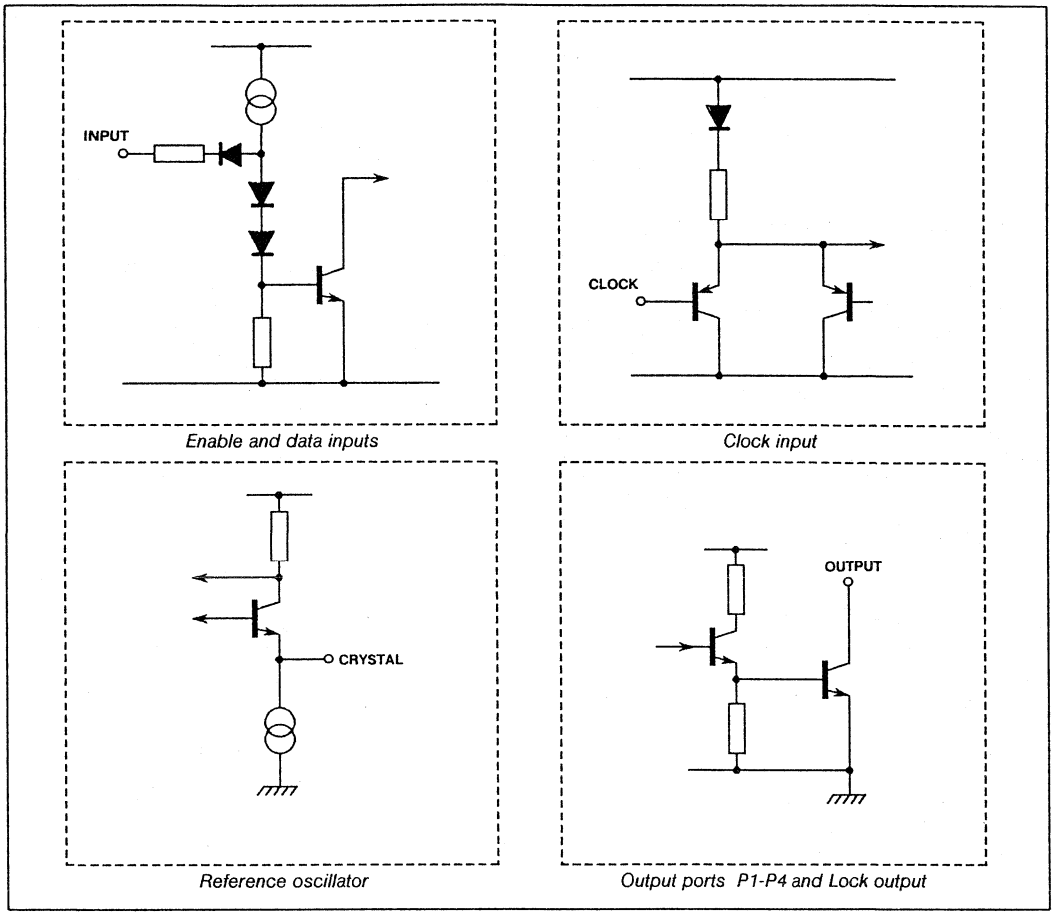


Fig.6b Input/Output interface circuits (continued)

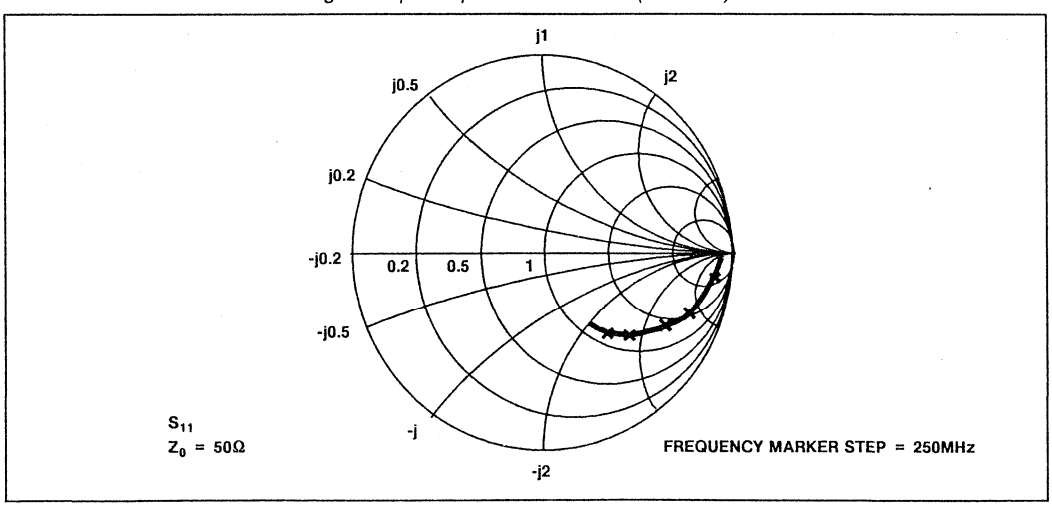


Fig.7 Typical input impedance

SP5026

1.0 GHz 3–WIRE BUS CONTROLLED SYNTHESISER

(Supersedes September 1992 edition)

The SP5026 is a programming variant of the SP5510, allowing the design of one tuner with either I²C bus or 3–wire bus format depending on which device is inserted. The SP5026, when used with a TV varicap tuner, forms a complete phase locked loop tuning system. The circuit consists of a divider–by–8 prescaler with its own preamplifier and a15–bit programmable divider controlled by a serially–loaded data register. Four open–collector outputs, each independently programmable, are included. The device has two modes of operation, selected by the 'mode select' input. In mode 1, the comparison frequency is 7.8125kHz and the programmable divider MSB is bypassed; mode 2 comparison frequency is 3.90625kHz. The comparison frequencies are both obtained from a 4MHz crystal controlled on–chip oscillator. The comparator has a charge pump output with an amplifier stage around which feedback may be applied. Only one external transistor is required for varicap line driving.

FEATURES

- Complete 1.0GHz Single Chip System
- Dual Standard 62.5kHz or 31.25 kHz Step Size
- Low power Consumption (5V 40mA)
- Function Compatible with Toshiba TD6380 and TD6382*
- Pin Compatible with SP5510 *
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- ESD Protection †

* See notes on pin compatibility on page 4
† Normal ESD handling procedures should be observed

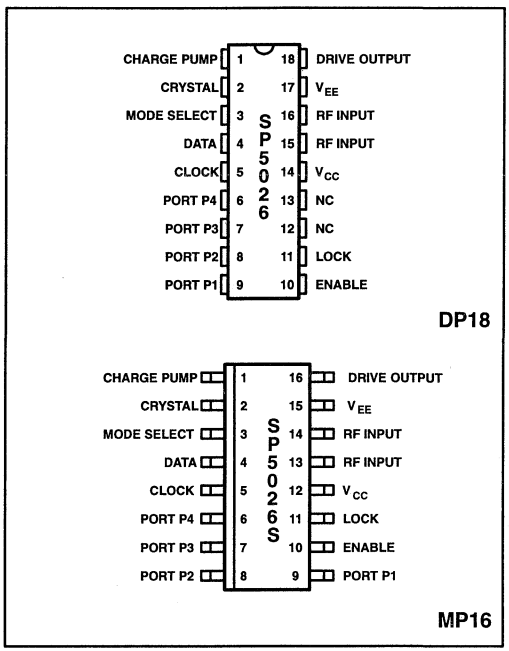


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz prescaler
- Cable tuning systems
- VCRs

ORDERING INFORMATION

SP5026 DP – (18 lead Plastic Package)
SP5026S MP – (16 lead Miniature Plastic Package)

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Frequency Standard = 4MHz. Pin numbers refer to SP5026 (DP package) These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	14		40	55	mA	V_{CC}=5V
Prescaler		15, 16	12.5		300	mV_{RMS}	50MHz to 1GHz sinewave
Prescaler input impedance		15, 16		50		Ω	
Input capacitance				2		pF	
High level input voltage		4, 5, 10	3		V_{CC}	V	
High level input voltage		3	4		V_{CC}	V	
Low level input voltage		3,4,5,10	0		0.7	V	
High level input source current		4, 5, 10			1	µA	V_{IN}=5.5V, V_{CC}=5.5V
Low level input source current		5			5	µA	V_{IN}=0V, V_{CC}=5.5V
Low level input source current		4, 10			250	µA	V_{IN}=0V, V_{CC}=5.5V
High level input sink current		3			150	µA	V_{IN}=5.5V, V_{CC}=5.5V
Low level input sink current		3			1	µA	V_{IN}=0V, V_{CC}=5.5V
Clock input hysteresis		5		0.4		V	
Clock rate		5			0.5	MHz	
Data setup time	t_2	4	300			ns	See Fig,3
Data hold time	t_3	4	600			ns	See Fig. 3
Enable setup time	t_1	10	300			ns	See Fig. 3
Enable hold time	t_5	10	600			ns	See Fig.3
Clock–to–enable time	t_4	10	300			ns	See Fig. 3
Charge pump output current		1		±150		µA	V pin 1=2.0V
Charge pump output leakage current		1			±5	nA	V pin 1=2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Charge pump drive output current		18	1			mA	V pin 18=0.7V
Charge pump amplifier gain				6400			Pin 18 current =100µA
Oscillator temperature stability					2	ppm/°C	
Oscillator stability with supply voltage					2	ppm/V	
Recommended crystal series resistance			10		200	Ω	"Parallel resonant crystal". Figure quoted is under all conditions including startup
Crystal oscillator drive level		2		40		mV p–p	
Crystal oscillator source impedance		2		–400		Ω	Normal spread ±15%
Port and lock sink current		6–9, 11	10			mA	V_{OUT}=0.7V

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= –20°C to +80°C, V_{CC}=+4.5V to +5.5V. Frequency Standard = 4MHz. Pin numbers refer to SP5026 (DP package) These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Port leakage current		6–9			10	µA	V_{OUT}=13.2V
Lock leakage current		11			10	µA	$V_{OUT}=V_{CC}$
Varactor drive amp. disable		10	350			µA	V_{OUT}<0V. Current sourced from device
Charge pump disable		4	350			µA	V_{OUT}<0V. Current sourced from device

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE}=0V

Parameter	Pin SP5026	Pin SP5026S	Value		Units	Conditions
			Min	Max		
Supply voltage	14	12	–0.3	6	V	
Prescaler inputs	15, 16	13, 14		2.5	Vp–p	
Output ports	6–9	6–9	–0.3	14	V	Port in off state
			–0.3	6	V	Port in on state
Total port output current	6–9	6–9		50	mA	
Prescaler DC offset	15, 16	13, 14	–0.3	V_{CC}+0.3	V	
Loop amplifier DC offset	1, 18	1, 16	–0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	2	–0.3	V_{CC}+0.3	V	
Data bus inputs	4, 5, 10	4, 5, 10	–0.7	V_{CC}+0.3	V	With V_{CC} applied
Storage temperature			–55	+125	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip–to–ambient				78	°C/W	
DP thermal resistance, chip–to–case				24	°C/W	
MP16 thermal resistance, chip–to–ambient				111	°C/W	
MP16 thermal resistance, chip–to–case				41	°C/W	
Power consumption at 5V				275	mW	All ports off

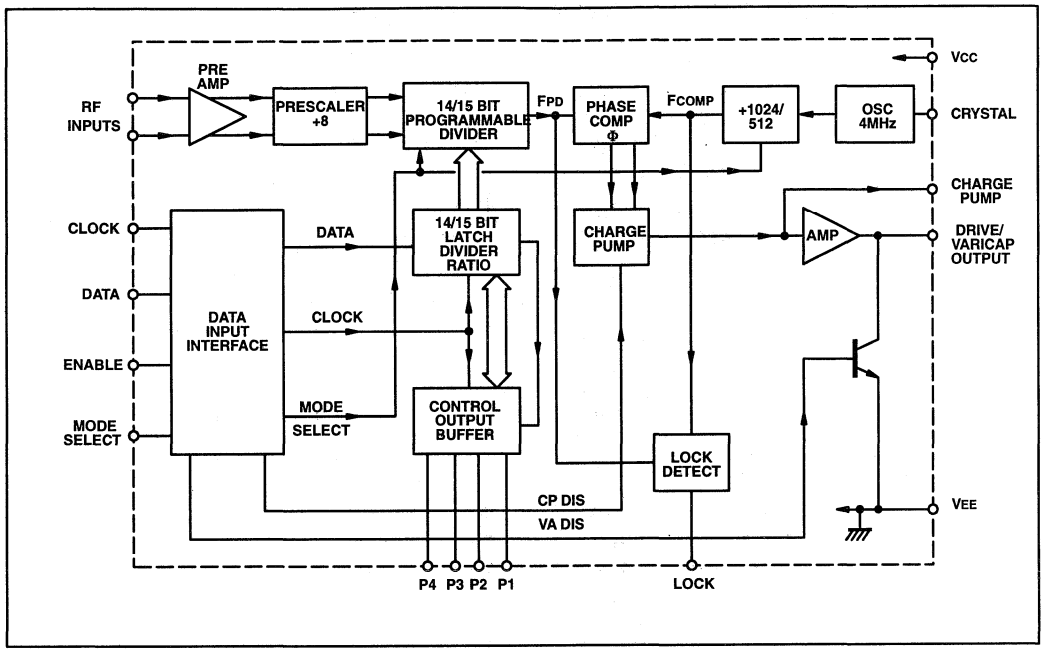


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5026 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard data, clock enable three–wire bus. The data load normally consists of a single word, which contains the frequency and port information and is only transferred to the internal data shift register during an enable high period. The clock is disabled during low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format as displayed in Fig. 3

The frequency is set by loading the programmable divider with the required 14/15–bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator, where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

The F_{COMP} is obtained by dividing the output of an on–chip crystal controlled oscillator. the crystal frequency used is generally 4MHz which gives an F_{COMP} of 3.90625kHz/7.8125kHz. When multiplied back up to the LO this gives a minimum step size of 31.25kHz/62.5kHz, respectively.

The programmable diver is preceded by an input RF preamplifier and high speed low radiation prescaler. The preamplifier is arranged to be self–oscillating, so giving excellent input sensitivity. The input sensitivity and impedance are shown in Figs. 5 and 7, respectively.

The SP5026 contains an improved lock detect circuit which generates a flag when the loop has attained lock. 'Out of lock' is indicated by a high impedance state.

The SP5026 contains four general–purpose open collector outputs, ports P1 – P4, which are capable of sinking at least 10mA. These outputs are set by the remaining four bits within the data word.

PIN COMPATIBILITY

The SP5026 may by used in SP5510 applications which require 3–wire bus as opposed to I^2C bus data format. In SP5510 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig.4.

Appropriate connections to the mode select input (pin 3) must also be made.

With pin 3 'HIGH (mode 1) the SP5026 is function compatible with the Toshiba TD6380; with pin 3 'LOW' (mode 2) it is compatible with the TD6382.

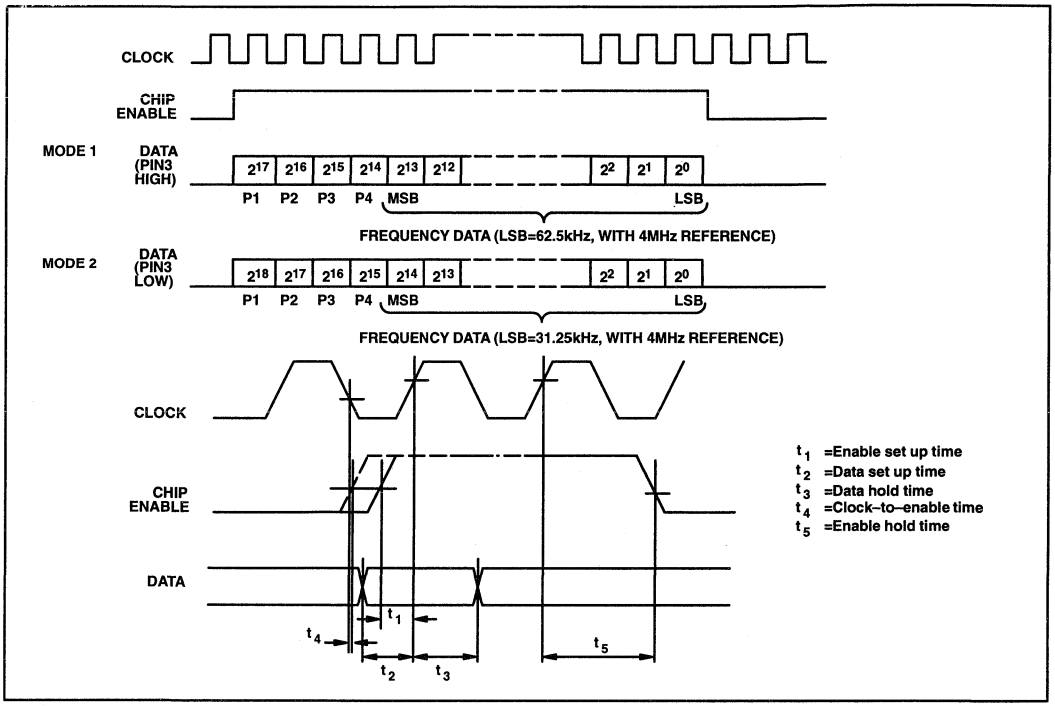


Fig. 3 Data format and timing

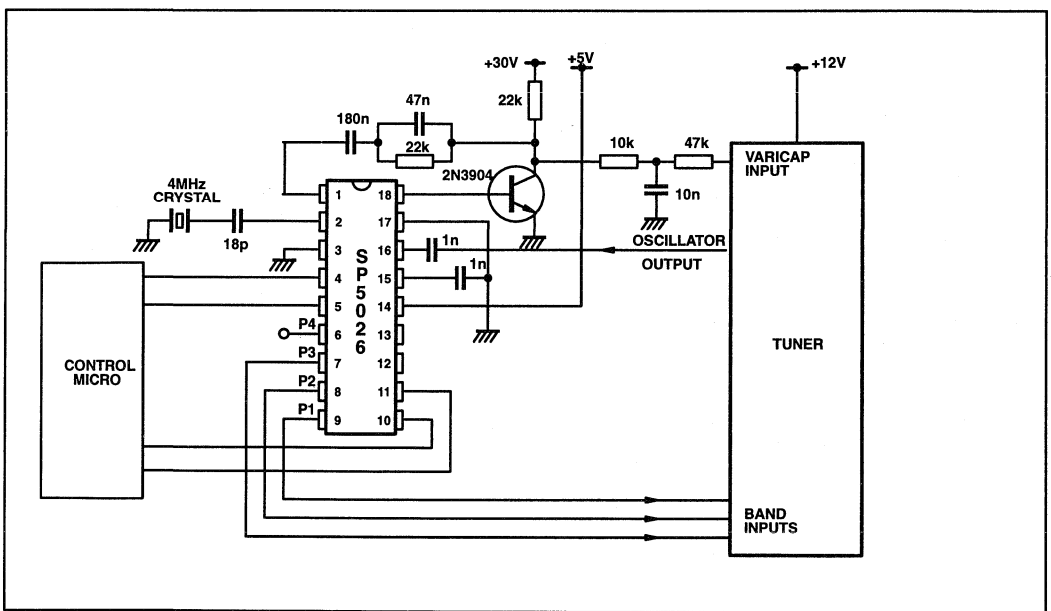


Fig. 4 Typical application (F_{STEP}=31.25kHz)

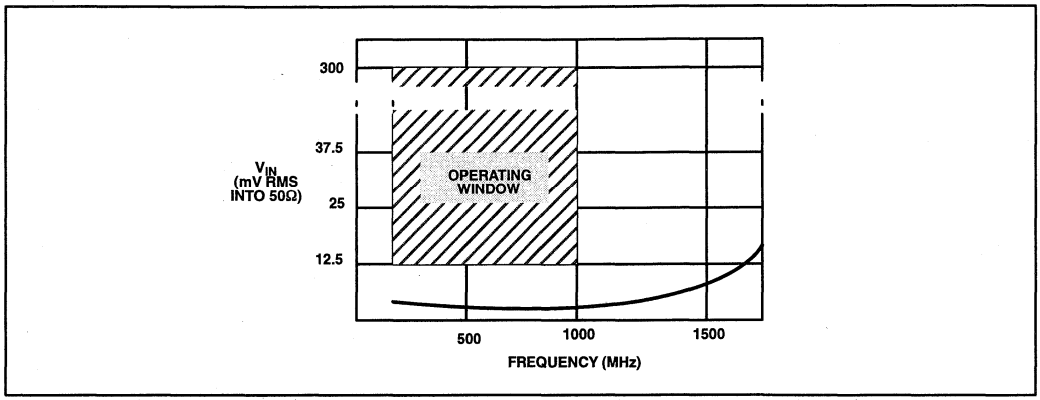


Fig. 5 Typical input sensitivity

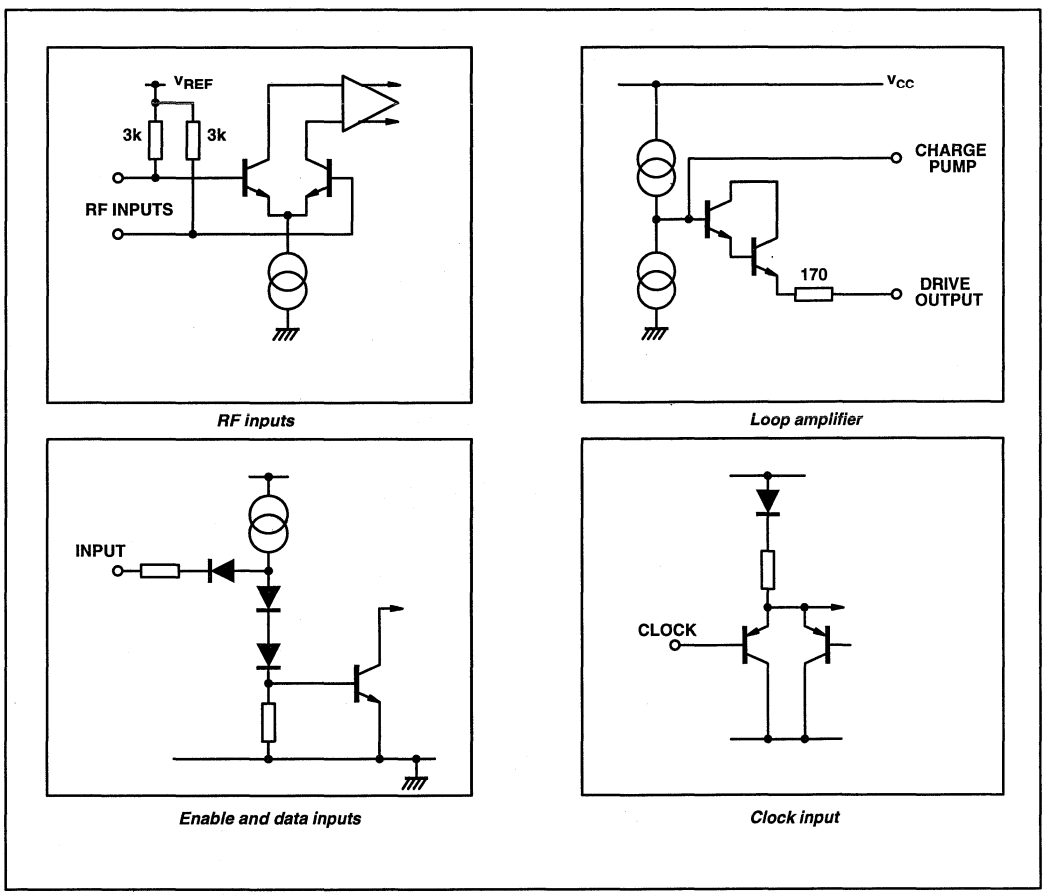


Fig. 6a Input /output interface circuits

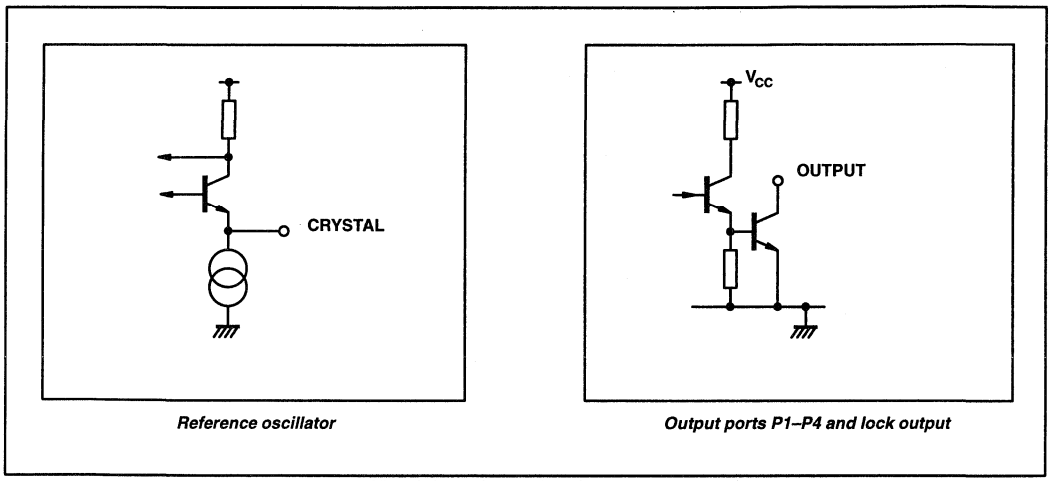


Fig. 6b Input /output interface circuits

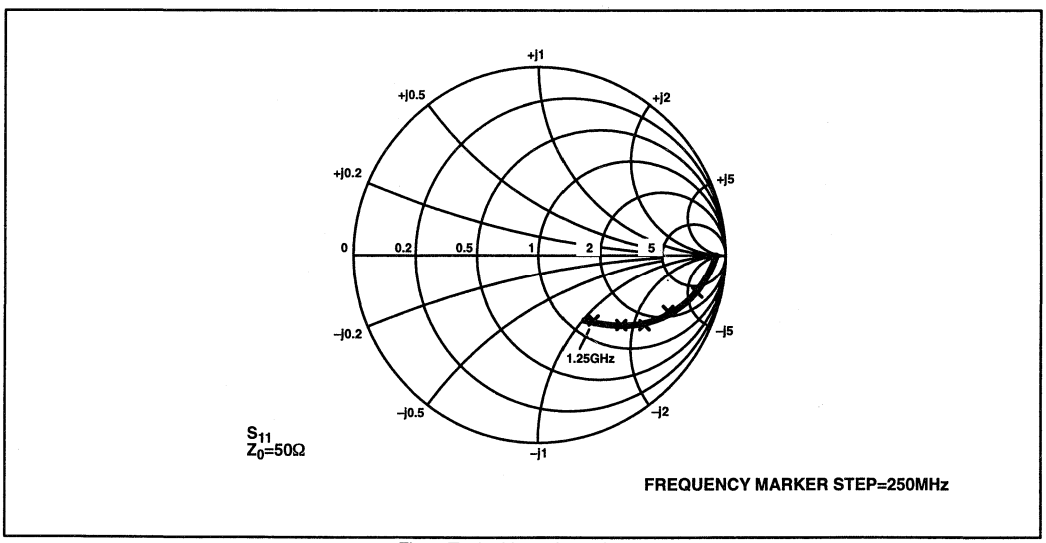


Fig. 7 Typical input impedance

SP5054

2·6 GHz 3-WIRE BUS CONTROLLED SYNTHESISER

The SP5054 is a single-chip frequency synthesiser designed for satellite TV tuning systems. It is a programming variant of the SP5055, allowing the design of one tuner with either I^2C bus or 3-wire bus format, depending on which device is inserted. The SP5054, when used with a satellite varactor tuner, forms a complete phase locked loop tuning system.

The circuit consists of a divide-by-16 prescaler with its own preamplifier and a 14/15-bit programmable divider controlled by a serially-loaded data register. Four independently programmable open-collector outputs are included. The device has four modes of operation, selected by the Mode Select input; these modes are summarised in Table1.

The comparison frequencies are obtained by the division of the output of a 4MHz crystal controlled on-chip oscillator. The phase comparator has a charge pump output with an output amplifier stage around which feedback may be applied. Only one external transistor is required for varactor line driving.

FEATURES

- Complete 2·6GHz Single Chip System
- 62·5kHz, 100kHz and 125kHz Step Size
- Low Power Consumption (325mW Typ.)
- Programming Compatible with Toshiba TD6380, TD6381 and TD6382 *
- Pin Compatible with SP5055 *
- Low Radiation
- Varactor Drive Amplifier Disable
- Charge Pump Disable
- Single Port 18/19 Bit Serial Data Entry
- Four Controllable Outputs
- ESD Protection †

* See notes on pin compatibility
† Normal ESD handling precautions should be observed

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

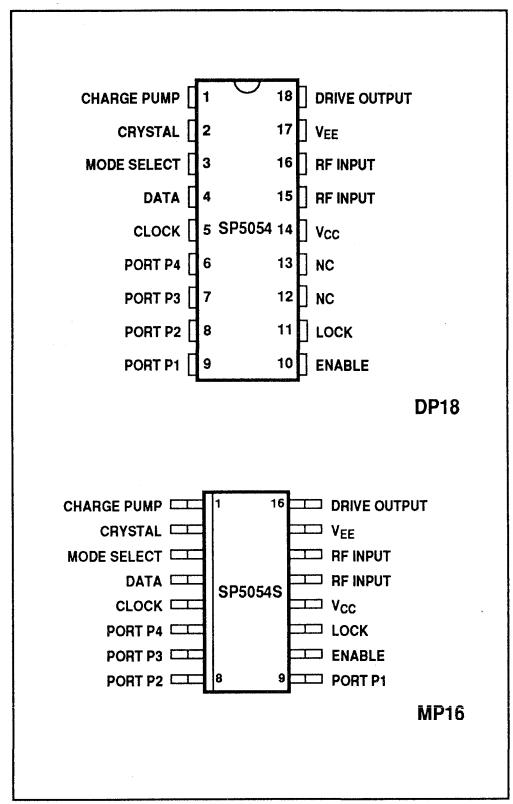


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SP5054 KG DPAS (18-lead plastic package)
SP5054S KG MPAS (16-lead miniature plastic package)

ELECTRICAL CHARACTERISTICS

T_{AMB} = −20°C to +80°C, V_{CC} = +4·5V to +5·5V. Frequency standard = 4MHz. All pin connections refer to DP package. These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	14		65	80	mA	V_{CC} = 5V
Prescaler input voltage	15,16	50		400	mVrms	500MHz to 2·6GHz sinewave
Prescaler input voltage		100		400	mVrms	120MHz and 500MHz, see Fig. 6
Prescaler input impedance	15,16		50		Ω	
Input capacitance			2		pF	
High level input voltage	4,5,10	3		V_{CC}	V	
Low level input voltage	4,5,10	0		0·7	V	
High level input current	4,5,10			1	µA	V_{IN} = 5·5V, V_{CC} = 5·5V
Low level input current	5			5	µA	V_{IN} = 0V, V_{CC} = 5·5V
Low level input current	4,10			−250	µA	V_{IN} = 0V, V_{CC} = 5·5V
High level input current	3			700	µA	V_{IN} = 5·5V, V_{CC} = 5·5V
Low level input current	3			−700	µA	V_{IN} = 0V, V_{CC} = 5·5V
Clock inout hysteresis	5		0·4		V	
Clock rate	5			0·5	MHz	
Data set up time, t_2	4	300			ns	See Fig. 4
Data hold time, t_3	4	600			ns	See Fig. 4
Enable set up time, t_1	10	300			ns	See Fig. 4
Enable hold time, t_5	10	600			ns	See Fig. 4
Clock-to-enable time, t_4	10	300			ns	See Fig. 4
Charge pump output current	1		±150		µA	V pin 1 = 2·0V
Charge pump output leakage current	1			±5	nA	V pin 1 = 2·0V
Drift due to leakage				5	mV/s	At collector of external transistor
Charge pump drive output current	18	1			mA	V pin 18 = 0·7V
Charge pump amplifier gain			6400			I pin 18 = 100µA
Oscillator temperature stability				2	ppm/°C	
Oscillator stability with supply voltage				2	ppm/V	
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 1)
Crystal oscillator drive level	2		40		mV p-p	
Crystal oscillator source impedance	2		−400		Ω	Nominal spread = ±15%
Ports and Lock Output						
Sink current	6-9,11	10			mA	V_{OUT} = 0·7V
Port leakage current	6-9			10	µA	V_{OUT} = 13·2V
Varactor drive amplifier disable	10	−350			µA	V_{IN} < 0V
Charge pump disable	4	−350			µA	V_{IN} < 0V

NOTE 1. The maximum resistance quoted refers to all conditions, including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Parameter	Pin		Value		Units	Conditions
	SP5054	SP5054S	Min.	Max.		
Supply voltage	14	12	−0·3	7	V	
RF input voltage	15,16	13,14		2·5	V p-p	
Port voltage	6-9	6-9	−0·3	14	V	Port in off state
	6-9	6-9	−0·3	6	V	Port in on state
Prescaler DC offset	15,16	13-14	−0·3	V_{CC}+0·3	V	
Loop amplifier DC offset	1,18	1,16	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	2	−0·3	V_{CC}+0·3	V	
Data bus inputs	4,5,10	4,5,10	−0·3	V_{CC}+0·3	V	With V_{CC} applied
Storage temperature			−55	+150	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5·5V				484	mW	

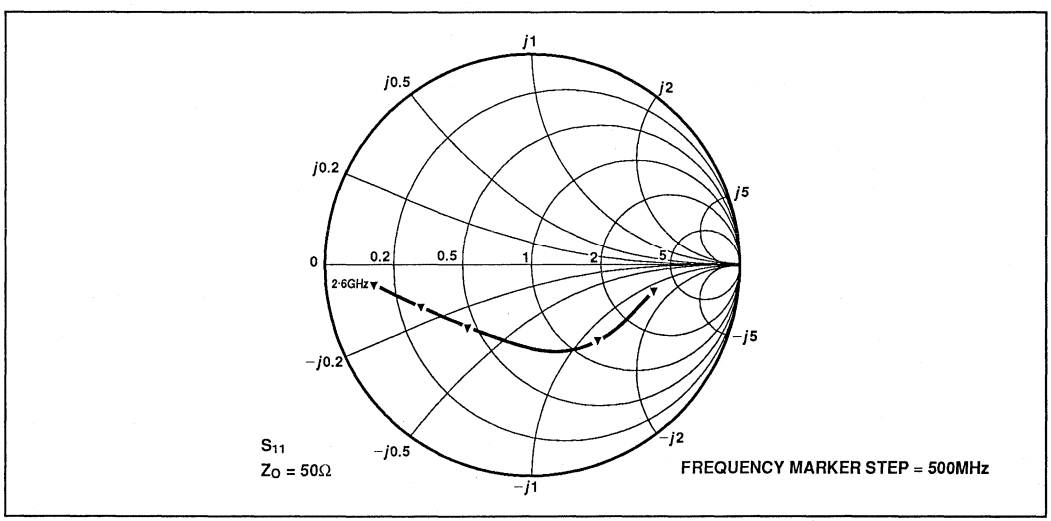


Fig. 2 Typical input impedance

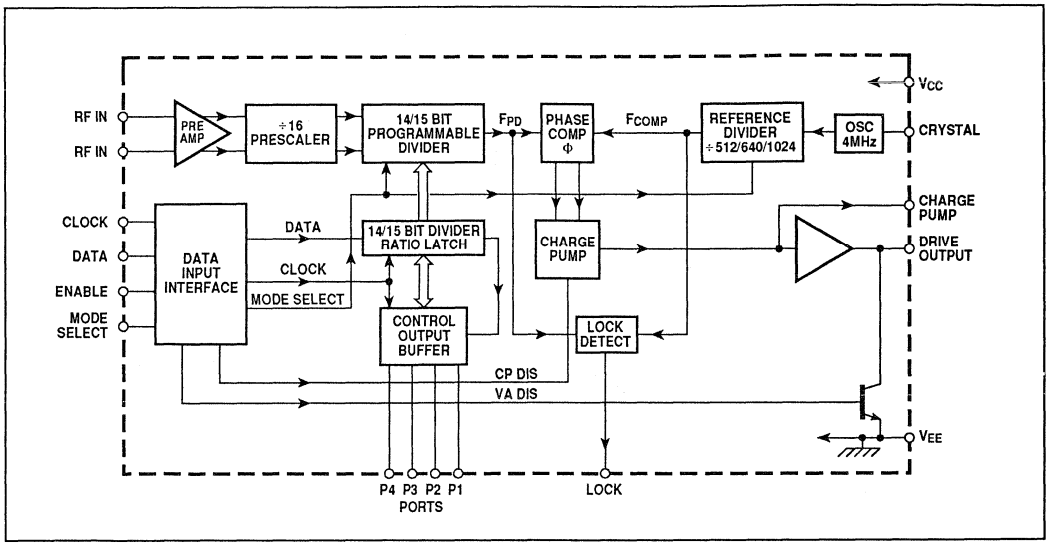


Fig. 3 Block diagram of SP5054

Mode	Mode Select input voltage	Programmable divider bit length	Reference divider ratio	Frequency step size (kHz) *	Maximum operating frequency (GHz) *
3	0·925V_{CC} to V_{CC}	14	512	125	2·0479
2	0·675V_{CC} to 0·825V_{CC}	15	512	125	2·5
1	Open circuit	15	1024	62·5	2·0479
0	0V to 0·325 V_{CC}	15	640	100	2·5

*Table 1 SP5054 modes of operation. * Frequencies stated apply when using a 4MHz crystal.*

FUNCTIONAL DESCRIPTION

The SP5054 contains all the elements necessary, with the exception of reference crystal, loop filter and external high voltage transistor, to control a voltage controlled local oscillator, so forming a PLL frequency synthesised source.

The system is controlled by a microprocessor via a standard Data, Clock and Enable three-wire data bus.

The data load normally consists of a single word, which contains the frequency and port information, and is only transferred to the internal data shift register during an enable high period.

The clock input is disabled during enable low periods. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the Enable, so giving improved fine tune facility for digital AFC etc.

The data sequence and timing follows the format shown in Fig. 4.

The frequency is set by loading the programmable divider with the required 14/15 bit divisor word. The output of this divider, F_{PD}, is fed to the phase comparator where it is compared in phase and frequency domain to the internally generated comparison frequency, F_{COMP}.

F_{COMP} is obtained by dividing the output of an on-chip crystal controlled oscillator. The crystal frequency used is generally 4MHz, which gives an F_{COMP} of 3·90625/6·25/7·8125kHz and, when multiplied back up to the synthesised LO, gives a minimum step size of 62·5/100/125kHz, respectively.

The programmable divider is preceded by an input RF preamplifier and high speed, low radiation prescaler. The preamplifier is arranged to be self oscillating, so giving excellent input sensitivity.

The SP5054 contains an improved lock detect circuit which generates a flag when the loop has attained lock. 'In lock' is indicated by high impedance state.

The SP5054 contains 4 general purpose open collector outputs, ports P1-P4, which are capable of sinking at least 10mA. These outputs are set by the remaining four bits within the normal data word.

NOTES ON PIN COMPATIBILITY

The SP5054 may be used in SP5055 applications which require 3-wire bus as opposed to I^2C bus data format. In SP5055 applications where the reference crystal is grounded to pin 3, a small modification is required to ground the crystal as shown in Fig. 5.

Appropriate connections must also be made to the Mode Select input (see Table 1). In Mode 3, The SP5054 is programming compatible with the Toshiba TD6380, in Modes 0 and 2 with the TD6381 and in Mode 1 with the TD6382.

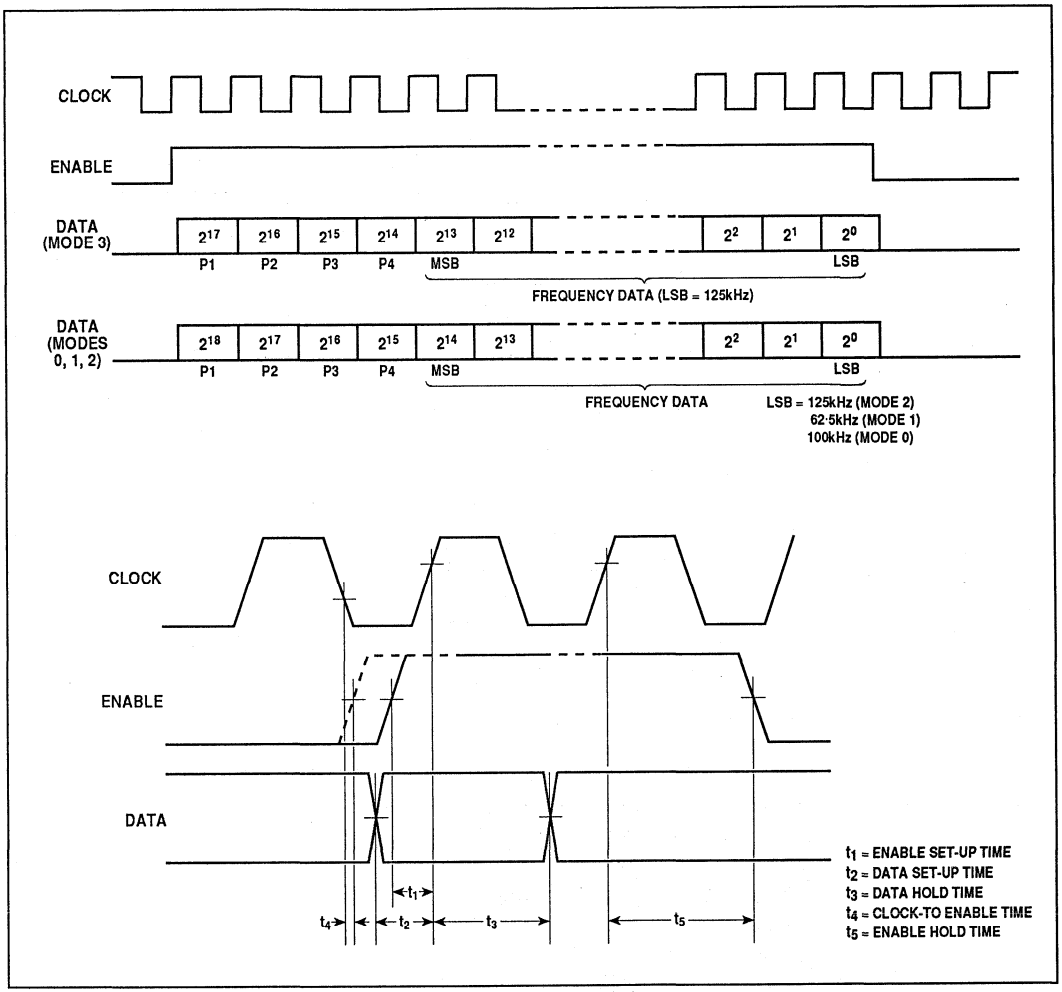


Fig. 4 Data format and timing

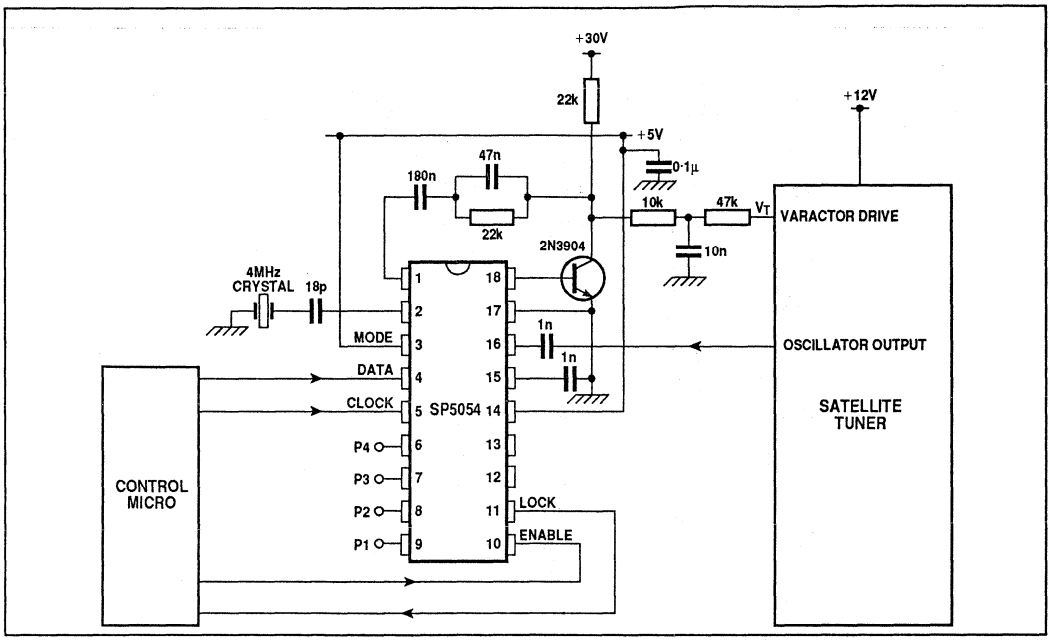


Fig. 5 Typical application (f_{STEP} = 125kHz)

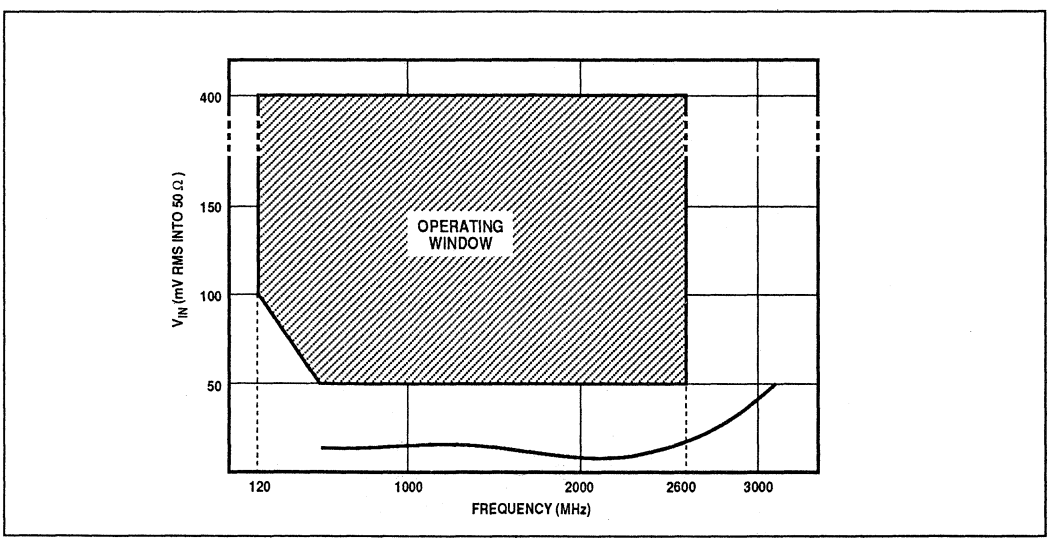


Fig. 6 Typical input sensitivity

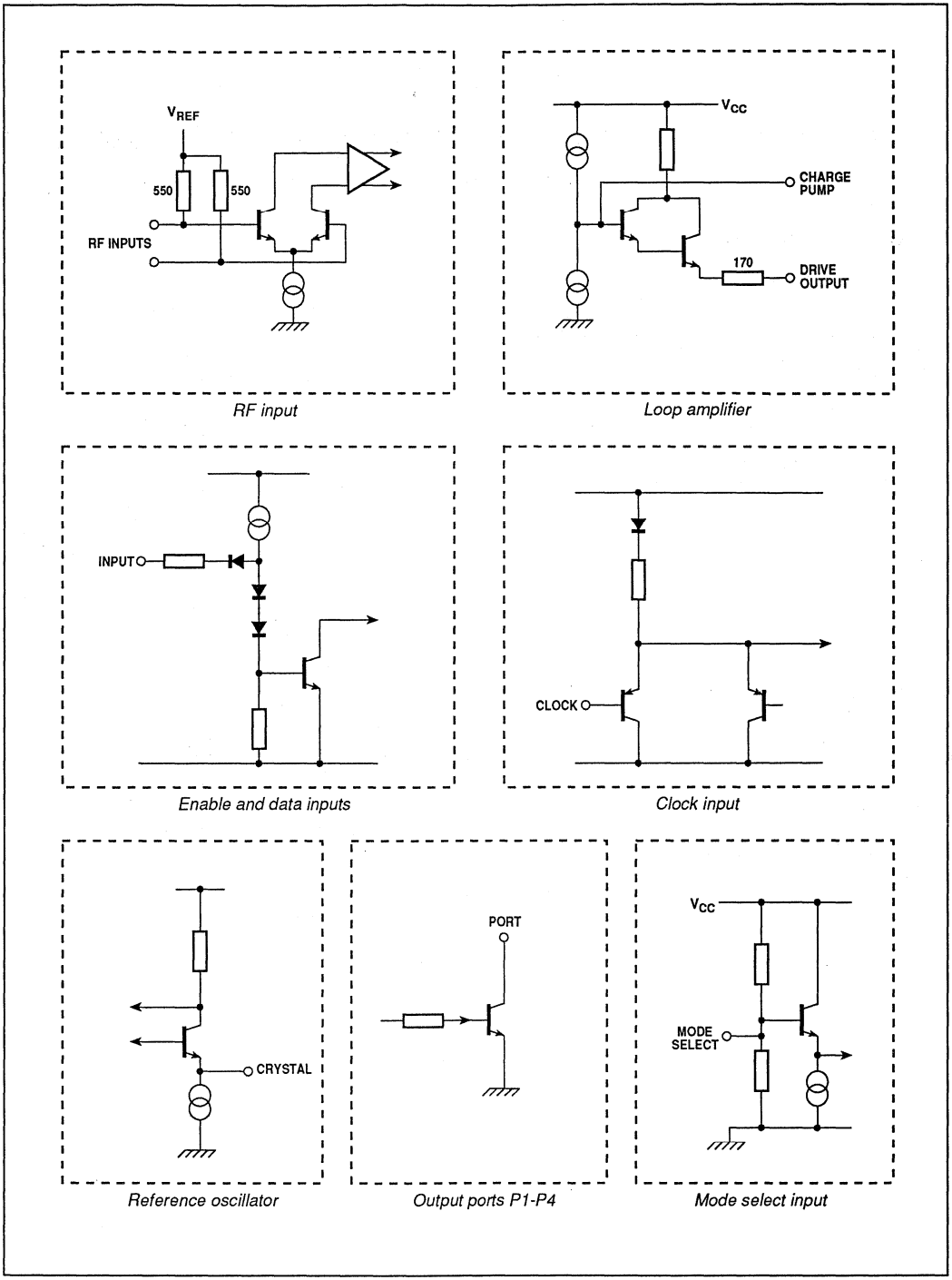


Fig. 7 SP5054 input/output interface circuits

SP5055

2.6 GHz BI-DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

(Supersedes version in September 1991 Consumer IC Handbook and March 1992 issue)

The SP5055 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 4 addressable current limited outputs and 4 addressable Bi-Directional open collector ports one of which is a 3 Bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

The device is available in two variants: the SP5055 in 18-lead plastic DIL (DP18) and the SP5055S in 16-lead miniature plastic DIL (MP16). See Features below for functional differences between the devices.

FEATURES

- Complete 2.6GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 65mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-Directional (SP5055)
- 6 Controllable Outputs, 4 Bi-Directional (SP5055S)
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- Full ESD Protection *

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

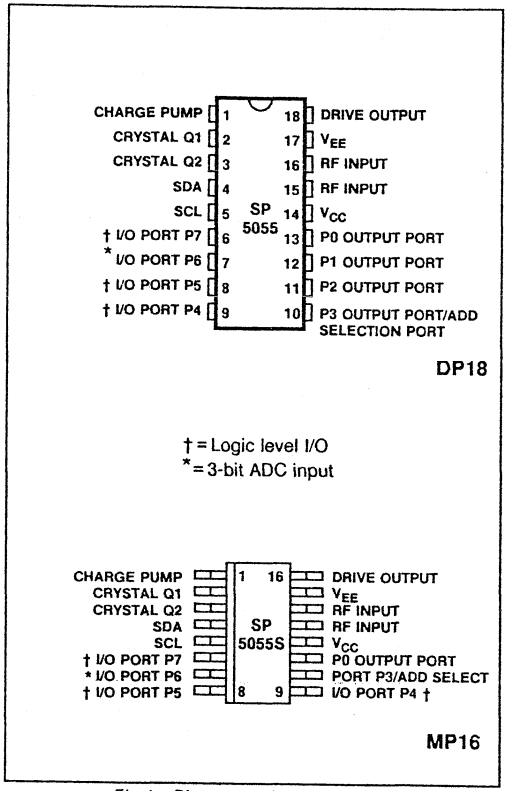


Fig.1 Pin connections - top view

ORDERING INFORMATION

SP5055 DP - (18 lead Plastic package)
SP5055S MP - (16 lead Miniature Plastic package)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = -20°C to 80°C, V_{CC} = +4.7V TO 5.3V

All pin connections refer to DP package.

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		65	80	mA	V_{CC} = 5V
Prescaler Input Voltage	15,16	50		300	mV_{RMS}	500MHz to 1.8GHz Sinewave
Prescaler Input Voltage	15,16	100		300	mV_{RMS}	120MHz & 2.6GHz, see Fig. 5
Prescaler Input Impedance Input Capacitance	15,16		50 2		Ω pF	
SDA,SCL Input High Voltage Input Low Voltage Input High Current Input Low Current Leakage Current	4,5 4,5 4,5 4,5 4,5	3 0		5.5 1.5 10 -10 10	V V µA µA µA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output Voltage	4			0.4	V	I_{sink} = 3mA
Charge Pump Current Low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge Pump Current High	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge Pump Output Leakage Current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge Pump Drive Output Current	18	500			µA	$V_{pin\ 18}$ = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended Crystal Series Resistance		10		200	Ω	
Crystal Oscillator Drive Level			40		mVp-p	
Crystal Oscillator Source Impedance	2		-400		Ω	Nominal Spread ± 15%
Output Ports						
P0-P3 Sink Current*	13-10	0.7	1	1.5	mA	V_{OUT} = 12V
P0-P3 Leakage Current*	13-10			10	µA	V_{OUT} = 13.2V
P4-P7 Sink Current	9-6	10			mA	V_{OUT} = 0.7V
P4-P7 Leakage Current	9-6			10	µA	V_{OUT} = 13.2V
Input Ports						
P3 Input Current High	10			+10	µA	V_{pin10} = 13.2V
P3 Input Current Low	10			-10	µA	V_{pin10} = 0V
P4,P5,P7 Input Voltage Low	9,8,6			0.8	V	
P4,P5,P7 Input Voltage High	9,8,6	2.7			V	
P6 Input Current High	7			+10	µA	See Table 3 for ADC Levels
P6 Input Current Low	7			-10	µA	

* Ports P1-P2 not present on the SP5055S.

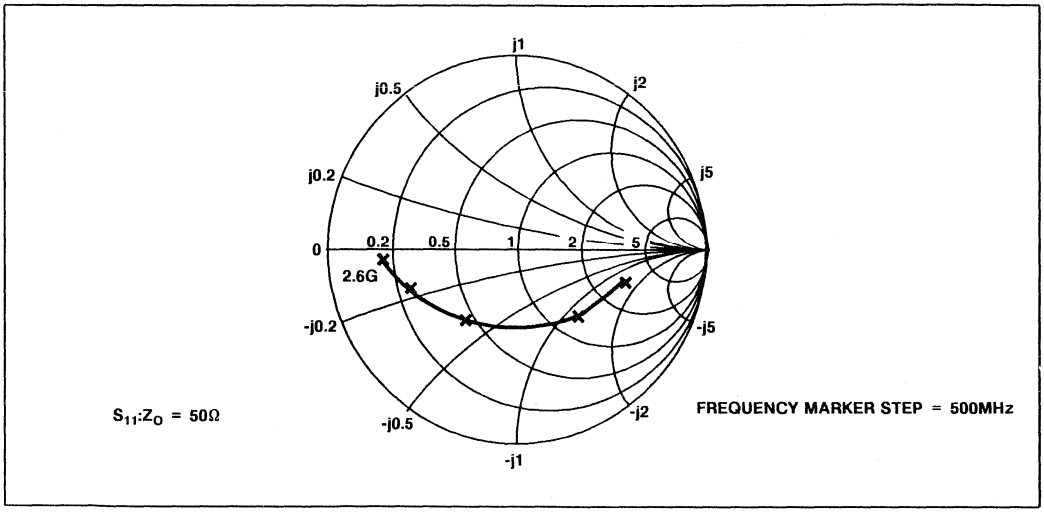


Fig.7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin SP5055	Pin SP5055S	Value Min	Value Max	Units	Conditions
Supply voltage	14	12	-0.3	7	V	
RF input voltage	15, 16	13, 14		2.5	Vp-p	
Port voltage	6 - 13	6 - 11	-0.3	14	V	Port in off state
	6 - 9	6 - 9	-0.3	6	V	Port in on state
	10-13	10, 11	-0.3	14	V	Port in on state
Total port output current	6-13	6-11		50	mA	
RF input DC offset	15, 16	13, 14	-0.3	V_{CC} + 0.3	V	
Charge pump DC offset	1	1	-0.3	V_{CC} + 0.3	V	
Drive DC offset	18	16	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	2	2	-0.3	V_{CC} + 0.3	V	
SDA, SCL input voltage	4, 5	4, 5	-0.3	V_{CC} + 0.3	V	With V_{CC} applied
			-0.3	5.5	V	V_{CC} not applied
Storage temperature			-55	+ 125	°C	
Junction temperature				+ 150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5.5V				440	mW	All ports off

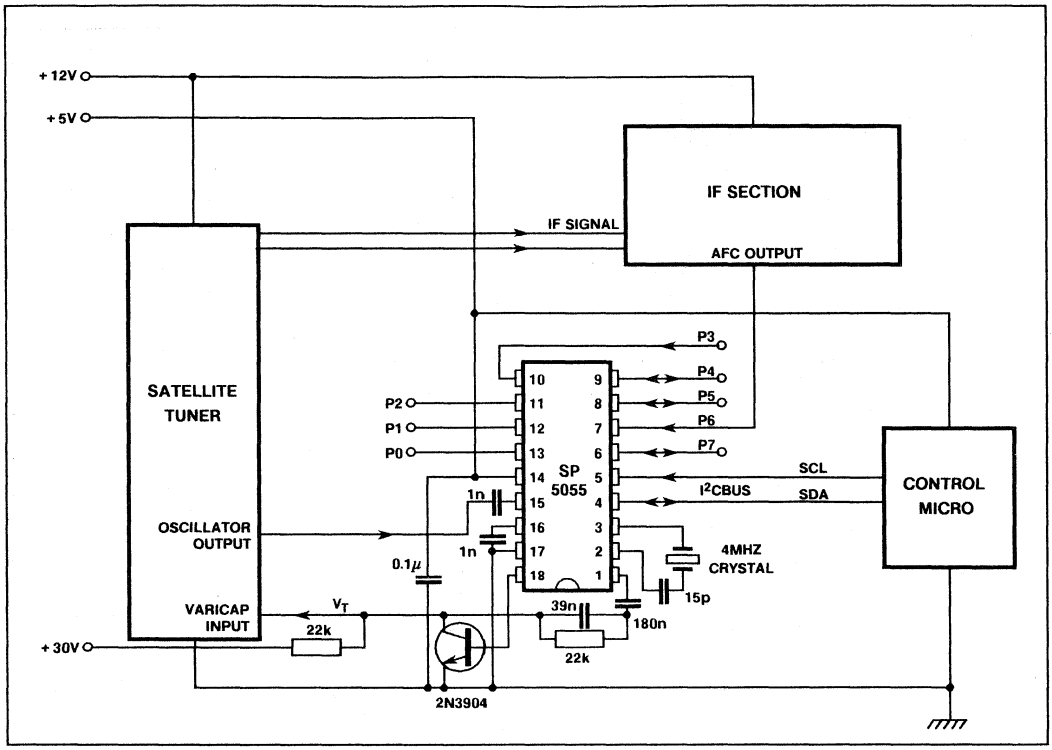


Fig.4 Typical SP5055 application

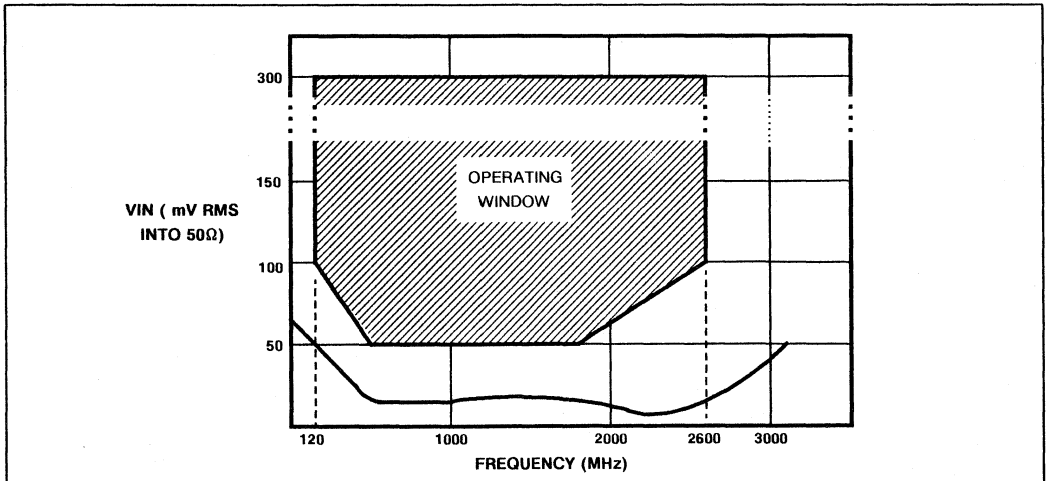


Fig.5 Typical input sensitivity

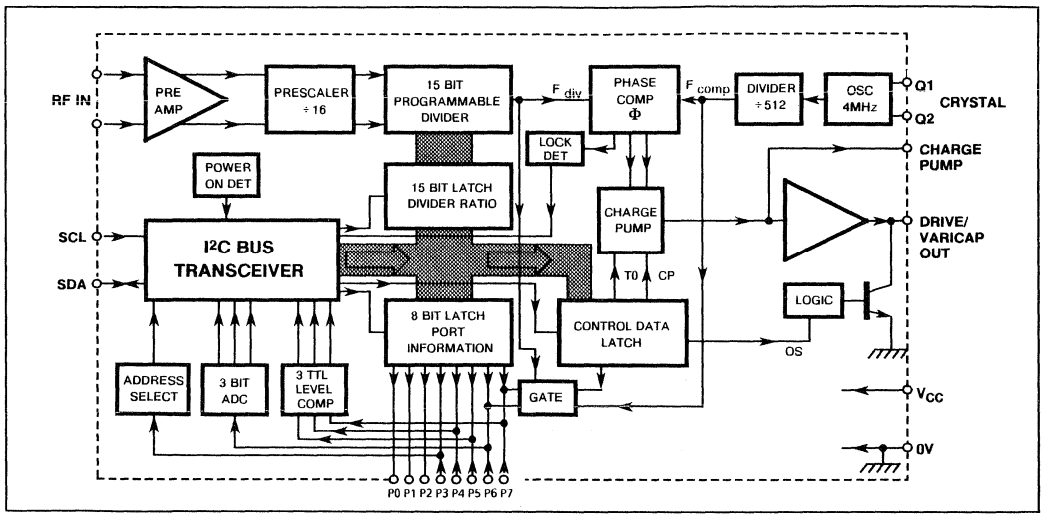


Fig.2 Block diagram of SP5055. (Ports P1-P2 not available on SP5055S)

FUNCTIONAL DESCRIPTION

The SP5055 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The last bit of the address byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5055 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5055 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode bytes 2 + 3 select the synthesised frequency while bytes 4 + 5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first bit of the next Byte determines whether that Byte is interpreted as byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (e.g. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-board 4MHz crystal controlled oscillator.

Note - the comparison frequency is 7.8125KHz when a 4MHz reference is used.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$ allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{comp} to P6 and F_{div} to P7.

Byte 5 programs the output ports P0 to P7; a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical Application is shown in Fig. 4. All input/ output interface circuits are shown in Fig. 6.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	**BYTE 4**
IO PORT CONTROL BITS	P7	P6	P5	P4	P3	P2*	P1*	P0	A	**BYTE 5**

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	**BYTE 1**
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	**BYTE 2**

Table 2 Read data format

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0 : control output states
POR : Power On Reset indicator
FL : Phase Lock detect Flag
I2, I1, I0 : Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0 : 5 Level ADC data from P6 (see Table 3)

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45\ V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3\ V_{CC}$
0	0	0	0 to $0.15\ V_{CC}$

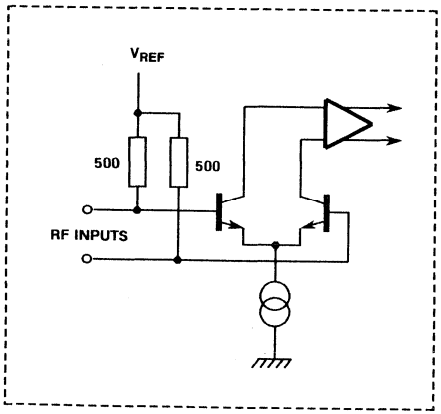
Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 - 0.2\ V_{CC}$
0	1	ALWAYS VALID
1	0	$0.3 - 0.7\ V_{CC}$
1	1	$0.8\ V_{CC}$ - 13.2V

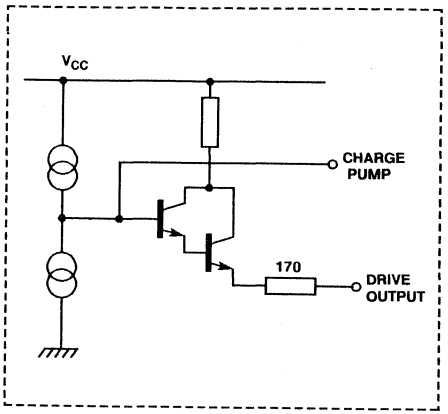
Table 4 Address selection

NOTE: * Don't care condition on SP5055S

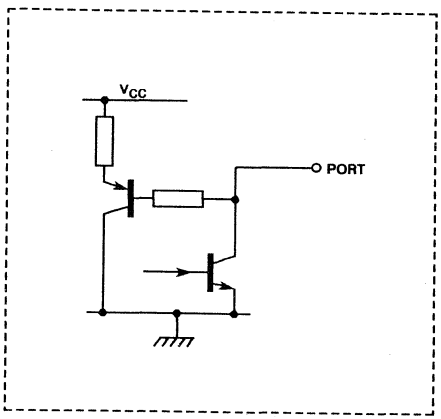
Fig. 3 Data Formats



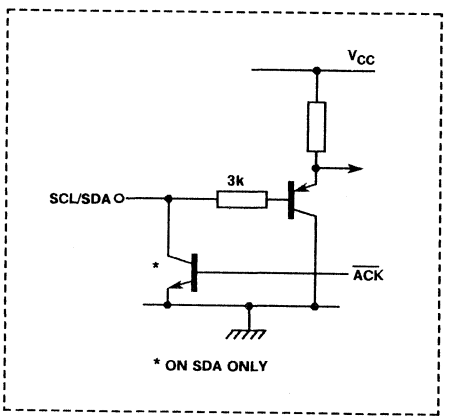
RF input



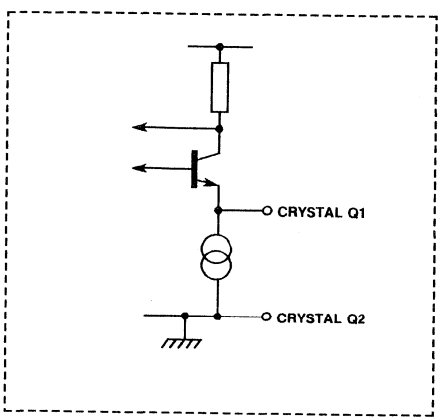
Loop amplifier



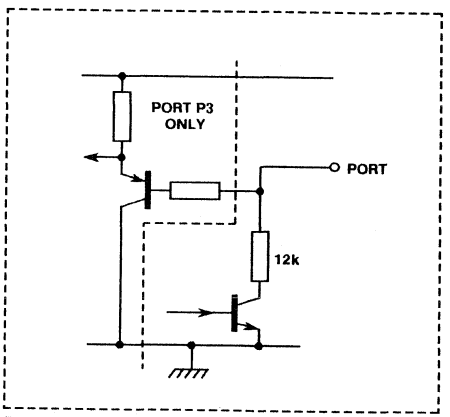
Ports P7 - P4



SCL and SDA input



Reference oscillator



Ports P0-P3 (SP5055), P0 and P3 only on SP5055S

Fig.6 SP5055 input/output interface circuits

SP5056

2.6 GHz BI-DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

(Supersedes version in September 1991 Consumer IC Handbook)

The SP5056 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 3 addressable current limited outputs and 4 addressable Bi-Directional open-collector ports one of which is a 3-Bit ADC. The information on these ports can be read via the I²C BUS. The device has 4 programmable I²C BUS addresses, which enables 2 or more synthesisers to be used in a system.

The device is available in two variants: the SP5056 in 18-lead plastic DIL (DP18) and the SP5056S in 16-lead miniature plastic DIL (MP16). See Features below for functional differences between the devices.

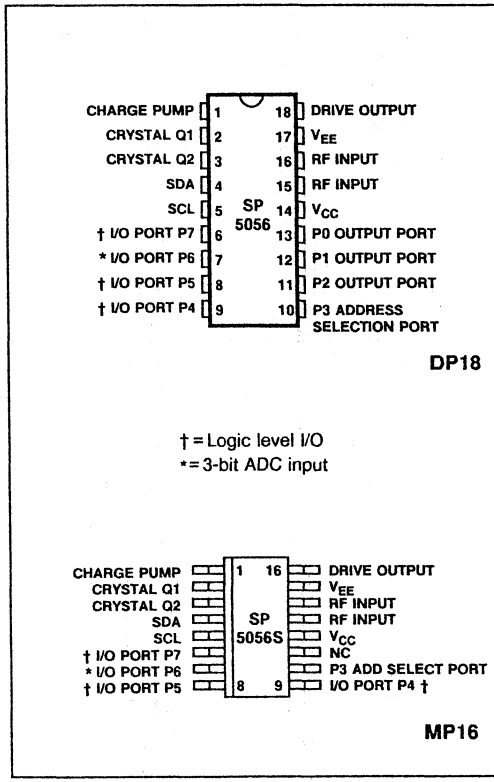


Fig.1 Pin connections - top view

FEATURES

- Complete 2.6GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 65mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 7 Controllable Outputs, 4 Bi-Directional (SP5056)
- 4 Bi-Directional Controllable Outputs (SP5056S)
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- Full ESD Protection *

* Normal ESD handling procedures should be observed.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ORDERING INFORMATION

SP5056 /KG/DPAS
SP5056S /KG/MPAS

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

T_{amb} = -20°C to 80°C, V_{CC} = +4.5V TO 5.5V

All pin connections refer to DP package.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		65	80	mA	V_{CC} = 5V
Prescaler Input Voltage	15,16	50		300	mV_{RMS}	500MHz to 1.8GHz Sinewave
Prescaler Input Voltage	15,16	100		300	mV_{RMS}	120MHz & 2.6GHz, see Fig. 5
Prescaler Input Impedance Input Capacitance	15,16		50 2		Ω pF	
SDA,SCL Input High Voltage Input Low Voltage Input High Current Input Low Current Leakage Current	4,5 4,5 4,5 4,5 4,5	3 0		5.5 1.5 10 -10 10	V V µA µA µA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output Voltage	4			0.4	V	I_{sink} = 3mA
Charge Pump Current Low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge Pump Current High	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge Pump Output Leakage Current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge Pump Drive Output Current	18	500			µA	$V_{pin\ 18}$ = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended Crystal Series Resistance		10		200	Ω	
Crystal Oscillator Drive Level			40		mVp-p	
Crystal Oscillator Source Impedance	2		-400		Ω	Nominal Spread ± 15%
Output Ports						
P0-P2 Sink Current*	11-13	0.7	1	1.5	mA	V_{OUT} = 12V
P0-P2 Leakage Current*	11-13			10	µA	V_{OUT} = 13.2V
P4-P7 Sink Current	9-6	10			mA	V_{OUT} = 0.7V
P4-P7 Leakage Current	9-6			10	µA	V_{OUT} = 13.2V
Input Ports						
P3 Input Current High	10			1	mA	V_{pin10} = V_{CC}
P3 Input Current Low	10			0.5	mA	V_{pin10} = 0V
P4,P5,P7 Input Voltage Low	9,8,6			0.8	V	
P4,P5,P7 Input Voltage High	9,8,6	2.7			V	
P6 Input Current High	7			+10	µA	See Table 3 for ADC Levels
P6 Input Current Low	7			-10	µA	

* Ports P0-P2 not present on the SP5056S.

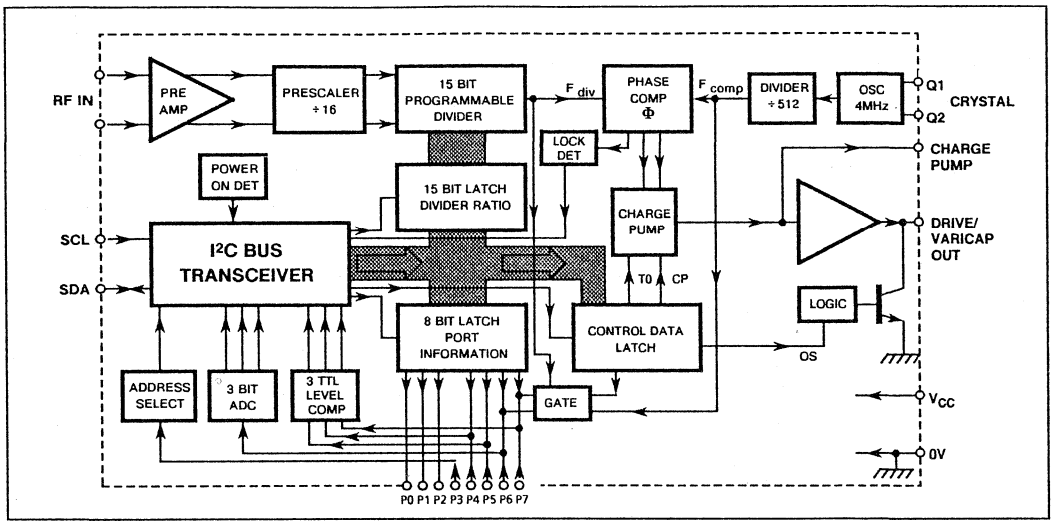


Fig.2 Block diagram of SP5056. (Ports P0-P2 not available on SP5056S)

FUNCTIONAL DESCRIPTION

The SP5056 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The last bit of the address byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5056 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5056 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode bytes 2+3 select the synthesised frequency while bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first bit of the next Byte determines whether that Byte is interpreted as byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid byte (i.e. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-board 4MHz crystal controlled oscillator.

Note - the comparison frequency is 7.8125kHz when a 4MHz reference is used.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$ allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{comp} to P6 and F_{div} to P7.

Byte 5 programs the output ports P0 to P2 and P4 to P7, a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical Application is shown in Fig. 4. All input/ output interface circuits are shown in Fig. 6.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	**BYTE 1**
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**BYTE 2**
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**BYTE 3**
CHARGE PUMP AND TEST BITS	1	CP	T1	T0	1	1	1	OS	A	**BYTE 4**
IO PORT CONTROL BITS	P7	P6	P5	P4	X	P2*	P1*	P0*	A	**BYTE 5**

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	**BYTE 1**
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	**BYTE 2**

Table 2 Read data format

A : Acknowledge Bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0* : control output states
POR : Power On Reset indicator
FL : Phase Lock detect Flag
I2, I1, I0 : Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0 : 5 Level ADC data from P6 (see Table 3)

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45\ V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3\ V_{CC}$
0	0	0	0 to $0.15\ V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 - 0.1\ V_{CC}$
0	1	OPEN CIRCUIT
1	0	$0.4 - 0.6\ V_{CC}$†
1	1	$0.9\ V_{CC} - V_{CC}$

Table 4 Address selection

NOTES: † Programmed by connecting a 15kΩ resistor between Address Select Port P3 and V_{CC}
* Don't care condition on SP5056S.

Fig. 3 Data Formats

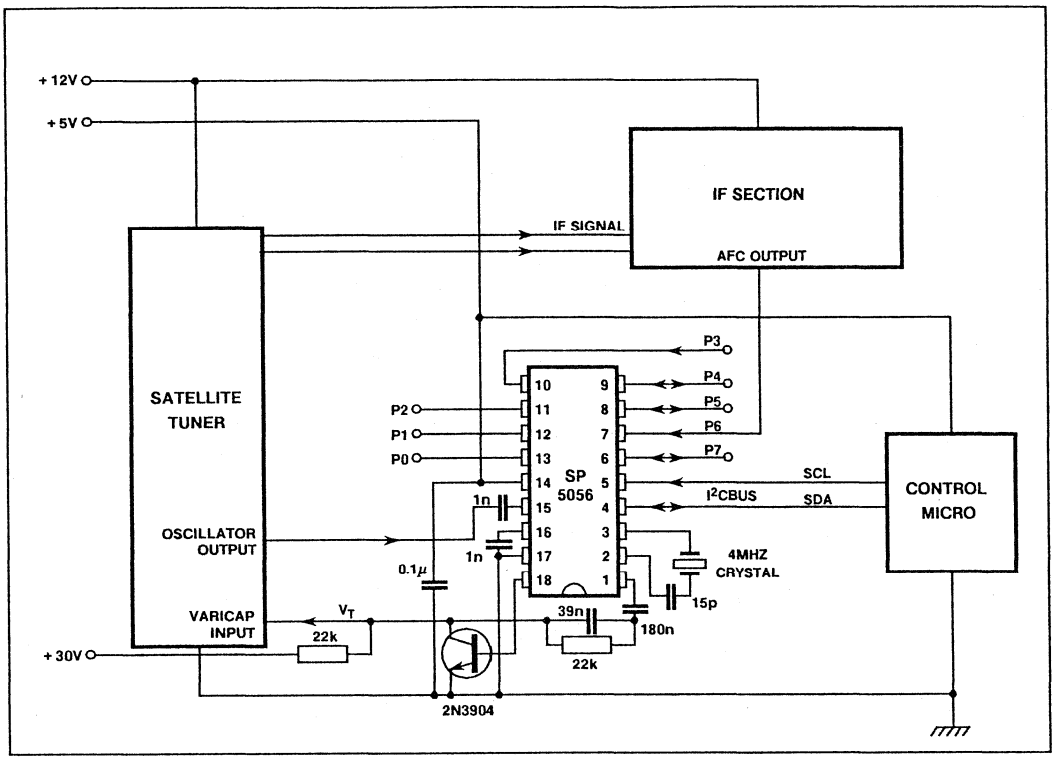


Fig.4 Typical SP5056 application

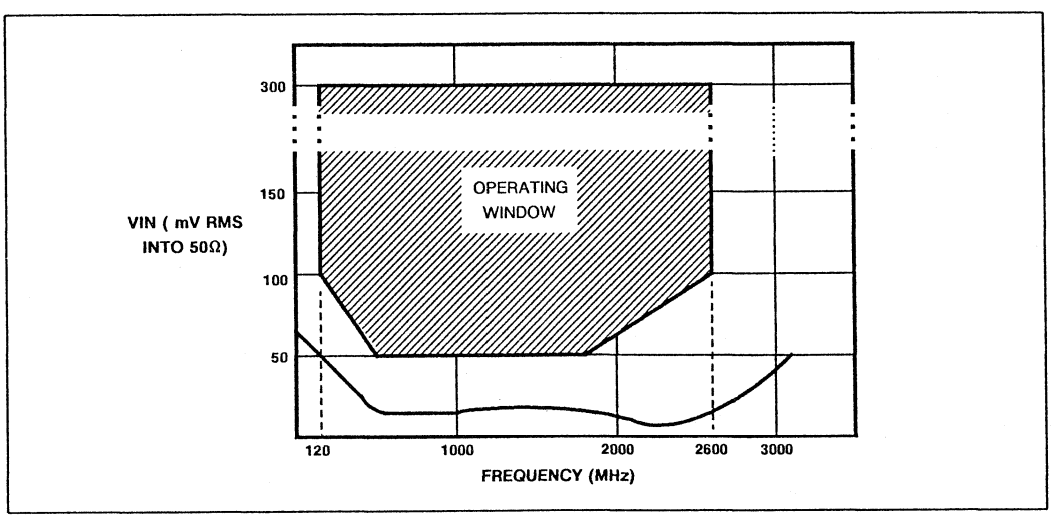


Fig.5 Typical input sensitivity

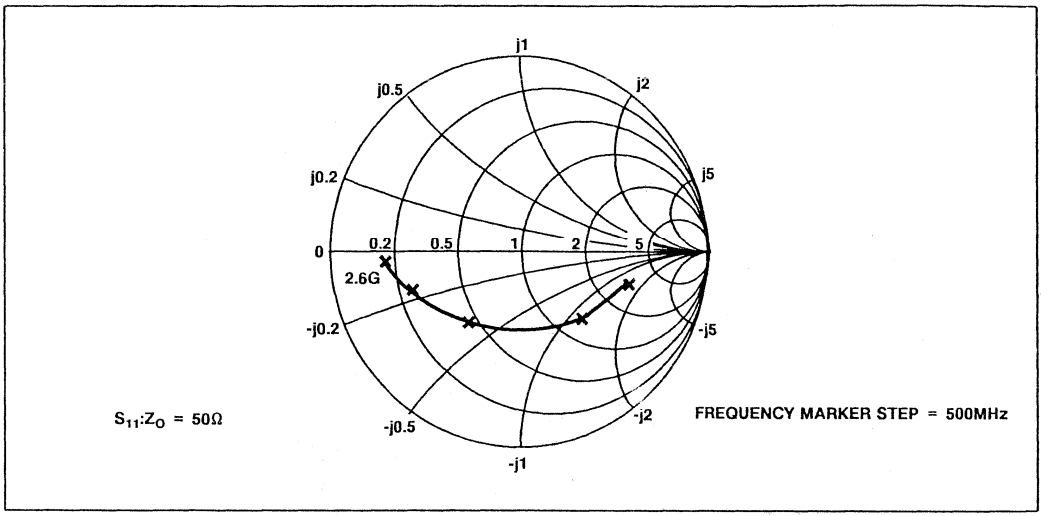
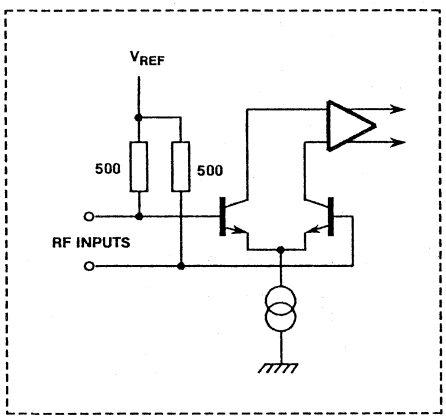


Fig.7 Typical input impedance

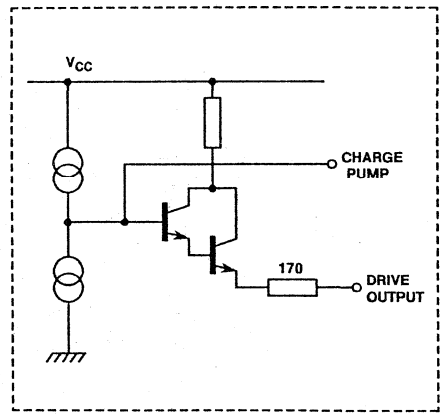
ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

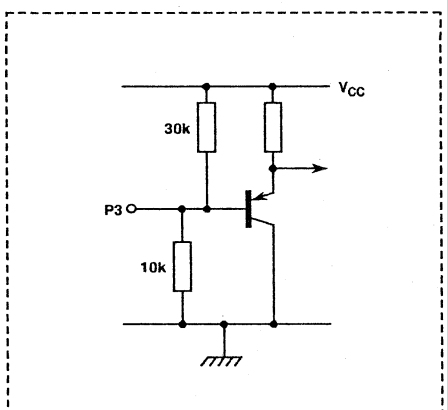
Parameter	Pin SP5056	Pin SP5056S	Value Min	Value Max	Units	Conditions
Supply voltage	14	12	-0.3	7	V	
RF input voltage	15, 16	13, 14		2.5	Vp-p	
Port voltage	6-9,11-13	6 - 9	-0.3	14	V	Port in off state
	6 - 9	6 - 9	-0.3	6	V	Port in on state
	11-13	-	-0.3	14	V	Port in on state
	10	10	-0.3	V_{CC} + 0.3	V	
Total port output current	6-9, 11-13	6-9		50	mA	
RF input DC offset	15, 16	13, 14	-0.3	V_{CC} + 0.3	V	
Charge pump DC offset	1	1	-0.3	V_{CC} + 0.3	V	
Drive DC offset	18	16	-0.3	V_{CC} + 0.3	V	
Crystal oscillator DC offset	2	2	-0.3	V_{CC} + 0.3	V	
SDA, SCL input voltage	4, 5	4, 5	-0.3	V_{CC} + 0.3	V	With V_{CC} applied
			-0.3	5.5	V	V_{CC} not applied
Storage temperature			-55	+125	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5.5V				440	mW	All ports off



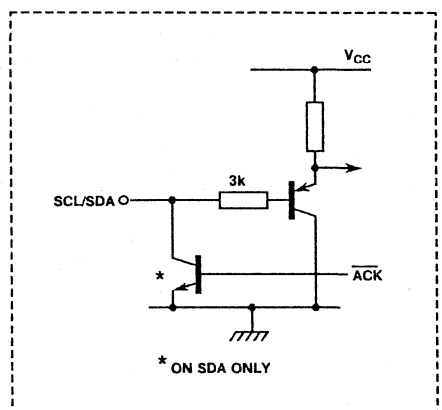
RF input



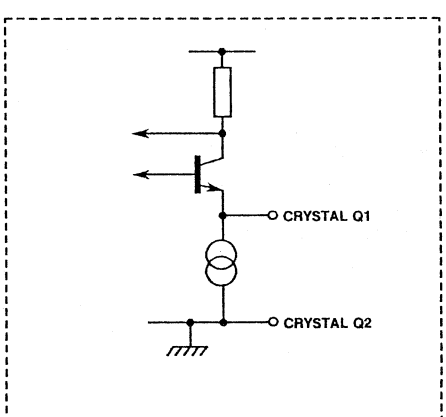
Loop amplifier



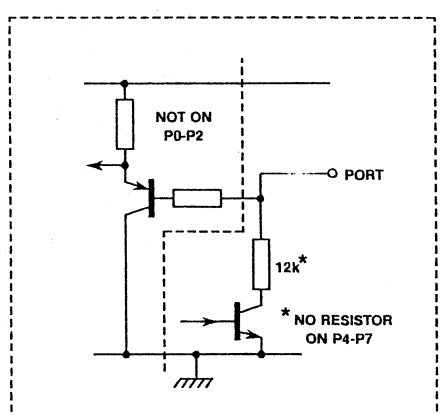
Address programming input



SCL and SDA input



Reference oscillator



Ports P0-P2 (SP5056 only) and P4-P7

Fig.6 SP5056 input/output interface circuits

SP5058

2.6GHz 3–WIRE BUS SYNTHESISER

(Supersedes December 1992 Edition DS3514 1.2)

The SP5058 is a single chip frequency synthesiser designed for tuning systems up to 2.6GHz requiring high loop comparison frequencies.

The circuit consists of a divide by 4 prescaler with its own preamplifier and a 14 bit MN+A programmable counter which utilises an on–board 16/17 divider. Comparison frequencies are obtained either from a crystal controlled on–chip oscillator or from an external source. Four reference oscillator divider ratios are available, programmed by 2 bits in the data word.

The phase comparator has a charge pump output with an amplifier stage around which feedback may be applied. Only one external transistor is required for varactor line driving.

The device also contains a disable input for asynchronously switching the charge pump output to high impedance state. A software programmable varactor line disable is included to aid the set up of oscillators and tuners. Two independently programmable open collector outputs are included which may be used for band selection.

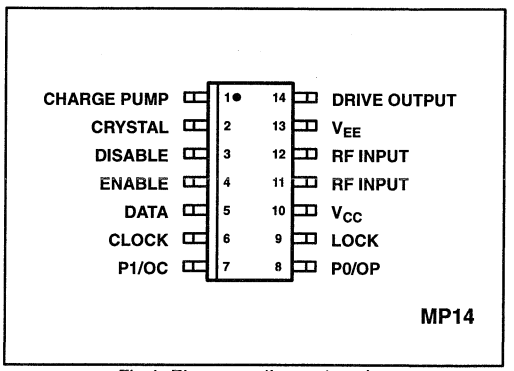


Fig 1. Pin connections – top view

FEATURES

- Complete 2.6GHz Single Chip System
- User Defined Step Size
- Improved Phase Noise
- Low Power Consumption
- Phase Lock Detector
- Varactor Drive Amplifier Disable
- Asynchronous Charge Pump Disable
- Low Radiation
- 20 Bit Serial Data Entry
- Two Controllable High Current Outputs

APPLICATIONS

- Double Conversion Tuners
- Satellite TV
- Cable TV Systems

ORDERING INFORMATION

SP5058F/KG/MPAS – (14 lead Miniature Plastic Package)

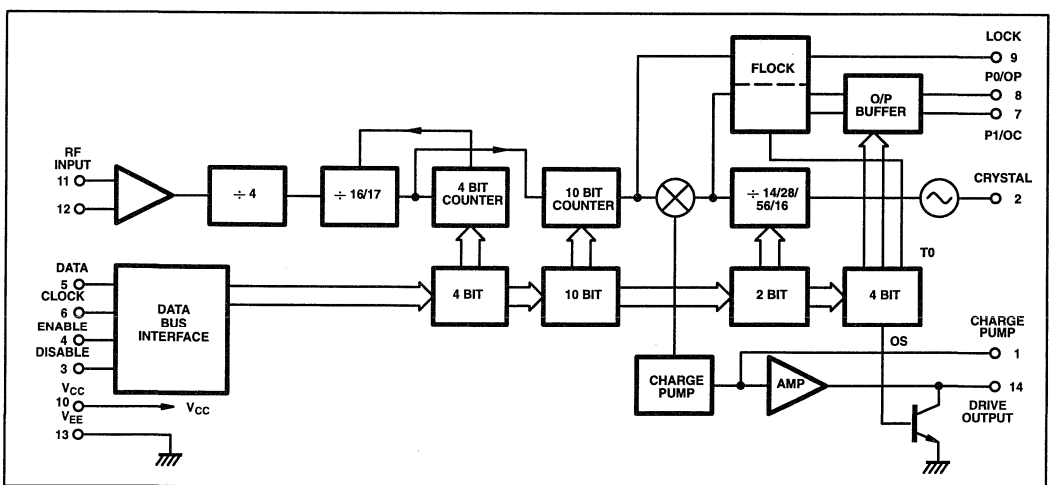


Fig. 2 Block diagram of SP5058

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +85°C, V_{CC}= +4.5V to +5.5V. These characteristics are guaranteed over the following conditions. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	10		70	85	mA	V_{CC}=5V
Prescaler input voltage		11, 12	50		400	mV_{RMS}	500MHz to 1.8GHz sinewave
Prescaler input voltage		11, 12	100		400	mV_{RMS}	2.6GHz See Fig.4
Prescaler input impedance		11, 12		50		Ω	
Input capacitance		11, 12		2		pF	
High level input voltage		3, 4, 5, 6	3		V_{CC}	V	
Low level input voltage		3, 4, 5, 6	0		0.7	V	
High level input sink current		3, 4, 5, 6			10	µA	V_{IN}=5.5V V_{CC}=5.5V
Low level input source current		3, 4, 5, 6			10	µA	V_{IN}=0V V_{CC}=5.5V
Clock input hysteresis		6		0.4		V	
Clock rate		6			0.5	MHz	
Data setup time	t_2	5	300			ns	See Fig. 6
Data hold time	t_3	5	600			ns	See Fig. 6
Enable setup time	t_1	4	300			ns	See Fig. 6
Enable hold time	t_5	4	600			ns	See Fig. 6
Clock–to–enable time	t_4	4	300			ns	See Fig. 6
Charge Pump output current		1	±200	±300		µA	V pin 1=2.0V
Charge Pump output leakage current				±1	±5	nA	V pin 1=2.0V
Drift due to leakage					5	mV/s	At collector of external varicap drive transistor
Charge Pump Drive output current		14	1			mA	V pin 14=0.7V
Charge Pump Amplifier Gain				6400			Pin 14 current=100µA
Oscillator Temperature Stability					2	ppm/°C	
Oscillator Stability with Supply Voltage					2	ppm/V	
Comparison frequency (at phase detector)					520	kHz	
External Reference Input Frequency		2	3.5		16	MHz	
External Reference Input Amplitude			200		500	mV p–p	AC Coupled sinewave
Reference Crystal Frequency		2	3.5		8	MHz	"Parallel Resonant " Crystal
Port Sink Current		7, 8	10			mA	V_{OUT}=0.7V
Lock Sink Current		9	1			mA	V_{OUT}=0.7V
Port Leakage Current		7, 8			10	µA	V_{OUT}=13.2V
Lock Leakage Current		9			10	µA	V_{OUT}=V_{CC}

ABSOLUTE MAXIMUM RATINGS

(All voltages are referred to V_{EE}=0V)

Parameter	Pin	Value			Units
		Min	Typ	Max	
Storage temperature range		–55		125	°C
Prescaler input signal	11, 12			2.5	V_{p-p}
DC VOLTAGES					
Supply	10	–0.3		7	V
Output ports	7, 8				
Off state		–0.3		14	V
On state		–0.3		6	V
Lock output DC offset	9	–0.3		V_{CC}+0.3	V
Loop amplifier DC offset	1, 14	–0.3		V_{CC}+0.3	V
Reference/Crystal input	2	–0.3		V_{CC}+0.3	V
Data bus inputs	3, 4, 5, 6	–0.3		V_{CC}+0.3	V
Prescaler DC offset	11, 12	–0.3		V_{CC}+0.3	V
THERMAL RESISTANCE MP14					
Die to ambient				123	°C/W
Die to case				45	°C/W
Power consumption (@ V_{CC}=5.5V)				470	mW
INPUT/OUTPUT PROTECTION MIL STD–883 METHOD 3015					
Electrostatic discharge		2.0			kV

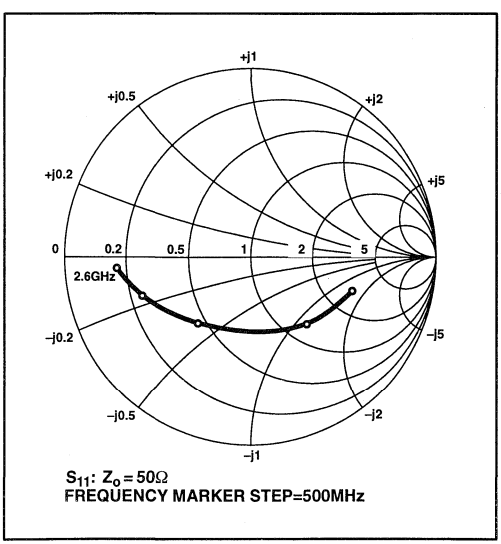


Fig. 3 Typical input impedance

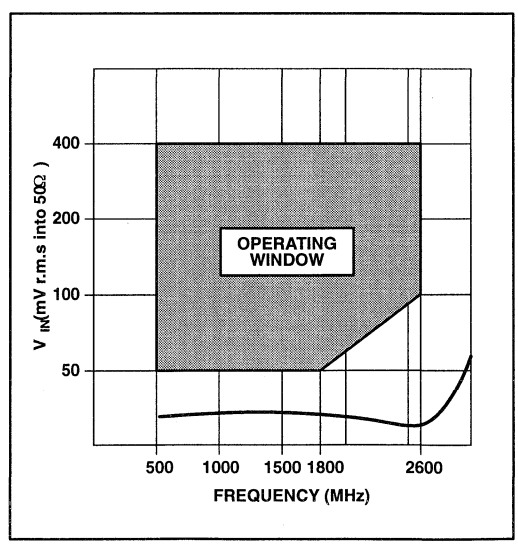


Fig. 4 Typical input sensitivity

FUNCTIONAL DESCRIPTION

The SP5058 contains all the elements necessary, with the exception of a frequency reference, loop filter and external high voltage transistor, to control a varicap tuned local oscillator, so forming a complete PLL frequency synthesised source. The use of a high comparison frequency gives excellent phase noise characteristics making the device particularly suitable for synthesising 1st oscillators in Double Conversion systems.

The SP5058 is controlled by a standard 3–wire bus comprising data, clock and enable inputs. The word consists of 20 bits, two of which are used for port selection, 14 to set the programmable divider, and the remaining four to select the reference division ratio, set the test mode and disable the varactor drive. The programming format is shown in Fig. 5

Data is only transferred to the internal shift register during enable high periods. The clock input is disabled when the enable is low. New data words are only accepted by the internal data buffers from the shift register on a negative transition of the enable.

The local oscillator output frequency is input to the prescaler/programmable divider where it is down by the ratio programmed. The output of the programmable divider, F_{pd}, is fed to the phase comparator where it is compared in both phase and frequency to the comparison frequency, F_{comp}.

F_{comp} may be obtained by two means, either by feeding in an external reference, or by use of an on–board crystal controlled oscillator. The programmable reference divider between the reference oscillator and the phase comparator gives a choice of comparison frequency. As an example of the comparison frequencies and related LO step sizes for a 7MHz reference frequency are shown in Table 1 below.

By careful choice of reference oscillator frequency and divider ratio the local oscillator step size can be optimised for each application. The phase comparator can operate with a comparison frequency up to 520kHz thus giving an LO step size up to 2080kHz.

The programmable divider is preceded by an input RF preamplifier and a high speed, low radiation prescaler thus giving excellent sensitivity at input frequencies between 500 and 2600MHz.

A 'lock detect' circuit is provided which generates a flag when the loop has obtained lock. 'In lock' is indicated by a high impedance state on the lock output.

The SP5058 also contains two open collector output ports, ports P0 and P1, may be used for a variety of band switching or driving purposes.

VARACTOR LINE/CHARGE PUMP DISABLE AND TEST FEATURES

The SP5058 offers the following facilities to aid testing and alignment of oscillators and tuners.

Varactor Line Disable – set by programming the OS bit to a 1.

Charge Pump Disable – set by forcing a 1 on the DIS input.

Test Mode – set by programming the T0 bit to a 1.

When in TEST mode the inputs to the Phase Comparator F_{pd} and F_{comp} are available on ports P0 and P1 respectively.

Reference Divider ratio	14	28	56	16
Comparison Frequency	500kHz	250kHz	125kHz	437.5kHz
Local Osc. Step Size	2MHz	1MHz	500kHz	1.75MHz

Table 1 Comparison and step frequencies with an 7MHz crystal

T0	OS	DIS	P0/OP	P1/OC	LOCK (In lock=Hi Z)	Functional Description
0	0	0	#	#	Lock Flag	Normal Operation
0	0	1	#	#	Lock Flag	Charge Pump Disable
1	0	0	F_{pd}	F_{comp}	Lock Flag	Normal Operation
0	1	0	#	#	Lock Flag	Varactor Line Disable
0	1	1	#	#	Lock Flag	Charge Pump and Varactor Line Disable
1	X	1	–	–	–	NOT PERMITTED
# Controlled by data bits P0, P1						

Table 2 Test Modes

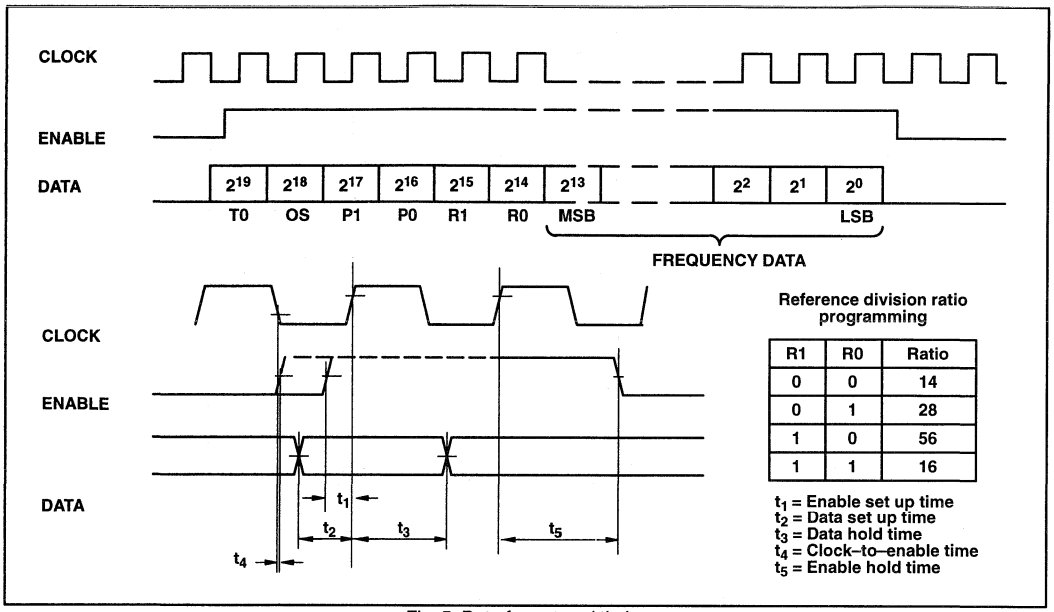
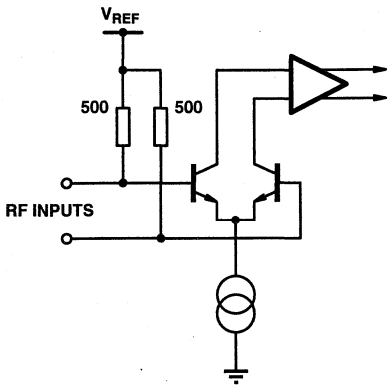
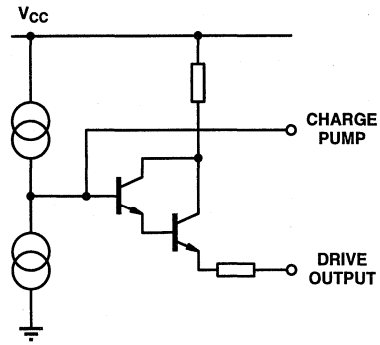


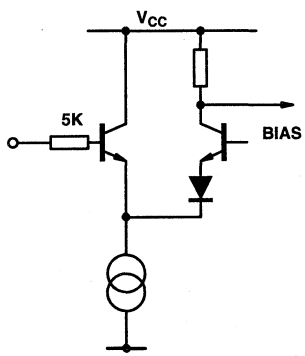
Fig. 5 Data format and timing



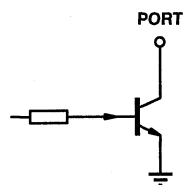
RF input



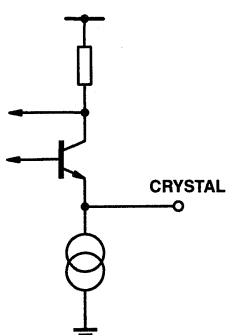
Loop amplifier



Enable, Data and Clock inputs



Output ports P0–P1



Reference oscillator

Fig.6 Input/Output interface circuits

DOUBLE CONVERSION TUNER SYSTEMS

The high 2.6GHz maximum operating frequency and excellent noise characteristics of the SP5058 enables the construction of double conversion high IF tuners when used in conjunction with the SP5022, a 1.6GHz frequency synthesiser.

A typical system shown in Fig.7 will use the SP5058 as the first LO control for full band upconversion to an IF of greater than 1GHz; the SP5022 is used to control the 2nd LO which downconverts the 1st IF to either a conventional IF, TV channel or other chosen frequency.

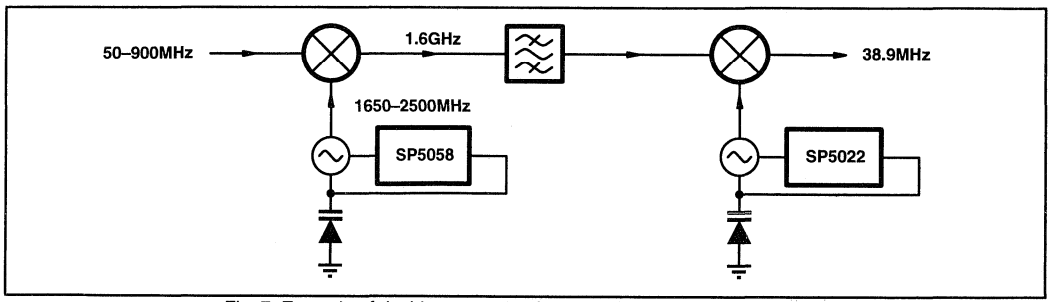


Fig. 7 Example of double conversion from VHF/UHF frequencies to TV IF

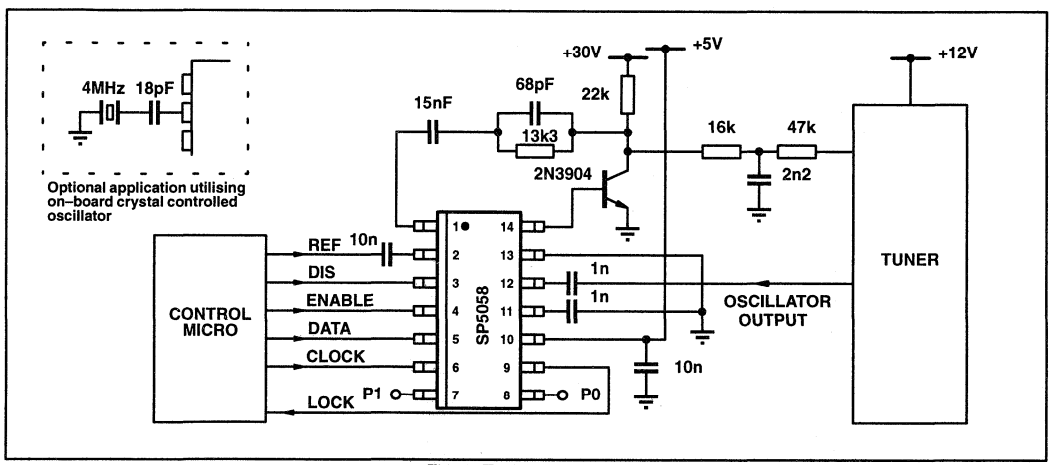


Fig. 8 Typical application

SP5070

2.4GHz FIXED MODULUS FREQUENCY SYNTHESISER

(Supersedes Consumer IC handbook September 1991)

The SP5070 is a single modulus frequency synthesiser for use in Satelite TV receivers and together with an appropriate voltage controlled oscillator (VCO), forms a complete phase locked loop (PLL) synthesiser. The circuit consists of a prescaler with preamplifier and a fixed modulus divider. The phase comparator is fed with a reference frequency derived from an external oscillator or crystal. The comparator has a charge pump output amplifier stage around which feedback may be applied. Only an external transistor is required for varicap line driving.

FEATURES

- Low Power Consumption (5V, 47mA Typ.)
- Prescaler and Preamplifier Included
- Charge Pump Amplifier with Feedback Point
- Charge Pump Disable Facility
- Synthesises Frequencies up to 2.4GHz
- Pin and Function Compatible with SP5060 and SP5062.
- Full ESD Protection *

  * Normal ESD handling procedures should be observed

APPLICATIONS

- Satelite TV
- High IF Cable Tuning Systems
- C–Band with Frequency Doubling Mixer

ORDERING INFORMATION

SP5070 DP – (14 Lead Plastic Package)
SP5070F MP – (14 Lead Miniature Plastic Package)

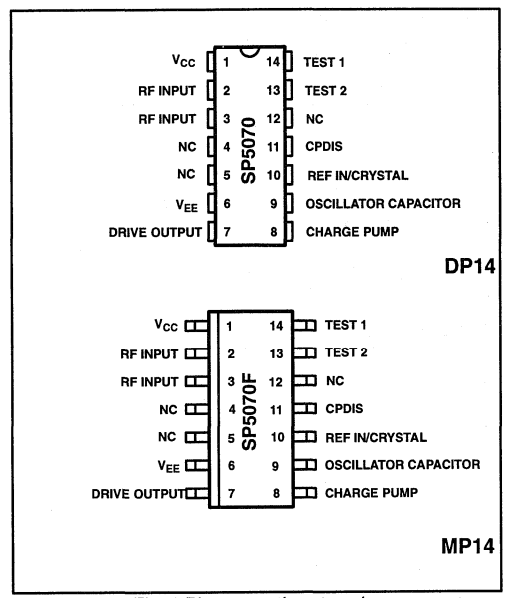


Fig. 1 Pin connections top view

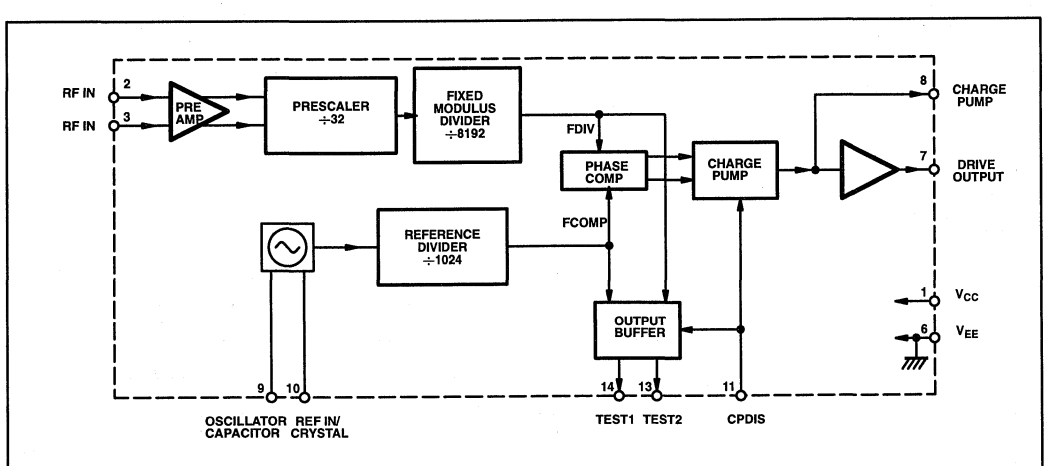


Fig. 2 Block diagram of SP5070

ELECTRICAL CHARACTERISTICS

T_{amb}= –40°C to +85°C, V_{CC}=+4.5V to +5.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Sym-bol	Pin	Value			Units	Conditions
			Min	Typ	Max		
Supply current	I_{CC}	1		47	55	mA	V_{CC} =5V
Prescaler input voltage		2, 3	50		300	mV_{RMS}	300MHz to 1.8GHz sinewave
Prescaler input voltage		2, 3	100		300	mV_{RMS}	2.4GHz, see Fig. 5
Prescaler input impedance		2, 3		50		Ω	
Input capacitance		2, 3		2		pF	
Charge pump output current		8		±100		µA	V pin 8=2.0V
Charge pump output leakage		8			±5	nA	V pin 8=2.0V
Drift due to leakage					5	mV/s	At collector of External Varicap Drive transistor
Charge pump drive output current		7	1			mA	V pin 7=0.7V
Charge pump amplifier gain				6400			pin 7 current 100µA
Oscillator temperature stability		9, 10			2	ppm/°C	
Oscillator stability with supply voltage		9, 10			2	ppm/V	
Reference clock frequency		10	2		10	MHz	
External reference amplitude		10	150		500	mV_{RMS}	
Charge pump disable/TEST1 and TEST2 enable		11	–250		–500	µA	V_{IN} <0V
Charge pump disable leakage		11			10	µA	V pin 11=V_{CC}
TEST1/TEST2 sink current		13, 14	1			mA	V_{OUT}=0.7V
TEST1/TEST2 leakage current		13, 14			10	µA	V_{OUT}=V_{CC}+0.3V
TEST1/TEST2 Voltage		13, 14			V_{CC}+0.3	V	

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE}=0V

Characteristics	Pin	Value		Units
		Min	Max	
Supply Voltage	1	–0.3	7	V
RF input voltage	2, 3		2.5	Vp–p
RF input DC offset	2, 3	–0.3	V_{CC}+0.3	V
Charge pump DC offset	8	–0.3	V_{CC}+0.3	V
Charge pump disable	11	–0.7	V_{CC}+0.3	V
Drive DC offset	7	–0.3	V_{CC}+0.3	V
Crystal oscillator DC offset	9, 10	–0.3	V_{CC}+0.3	V

ABSOLUTE MAXIMUM RATINGS (cont.)

All voltages are referred to V_{EE}=0V

Characteristics	Pin	Value		Units
		Min	Max	
TEST outputs	13, 14	–0.3	V_{CC}+0.3	V
Storage temperature		–55	150	°C
Junction temperature			+150	°C
DP14 Thermal resistance, chip–to–ambient			78	°C/W
DP14 thermal resistance, chip–to case			30	°C/W
MP14 thermal resistance, chip–to–ambient			123	°C/W
MP14 thermal resistance, chip–to–case			45	°C/W
Power consumption at 5.5V			275	mW

FUNCTIONAL DESCRIPTION

The SP5070, when used with a voltage controlled oscillator, forms a complete phase locked loop frequency synthesiser.

The phase comparator comparison frequency is obtained by dividing the reference frequency. This may be generated on–chip by means of an external crystal, or from an external reference oscillator.

The output of the prescaler is divided by the fixed modulus divider, producing an output frequency which is phased locked to the comparison frequency.

The divider stages are arranged to give a fixed ratio between the synthesised frequency and the reference of 256:1. Any frequency within the range of 300MHz to 2.4GHz may be achieved by using the appropriate reference or crystal frequency.

A single external transistor, driven from the charge pump output, provides the output drive necessary for the oscillator varicap line.

A test facility which disables the charge pump is also provided. This is activated when a negative voltage is applied to pin 11, see electrical characteristics above. When the device is in this mode, F_{COMP} and F_{DIV} are also available at outputs TEST1 and TEST2 respectively. These are open collector outputs and are each capable of sinking a minimum of 1mA. In normal mode of operation these outputs are high impedance.

For compatibility with SP5060/SP5062, pin 11 may be connected to V_{CC}.

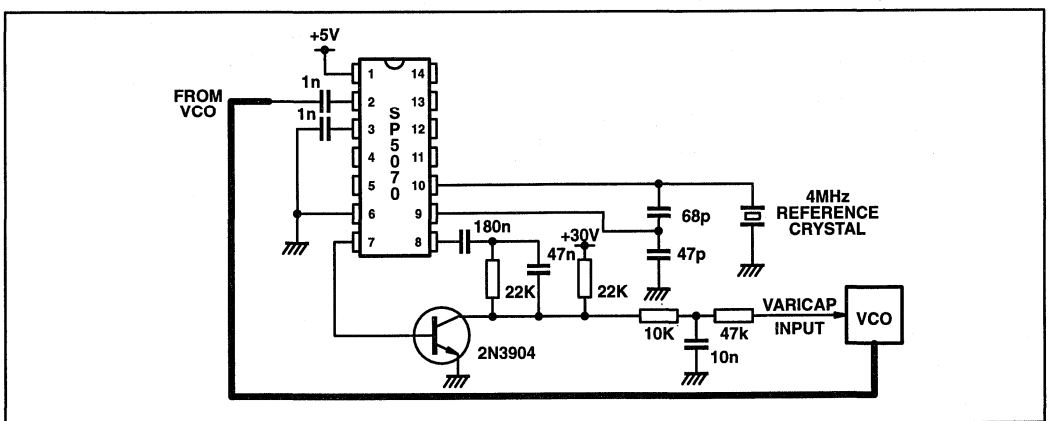


Fig. 3 Typical application and test circuit (1024MHz with 4MHz reference crystal)

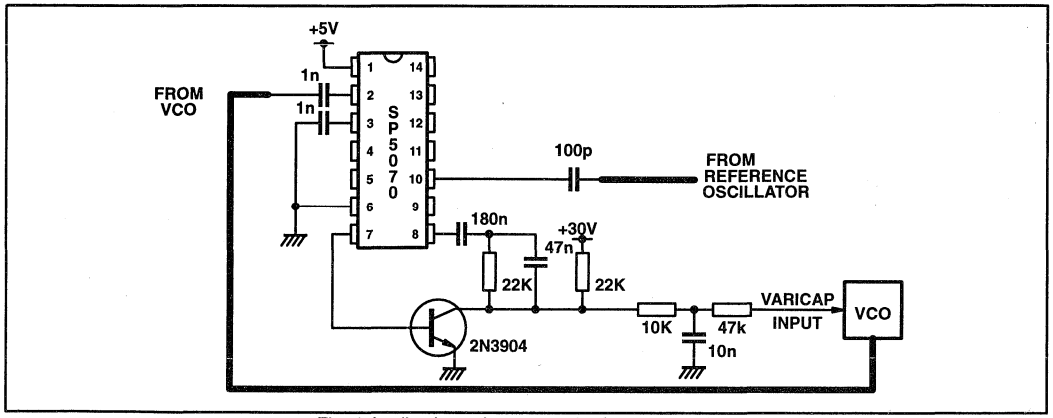


Fig. 4 Application using external reference oscillator

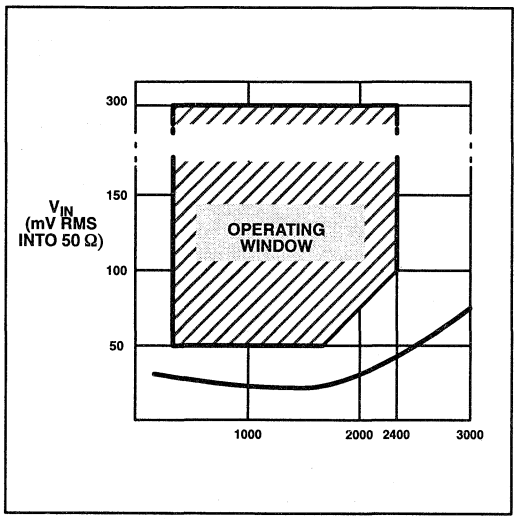


Fig.5 Typical input sensitivity

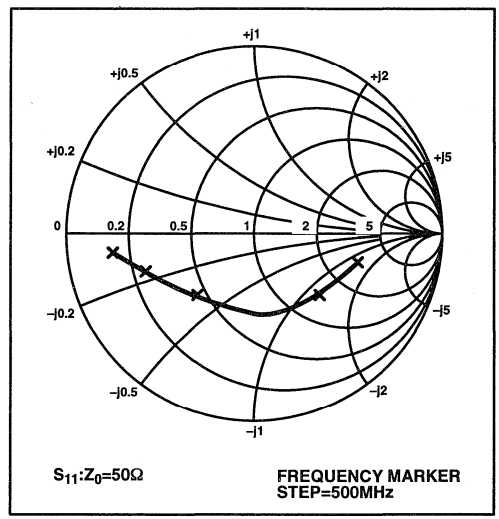


Fig. 6 Typical input impedance

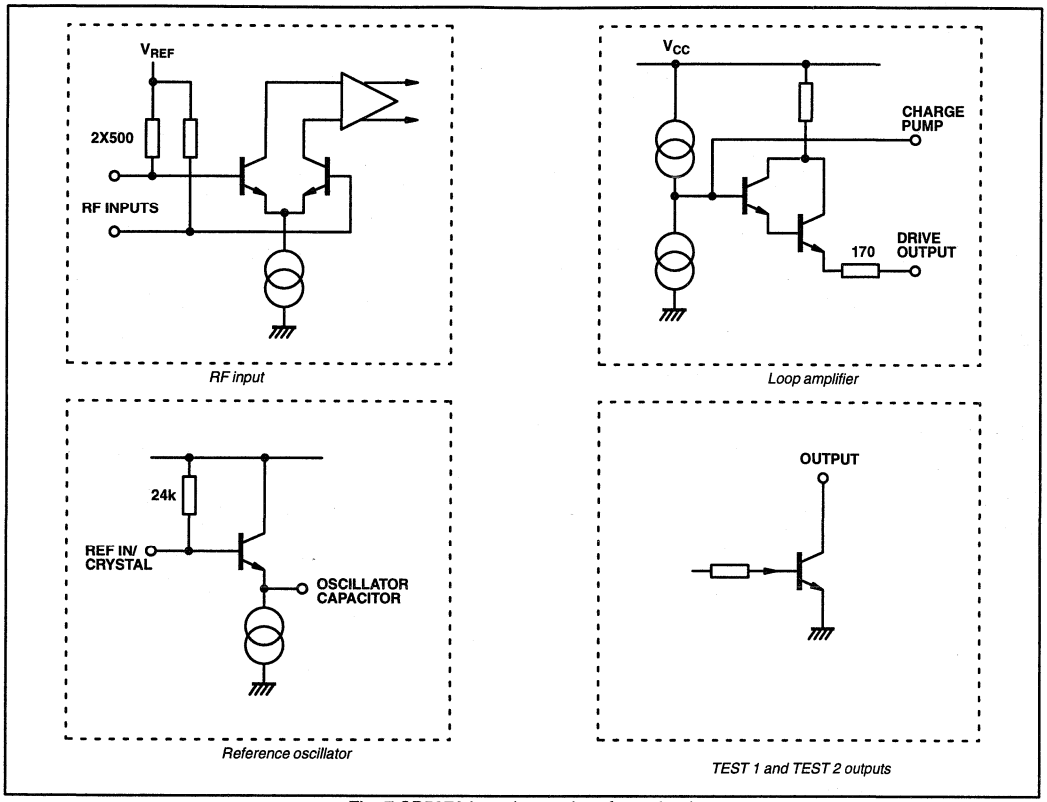


Fig. 7 SP5070 input/output interface circuits

SP5502

1·3 GHz I²C BUS 4-ADDRESS SYNTHESISER

The SP5502 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The SP5502 has four programmable I²C BUS addresses, which allows two or more synthesisers to be used in a system.

The device is available in two variants: the SP5502F in 14-lead miniature plastic package (MP14) and the SP5502S in 16-lead miniature plastic package (MP16). See Features below for functional differences between the devices.

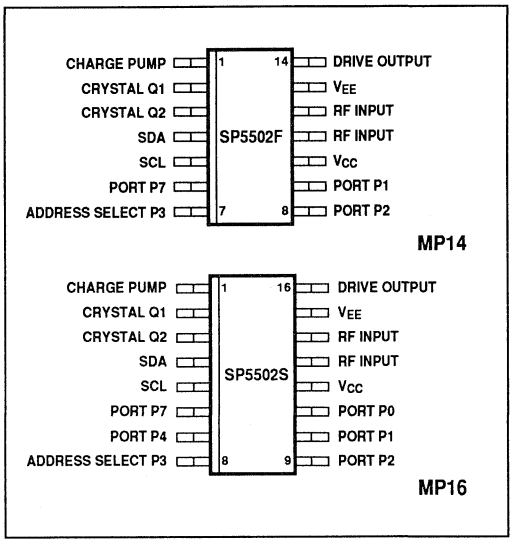


Fig. 1 Pin connections – top view

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (240mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 5×20mA Controllable Outputs (SP5502S)
- 3×20mA Controllable Outputs (SP5502F)
- Variable I²C BUS Address for Multi-Tuner Applications
- ESD Protection *

* Normal ESD handling precautions should be observed.

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5502F KG MPAS (14-lead miniature plastic package)
SP5502S KG MPAS (16-lead miniature plastic package)

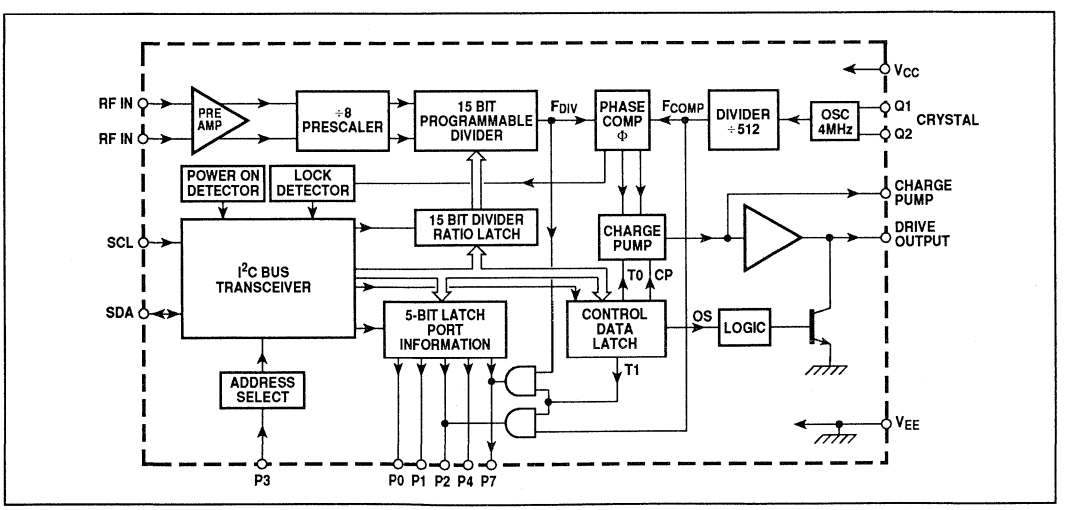


Fig. 2 Block diagram of SP5502S. (Ports P0 and P4 not present on SP5502F)

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V. All pin references are to the SP5502S (MP16 package).
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		48	60	mA	V_{CC} = 5V
Prescaler input voltage	13,14	12·5		300	mVrms	80MHz to 1GHz
Prescaler input voltage		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	13,14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		V_{CC}	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500				V pin 16 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator source impedance	2		−400		Ω	Nominal spread = ±15%
Output Ports						
Sink current	6,7,9-11	20			mA	V_{OUT} = 0·7V (see note 1)
Leakage current	6,7,9-11			10	µA	V_{OUT} = 13·2V
Input Port						
P3 input current high	8			1	mA	V pin 8 = V_{CC}
P3 input current low	8			−0·5	mA	V pin 8 = 0V

NOTES
1. Source impedance between all output ports and ground is approximately 5Ω. This should be taken into account when calculating output port saturation voltages.
2. The maximum resistance quoted refers to all conditions, including start-up.

FUNCTIONAL DESCRIPTION (Except where otherwise indicated, 'SP5502' refers to both variants)

The SP5502 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 3 shows how the address is selected by applying a voltage to P3. The address input is shown in Fig. 6. The LSB of the address Byte (R/$\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5502 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5502 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170µA and a logic 0 for ±50µA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P2 and P7, a logic 1 connects F_{COMP} to P2 and F_{DIV} to P7.

Byte 5 programs the output ports P0-P2, P4 and P7 on the SP5502S (P1, P2 and P7 only on SP5502F), a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2. Bit 1 (POR) is the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	X	X	P4*	X	P2	P1	P0*	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	N	N	N	N	N	N	A	**Byte 2**

Table 2 Read data format

MA1	MA0	Voltage input to P3
0	0	0V to 0·1V_{CC}
0	1	Open circuit
1	0	0·4V_{CC} to 0·6V_{CC}†
1	1	0·9V_{CC} to V_{CC}

Table 3 Address selection

A : Acknowledge bit
MA1, MA0 : Variable address bits (see Table 3)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P4*, P2, P1, P0* : Control output port states
POR : Power On Reset indicator
FL : Phase lock detect flag
X : Don't care
N : Not valid

NOTES
† Programmed by connecting a 15kΩ resistor between Address Select Port P3 and V_{CC}.
* Don't care condition on SP5502F.

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

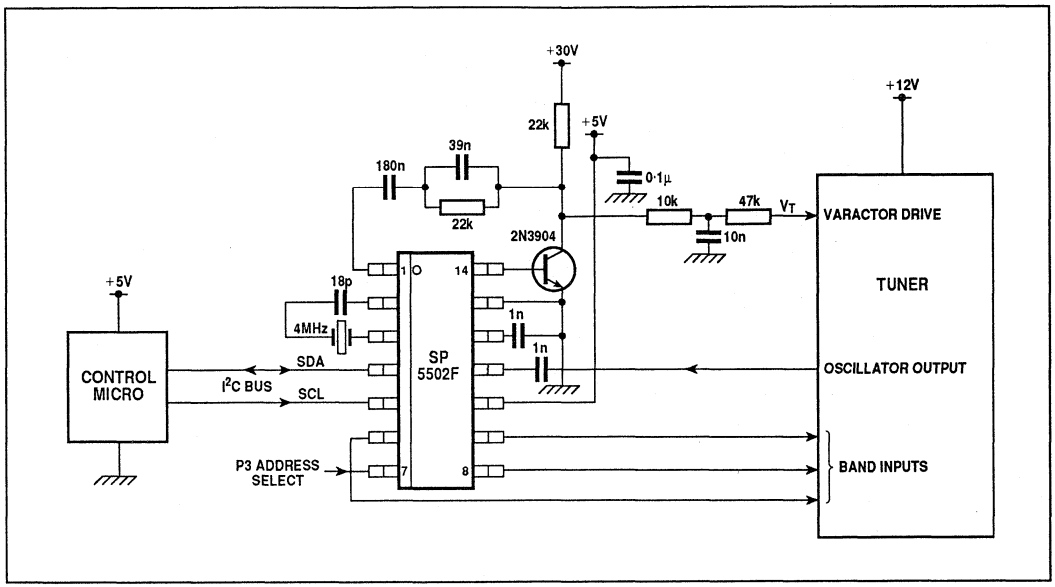


Fig. 4 Typical application

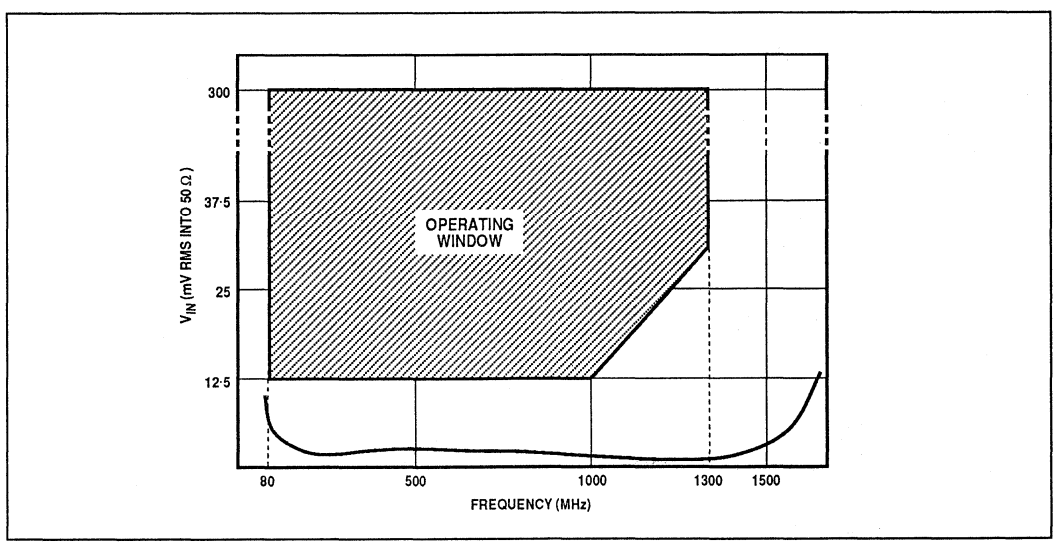


Fig. 5 Typical input sensitivity

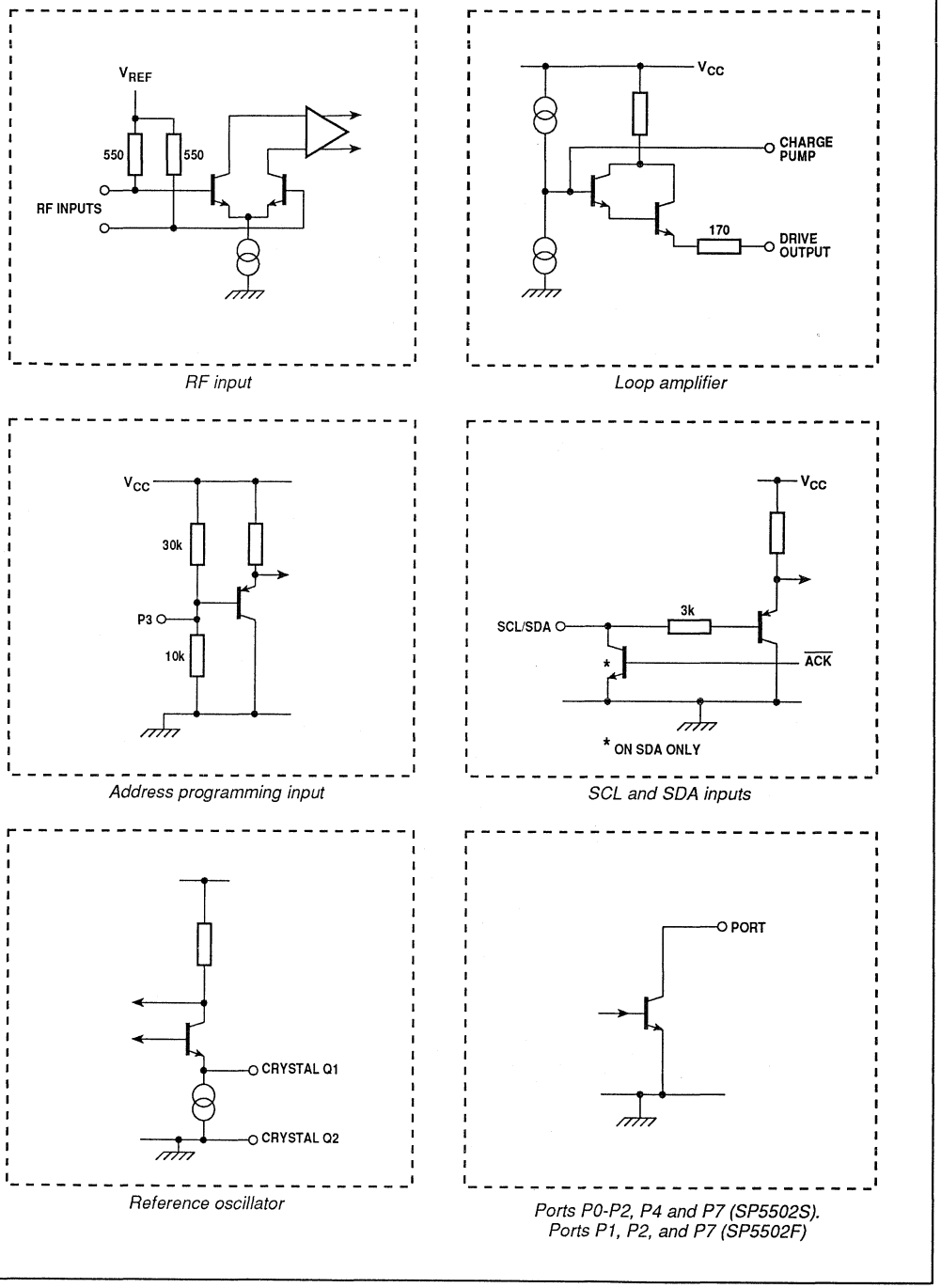


Fig. 6 SP5502 input/output interface circuits

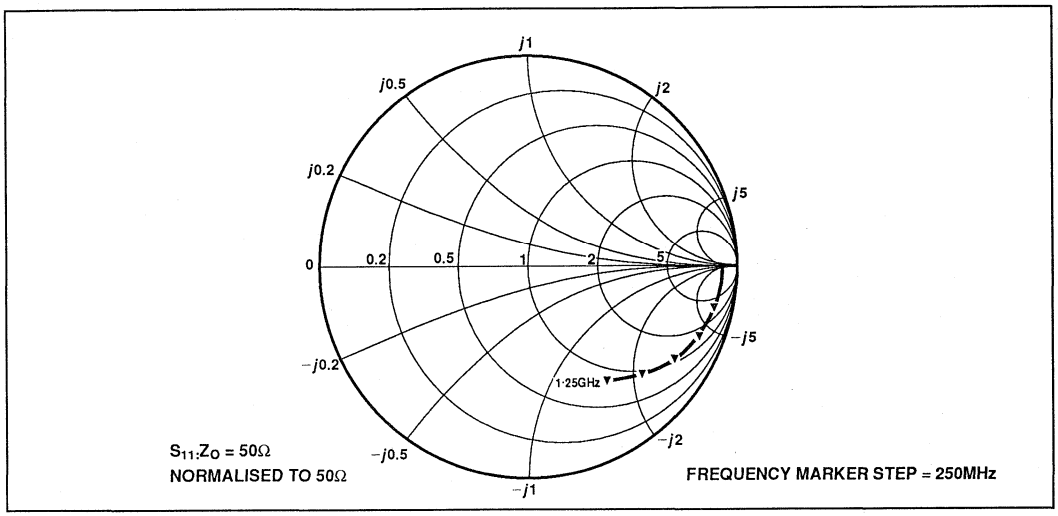


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} = 0V

Parameter	Pin		Value		Units	Conditions
	SP5502S	SP5502F	Min.	Max.		
Supply voltage	12	10	−0·3	7	V	
RF input voltage	13,14	11,12		2·5	V p-p	
Port voltage	6,7, 9-11	6,8, 9	−0·3	14	V	Port in off state
	6,7, 9-11	6,8, 9	−0·3	6	V	Port in on state
	8	7	−0·3	V_{CC}+0·3	V	
Total port output current	6,7, 9-11	6,8, 9		50	mA	
RF input DC offset	13,14	11,12	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	16	14	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
			−0·3	5·5	V	V_{CC} not applied
Storage temperature			−55	+150	°C	
Junction temperature				+150	°C	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
MP14 thermal resistance, chip-to-ambient				123	°C/W	
MP14 thermal resistance, chip-to-case				45	°C/W	
Power consumption at 5·5V				363	mW	

SP5510

1·3 GHz BIDIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

The SP5510 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. In 18-lead plastic DIL package (SP5510) and 20-lead miniature plastic package (SP5510T), the device has four addressable current-limited output ports (P0-P3) and four bi-directional open-collector ports (P4-P7), one of which (P6) is also a 3-bit 5-level ADC input. The information on these ports can be read via the I²C BUS. The SP5510S is a variant in a 16-lead miniature plastic package, without P0-P2 but functionally identical in other respects to the other two variants.

All variants have one fixed I²C BUS address and three programmable addresses, allowing two or more synthesisers to be used in a system.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (215mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-directional (SP5510, SP5510T)
- 5 Controllable Outputs, 4 Bi-directional (SP5510S)
- 5-Level ADC
- Variable I²C BUS Address for Picture in Picture TV
- ESD Protection *

* Normal ESD handling precautions should be observed.

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5510 NA DP (18-lead plastic package)
SP5510S NA MP (16-lead miniature plastic package)
SP5510T NA MP (20-lead miniature plastic package)

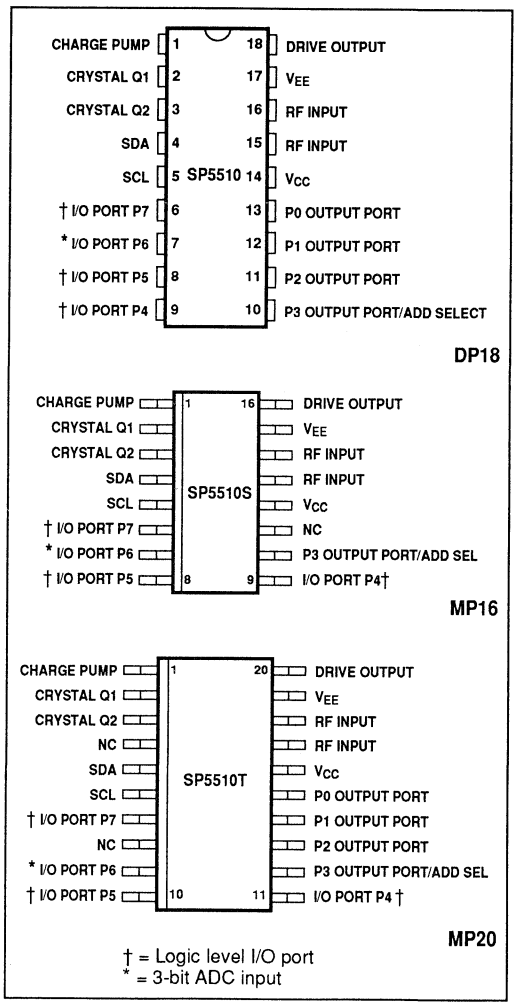


Fig. 1 Pin connections – top view

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V. All pin references are to the SP5510 (DP18 package). These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	14		43	53	mA	V_{CC} = 5V
Prescaler input voltage	15,16	12·5		300	mVrms	50MHz to 1GHz
Prescaler input voltage		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	15,16		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		5·5	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	18	500				V pin 18 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator source impedance	2		−400		Ω	Nominal spread = ±15%
Output Ports						
P0-P3 sink current (see note 1)	10-13	0·7	1	1·5	mA	V_{OUT} = 12V
P0-P3 leakage current (see note 1)	10-13			10	µA	V_{OUT} = 13·2V
P4-P7 sink current	6-9	10			mA	V_{OUT} = 0·7V
P4-P7 leakage current	6-9			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			+10	µA	V pin 10 = 13·2V
P3 input current low	10			−10	µA	V pin 10 = 0V
P4, P5, P7 input voltage low	6,8,9			0·8	V	
P4, P5, P7 input voltage high	6,8,9	2·7			V	
P6 input current high	7			+10	µA	See Table 3 for ADC levels
P6 input current low	7			−10	µA	

NOTES
1. Ports P0-P2 not present on the SP5510S.
2. The maximum resistance quoted refers to all conditions, including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V. Pin references are for SP5510 (DP18 package)

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	14	−0·3	7	V	
RF input voltage	15,16		2·5	V p-p	
Port voltage	6-13	−0·3	14	V	Port in off state
	6-9	−0·3	6	V	Port in on state
	10-13	−0·3	14	V	Port in on state
Total port output current	6-13		50	mA	
RF input DC offset	15-16	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	18	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
		−0·3	5·5	V	V_{CC} not applied
Storage temperature		−55	+150	°C	
Junction temperature			+150	°C	
DP18 thermal resistance, chip-to-ambient			78	°C/W	
DP18 thermal resistance, chip-to-case			24	°C/W	
MP16 thermal resistance, chip-to-ambient			111	°C/W	
MP16 thermal resistance, chip-to-case			41	°C/W	
MP20 thermal resistance, chip-to-ambient			93	°C/W	
MP20 thermal resistance, chip-to-case			34	°C/W	
Power consumption at 5·5V			321	mW	

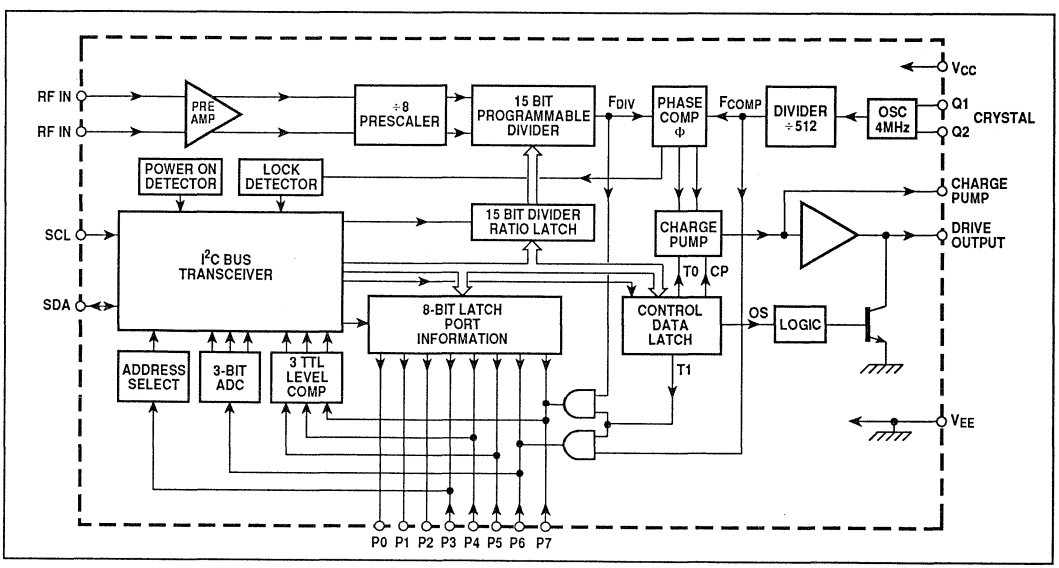


Fig. 2 Block diagram. (Ports P0-P2 not present on SP5510S)

FUNCTIONAL DESCRIPTION

The SP5510 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The LSB of the address Byte ($R/\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5510 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5510 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170μA and a logic 0 for ±50μA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7.

Byte 5 programs the output ports P0-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format

A2	A1	A0	Voltage input to P6
1	0	0	$0{\cdot}6V_{CC}$ to $13{\cdot}2V$
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0V to $0{\cdot}15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ to $13{\cdot}2V$

Table 4 Address selection

A : Acknowledge bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0* : Control output port states
POR : Power On Reset indicator
FL : Phase lock detect flag
I2, I1, I0 : Digital information from ports P7, P5 and P4 respectively
A2, A1, A0 : 5-level ADC data from P6 (see Table 3)

NOTE
* Don't care condition on SP5510S.

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

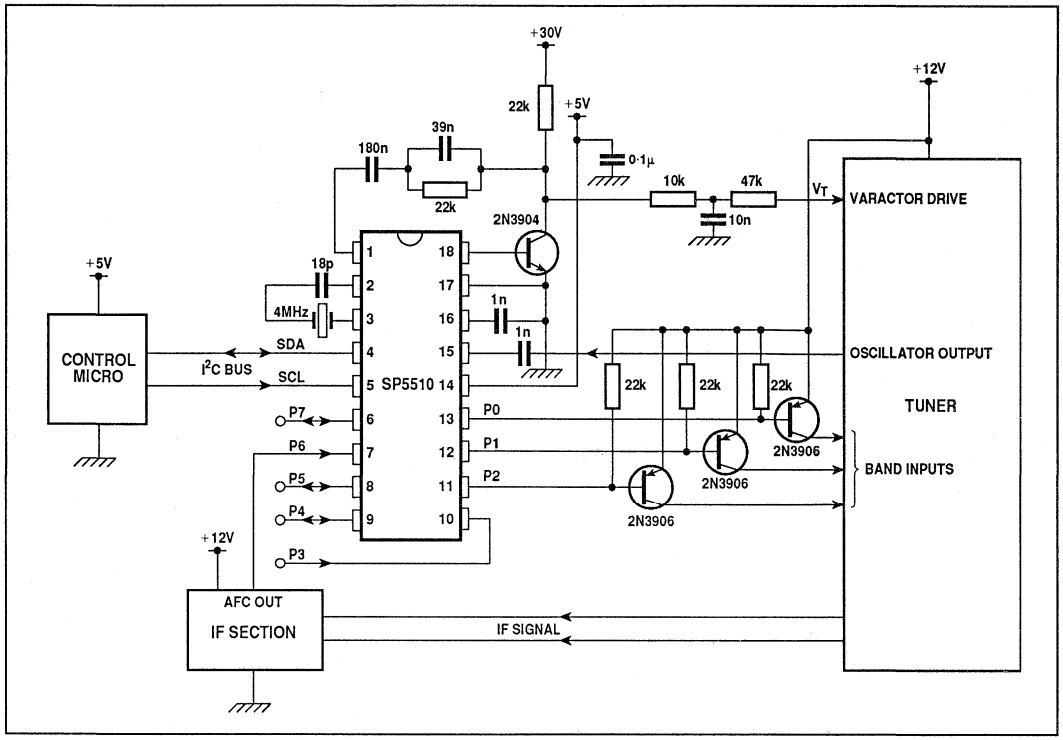


Fig. 4 Typical application

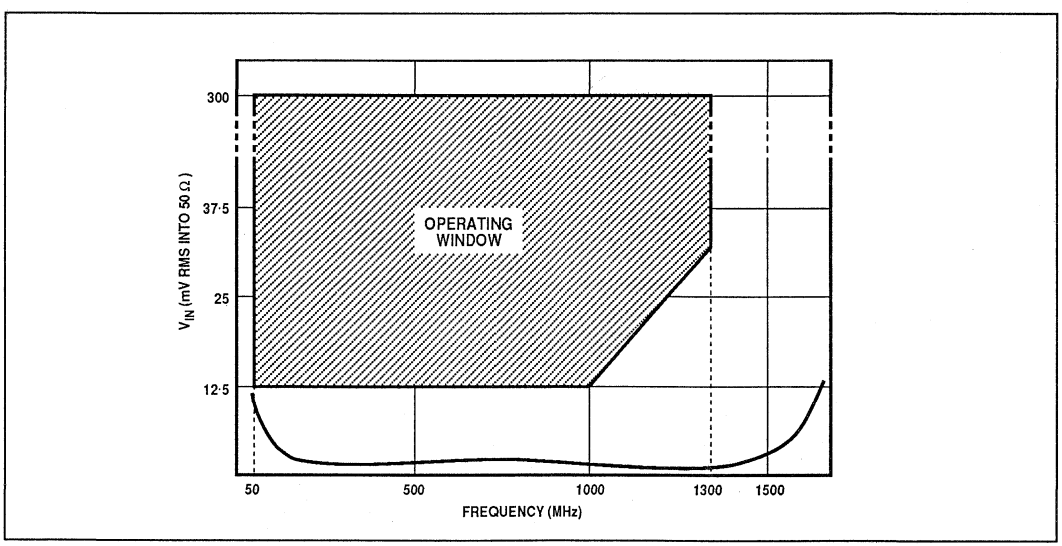
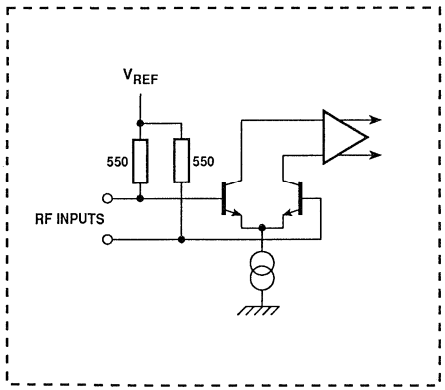
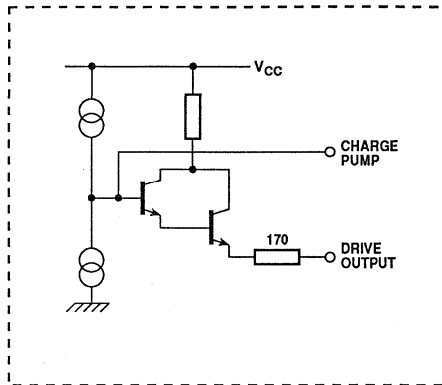


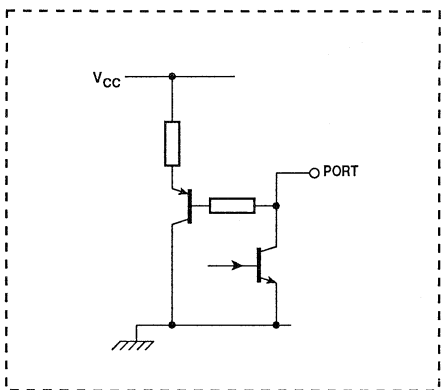
Fig. 5 Typical input sensitivity



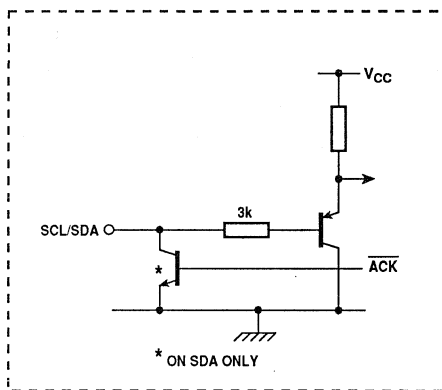
RF input



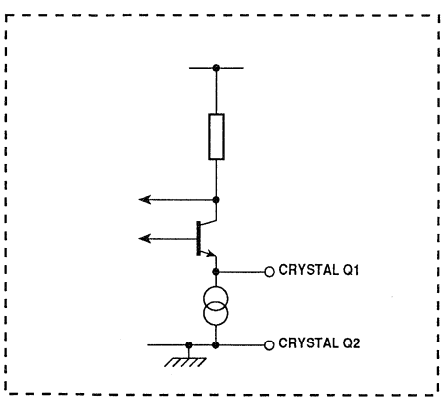
Loop amplifier



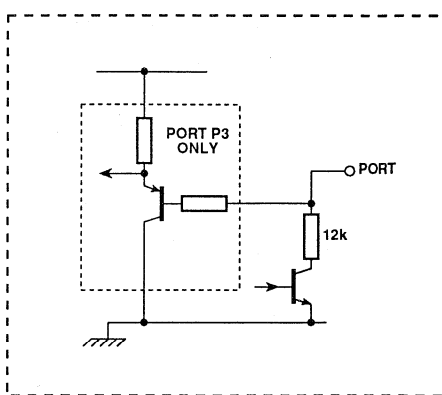
Ports P7 - P4



SCL and SDA inputs



Reference oscillator



Ports P0-P3 (SP5510 AND SP5510T).
P3 only on SP5510S.

Fig. 6 SP5510 input/output interface circuits

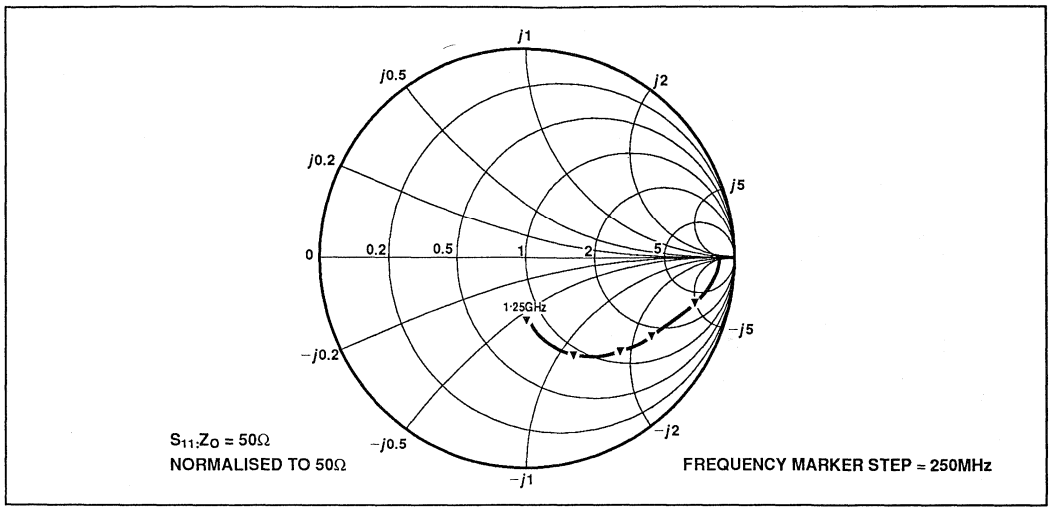


Fig. 7 Typical input impedance, SP5510

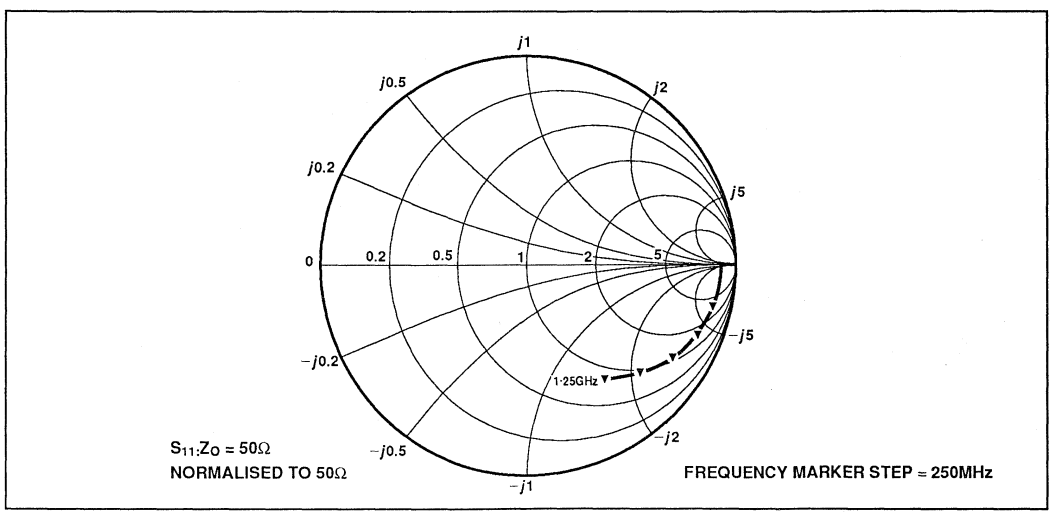


Fig. 8 Typical input impedance, SP5510S and SP5510T

SP5511

1·3 GHz BIDIRECTIONAL I²C BUS 4-ADDRESS SYNTHESISER

The SP5511 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. In 18-lead plastic DIL package, the SP5511 has three addressable current-limited output ports (P0-P3) and four bi-directional output ports (P0-P2) and four addressable bi-directional open-collector ports (P4-P7) of which P6 is also a 3-bit 5-level ADC input. The information on these ports can be read via the I²C BUS. The SP5511S is a variant in a 16-lead miniature plastic package, without P0-P2 but functionally identical in other respects to the SP5511.

The device has four programmable I²C BUS addresses, allowing two or more synthesisers to be used in a system.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (240mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 7 Controllable Outputs, 4 Bi-directional (SP5511)
- 4 Bi-directional Controllable Outputs (SP5511S)
- 5-Level ADC
- Variable I²C BUS Address for Picture in Picture TV
- ESD Protection *

* Normal ESD handling precautions should be observed.

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

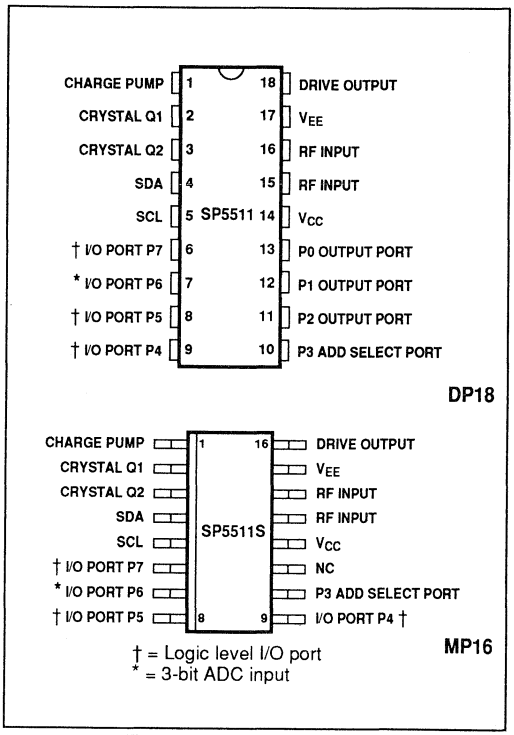


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SP5511 NA DP (18-lead plastic package)
SP5511S NA MP (16-lead miniature plastic package)

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V. All pin references are to the SP5511 (DP18 package). These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	14		48	60	mA	V_{CC} = 5V
Prescaler input voltage	15,16	12·5		300	mVrms	80MHz to 1GHz
		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	15,16		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		5·5	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	18	500				V pin 18 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator source impedance	2		−400		Ω	Nominal spread = ±15%
Output Ports						
P0-P2 sink current (see note 1)	11-13	0·7	1	1·5	mA	V_{OUT} = 12V
P0-P2 leakage current (see note 1)	11-13			10	µA	V_{OUT} = 13·2V
P4-P7 sink current	6-9	10			mA	V_{OUT} = 0·7V
P4-P7 leakage current	6-9			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			1	mA	V pin 10 = 13·2V
P3 input current low	10			−0·5	mA	V pin 10 = 0V
P4, P5, P7 input voltage low	6,8,9			0·8	V	
P4, P5, P7 input voltage high	6,8,9	2·7			V	
P6 input current high	7			+10	µA	See Table 3 for ADC levels
P6 input current low	7			−10	µA	

NOTES
1. Ports P0-P2 not present on the SP5511S
2. The maximum resistance quoted refers to all conditions, including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V

Parameter	Pin		Value		Units	Conditions
	SP5511	SP5511S	Min.	Max.		
Supply voltage	14	12	−0·3	7	V	
RF input voltage	15,16	13,14		2·5	V p-p	
Port voltage	6-9,11-13	6-9	−0·3	14	V	Port in off state
	6-9	6-9	−0·3	6	V	Port in on state
	11-13	-	−0·3	14	V	Port in on state
	10	10	−0·3	V_{CC}+0·3	V	
Total port output current	6-9,11-13	6-9		50	mA	
RF input DC offset	15-16	13-14	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	18	16	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
			−0·3	5·5	V	V_{CC} not applied
Storage temperature			−55	+150	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip-to-ambient				78	°C/W	
DP18 thermal resistance, chip-to-case				24	°C/W	
MP16 thermal resistance, chip-to-ambient				111	°C/W	
MP16 thermal resistance, chip-to-case				41	°C/W	
Power consumption at 5·5V				363	mW	

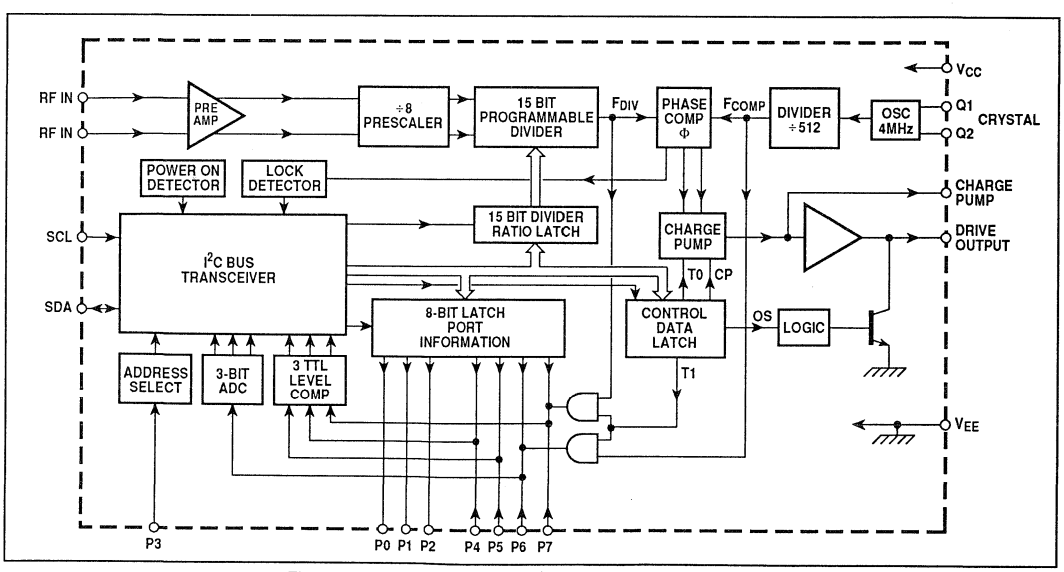


Fig. 2 Block diagram. (Ports P0-P2 not present on SP5511S)

FUNCTIONAL DESCRIPTION

The SP5511 is programmed from an I^2C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I^2C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The address input circuit is shown in Fig.6. The LSB of the address Byte ($R/\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5511 receives a correct address Byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data Bytes are programmed. When the SP5511 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status Byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that Byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data Bytes can be entered without the need to re-address the device until an I^2C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for $\pm 170\mu A$ and a logic 0 for $\pm 50\mu A$, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7.

Byte 5 programs the output ports P0-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format

A2	A1	A0	Voltage input to P6
1	0	0	$0{\cdot}6V_{CC}$ to 13·2V
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0V to $0{\cdot}15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}1V_{CC}$
0	1	Open circuit
1	0	$0{\cdot}4V_{CC}$ to $0{\cdot}6V_{CC}$†
1	1	$0{\cdot}9V_{CC}$ to V_{CC}

Table 4 Address selection

A : Acknowledge bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2*, P1*, P0* : Control output port states
POR : Power On Reset indicator
FL : Phase lock detect flag
I2, I1, I0 : Digital information from ports P7, P5 and P4 respectively
A2, A1, A0 : 5-level ADC data from P6 (see Table 3)

NOTE

† Programmed by connecting a 15kΩ resistor between pin 10 and V_{CC}
* Don't care condition on SP5511S.

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

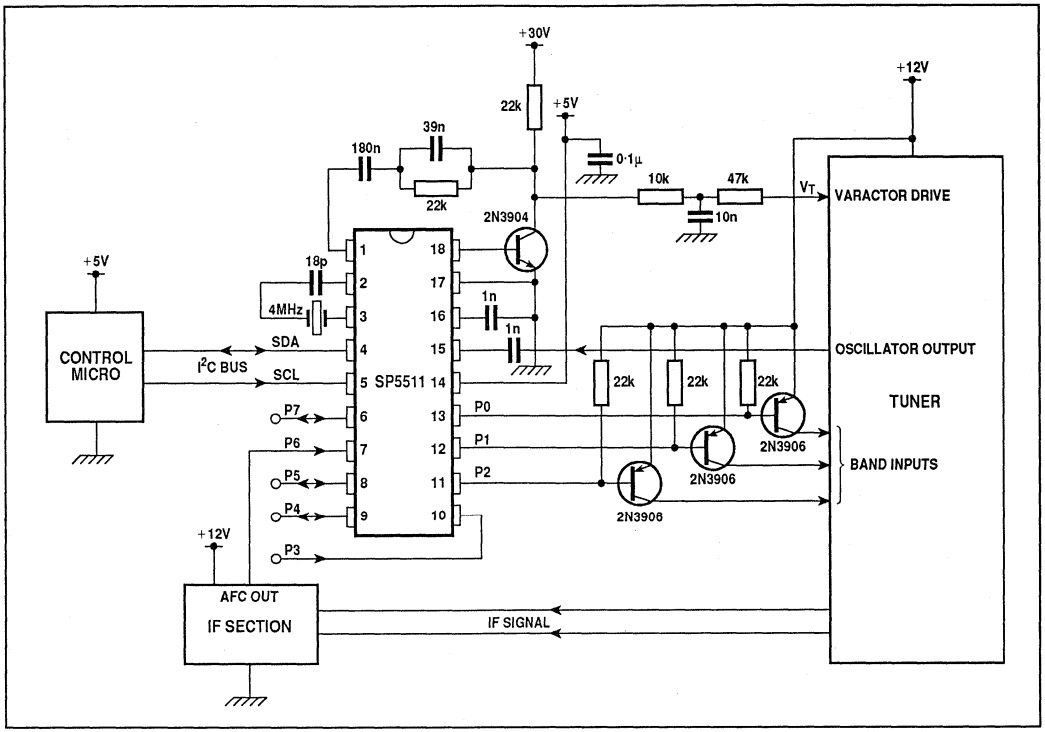


Fig. 4 Typical application

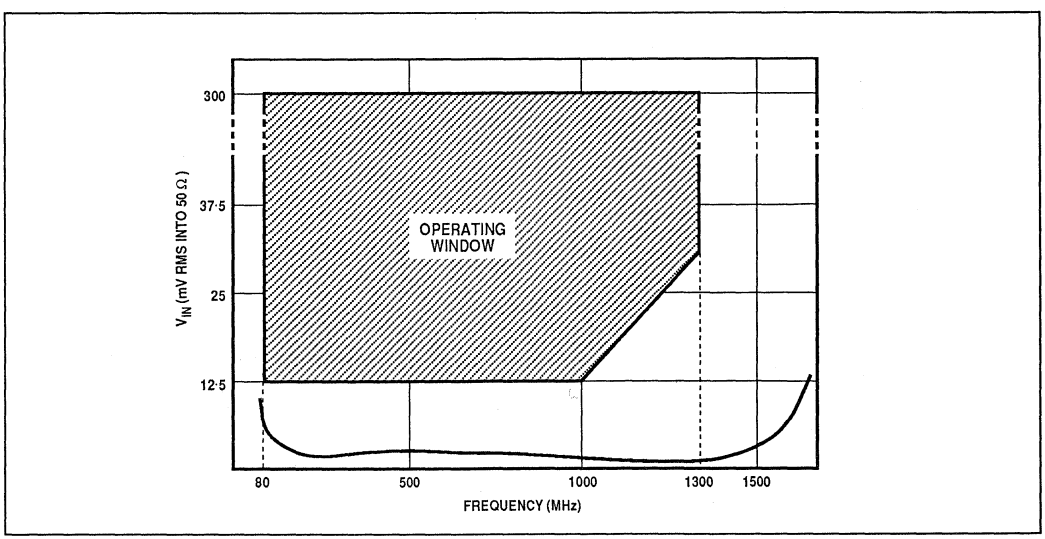
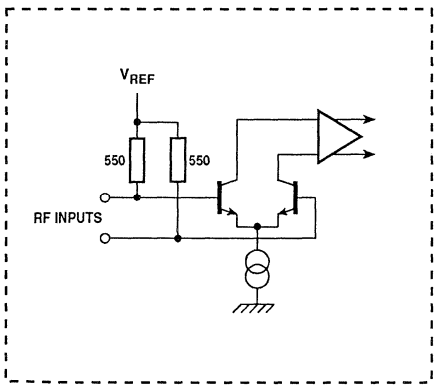
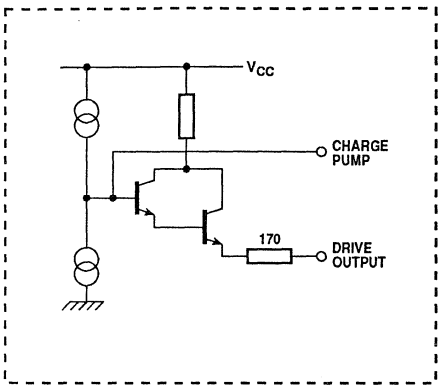


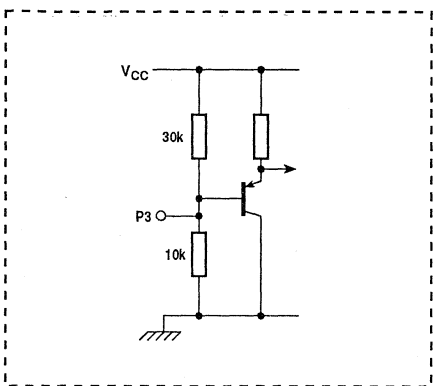
Fig. 5 Typical input sensitivity



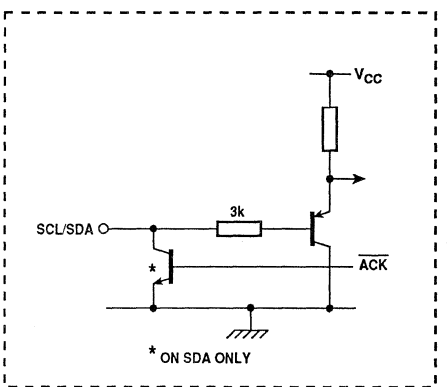
RF input



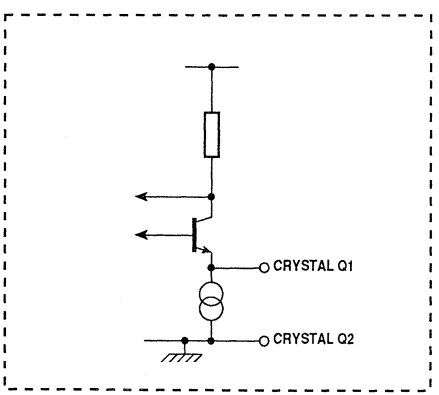
Loop amplifier



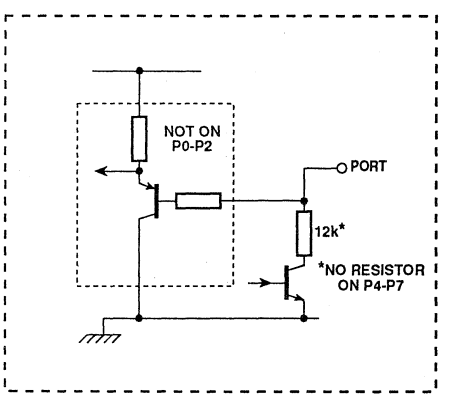
Address programming port



SCL and SDA inputs



Reference oscillator



Ports P0-P2 and P4-P7 (SP5511).
P4- P7 only on SP5511S

Fig. 6 SP5511 input/output interface circuits

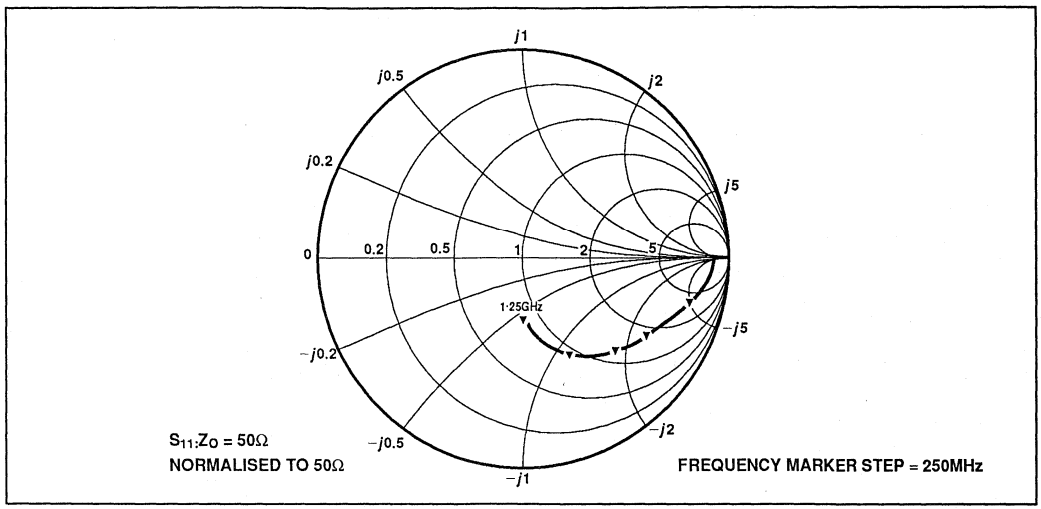


Fig. 7 Typical input impedance, SP5511

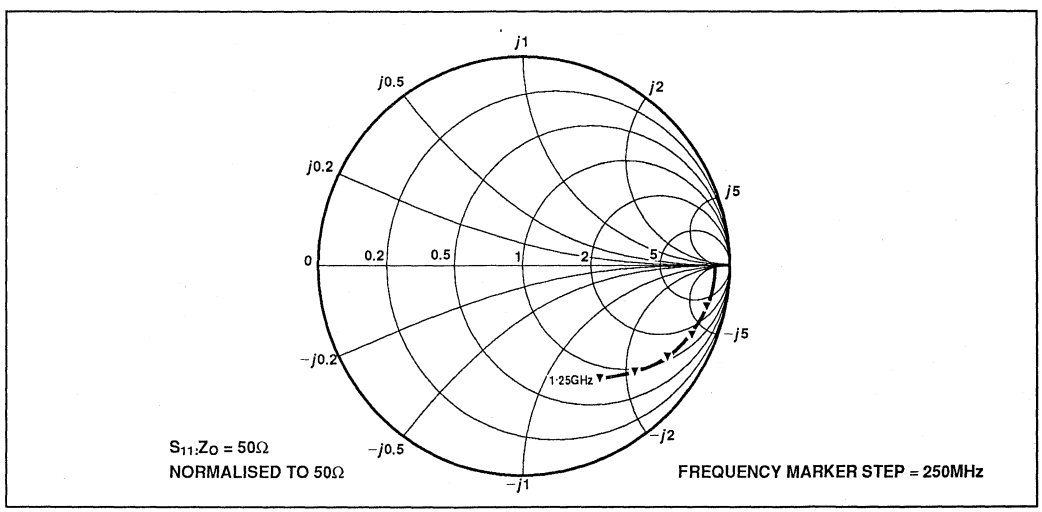


Fig. 8 Typical input impedance, SP5511S

SP5512

1·3 GHz BIDIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

The SP5512 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. In 18-lead plastic DIL package (SP5512) and 20-lead miniature plastic package (SP5512T), the device has eight controllable open-collector output ports (P0-P7), each capable of sinking 20mA. In addition, P6 is a 3-bit 5-level ADC input. The information on these ports can be read via the I²C BUS. The SP5512S is a variant in a 16-lead miniature plastic package, without P0 and P1 but functionally identical in other respects to the other two variants.

All variants have one fixed I²C BUS address and three programmable addresses, allowing two or more synthesisers to be used in a system.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (215mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi-directional (SP5512, SP5512T)
- 6 Controllable Outputs, 4 Bi-directional (SP5512S)
- 5-Level ADC
- Variable I²C BUS Address for Picture in Picture TV
- ESD Protection *

* Normal ESD handling precautions should be observed.

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5512 KG DPAS (18-lead plastic package)
SP5512S KG MPAS (16-lead miniature plastic package)
SP5512T KG MPES (20-lead miniature plastic package)

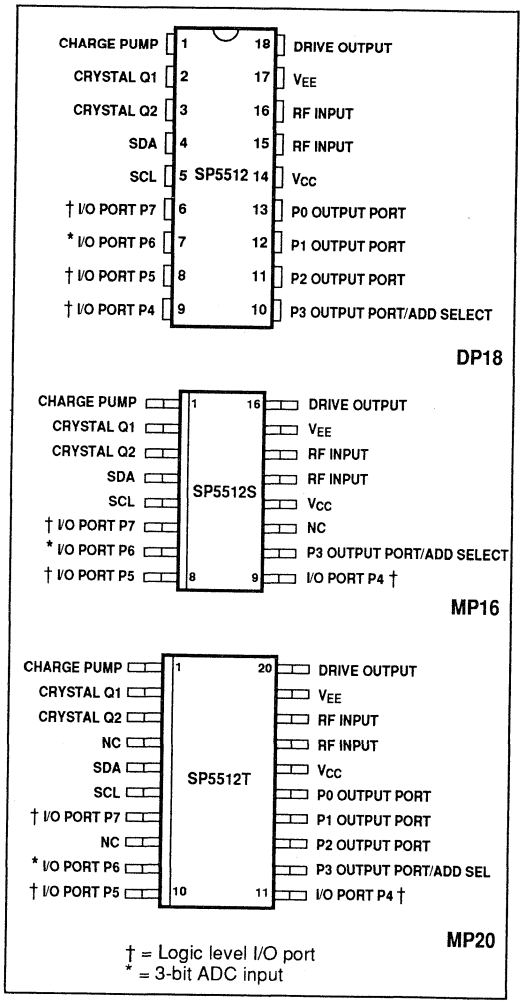


Fig. 1 Pin connections – top view

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V. All pin references are to the SP5512 (DP18 package).
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	14		43	53	mA	V_{CC} = 5V
Prescaler input voltage	15,16	12·5		300	mVrms	50MHz to 1GHz
		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	15,16		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		5·5	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	18	500				V pin 18 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 3)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator source impedance	2		−400		Ω	Nominal spread = ±15%
Output Ports						
P0-P7 sink current (see note 1)	6-13	20			mA	V_{OUT} = 0·7V, see note 2
P0-P7 leakage current (see note 1)	6-13			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			+10	µA	V pin 10 = 13·2V
P3 input current low	10			−10	µA	V pin 10 = 0V
P4, P5, P7 input voltage low	6,8,9			0·8	V	
P4, P5, P7 input voltage high	6,8,9	2·7			V	
P6 input current high	7			+10	µA	See Table 3 for ADC levels
P6 input current low	7			−10	µA	

NOTES
1. Ports P0 and P1 not present on the SP5512S.
2. Source impedance between all output ports and ground is approximately 5Ω. This should be taken into account when calculating output port saturation voltages.
3. The recommended crystal series resistance quoted refers to all conditions including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V. Pin references are for SP5512 (DP18 package)

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	14	−0·3	7	V	
RF input voltage	15,16		2·5	V p-p	
Port voltage	6-13	−0·3	14	V	Port in off state
	6-13	−0·3	6	V	Port in on state
Total port output current	6-13		50	mA	
RF input DC offset	15-16	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	18	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
		−0·3	5·5	V	V_{CC} not applied
Storage temperature		−55	+150	°C	
Junction temperature			+150	°C	
DP18 thermal resistance, chip-to-ambient			78	°C/W	
DP18 thermal resistance, chip-to-case			24	°C/W	
MP16 thermal resistance, chip-to-ambient			111	°C/W	
MP16 thermal resistance, chip-to-case			41	°C/W	
MP20 thermal resistance, chip-to-ambient			93	°C/W	
MP20 thermal resistance, chip-to-case			34	°C/W	
Power consumption at 5·5V			321	mW	

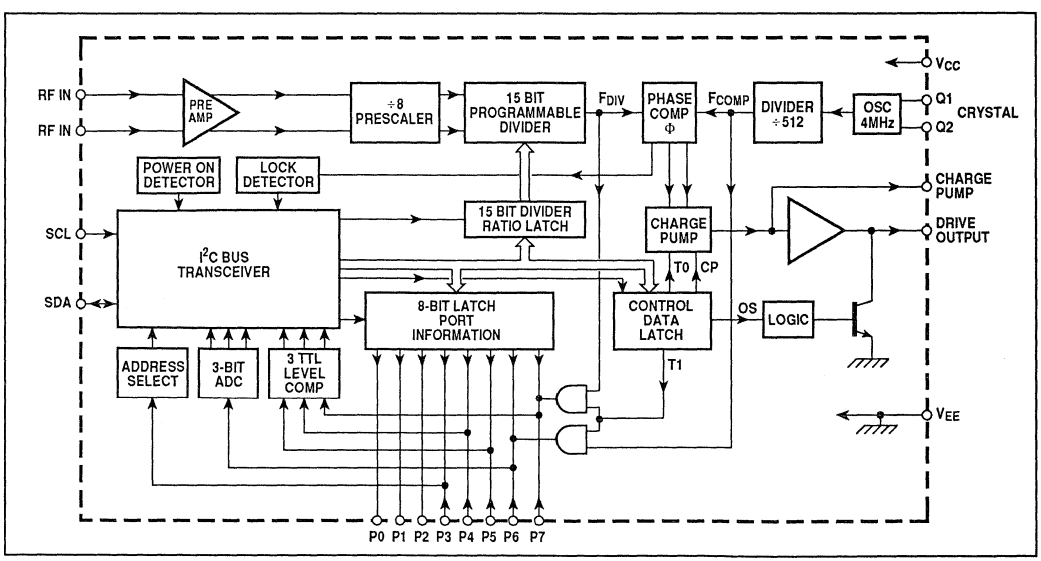


Fig. 2 Block diagram. (Ports P0 and P1 not present on SP5512S)

FUNCTIONAL DESCRIPTION

The SP5512 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C BUS system. Table 4 shows how the address is selected by applying a voltage to P3. The LSB of the address byte ($R/\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5512 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5512 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (e.g., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Figs. 7 and 8.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170µA and a logic 0 for ±50µA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7.

Byte 5 programs the output ports P0-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	P2	P1*	P0*	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format

A2	A1	A0	Voltage input to P6
1	0	0	$0{\cdot}6V_{CC}$ to $13{\cdot}2V$
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0V to $0{\cdot}15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ to $13{\cdot}2V$

Table 4 Address selection

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 4)
CP	:	Charge Pump current select
T1	:	Test mode selection
T0	:	Charge pump disable
OS	:	Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P2, P1*, P0*	:	Control output port states
POR	:	Power On Reset indicator
FL	:	Phase lock detect flag
I2, I1, I0	:	Digital information from ports P7, P5 and P4 respectively
A2, A1, A0	:	5-level ADC data from P6 (see Table 3)

NOTE
* Don't care condition on SP5512S.

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

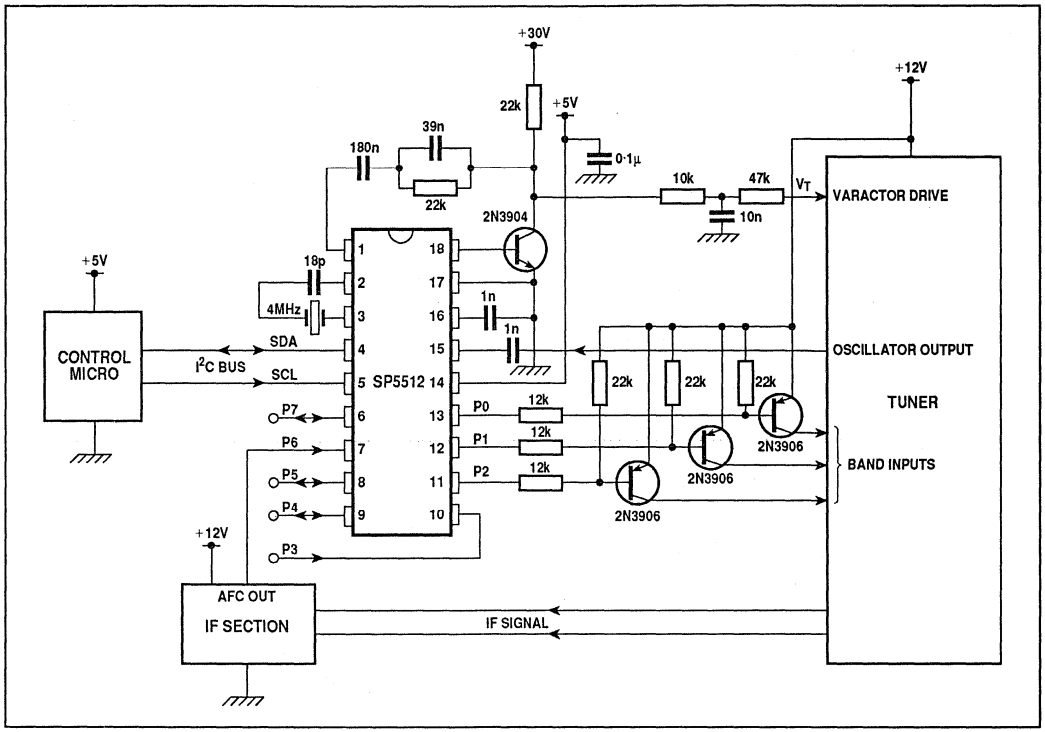


Fig. 4 Typical application

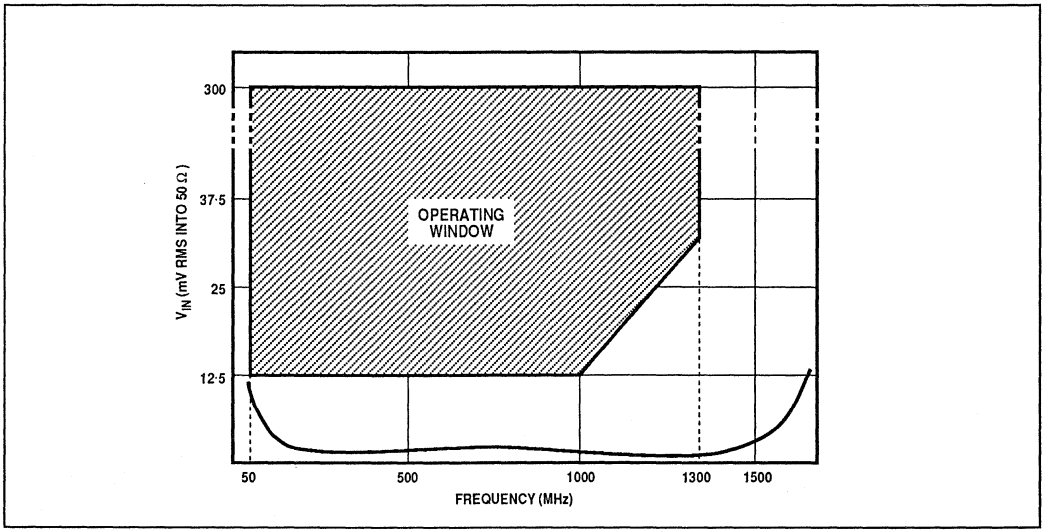
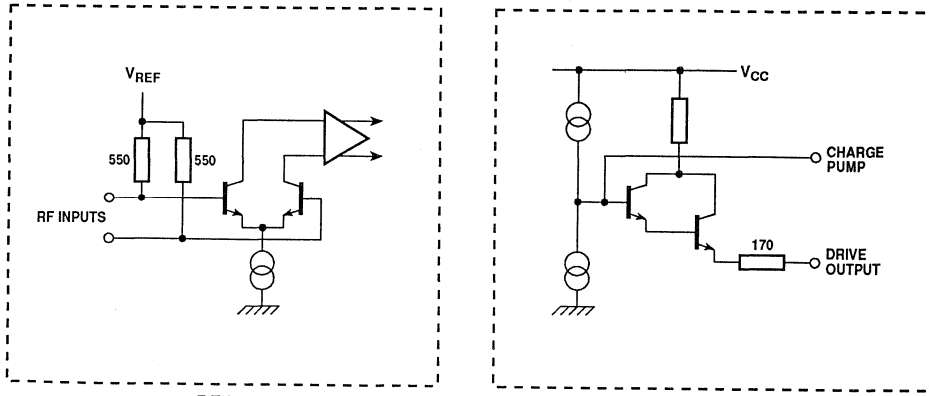
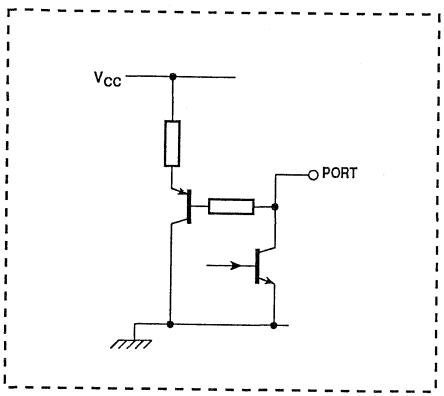


Fig. 5 Typical input sensitivity

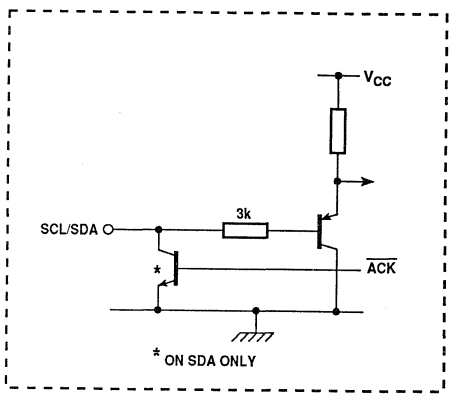


RF input

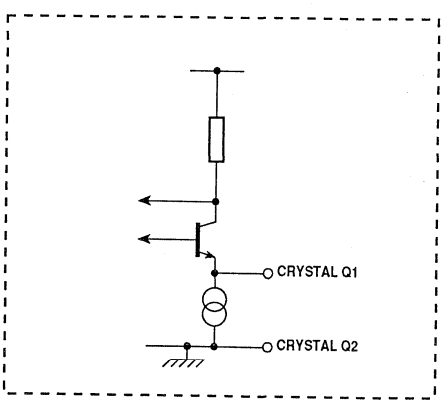
Loop amplifier



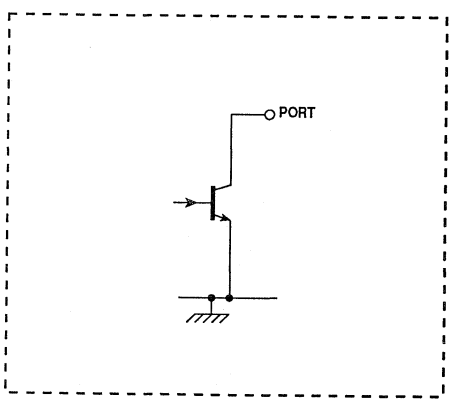
Ports P3 - P7



SCL and SDA inputs



Reference oscillator



Ports P0-P2 (P0 and P1 not present on SP5512S)

Fig. 6 SP5512 input/output interface circuits

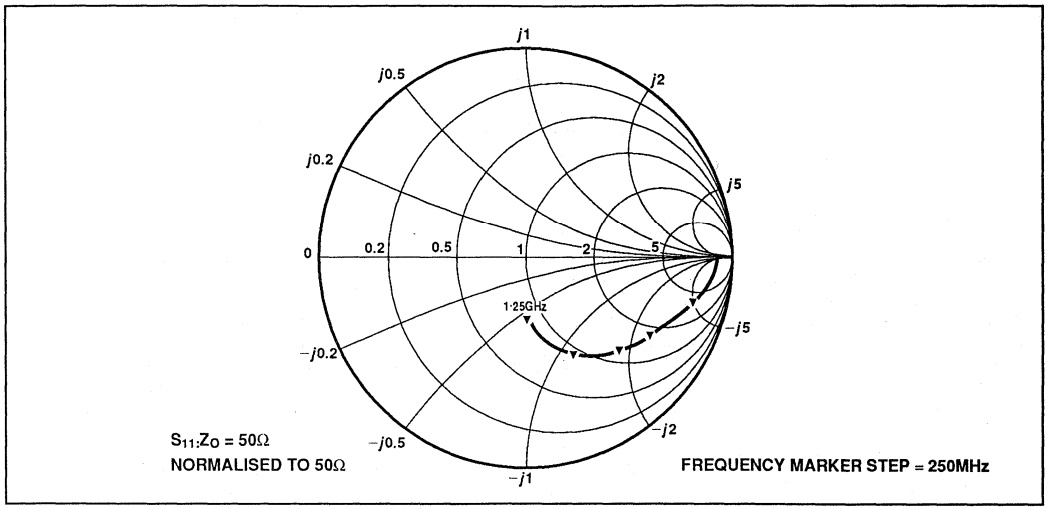


Fig. 7 Typical input impedance, SP5512

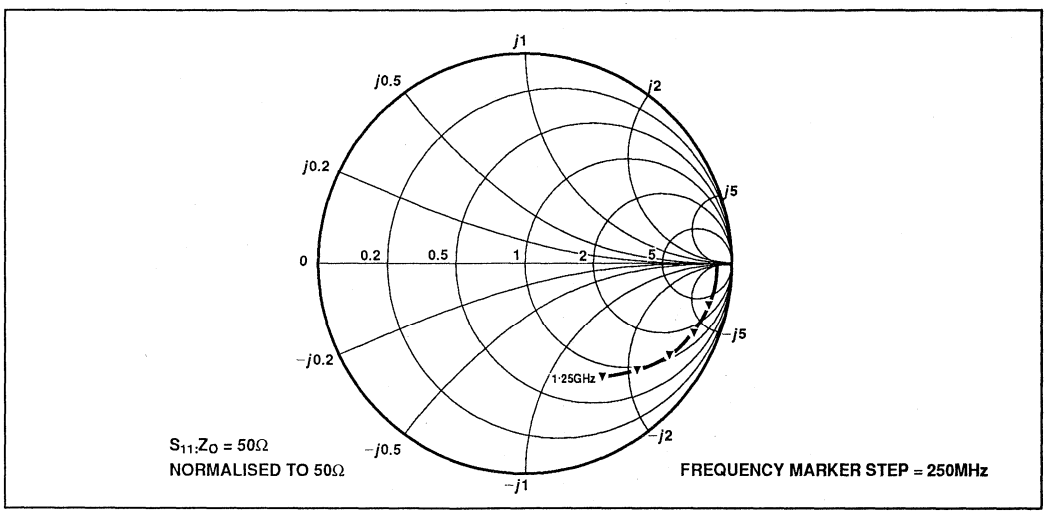


Fig. 8 Typical input impedance, SP5512S and SP5512T

SP5514S

1·3 GHz I²C BUS CONTROLLED SYNTHESISER

The SP5514S is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format, at a maximum rate of 500kHz. The device has one addressable current-limited output port (P3) and four addressable open-collector ports (P4-P7). The SP5514S has one fixed I²C BUS address and three programmable addresses, allowing two or more synthesisers to be used in a system. The comparison frequency is 7·8125kHz , derived from a 4MHz crystal controlled oscillator.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I²C BUS
- Low Power Consumption (215mW Typ.)
- Low Radiation
- Varactor Drive Amp Disable
- 5 Controllable Outputs
- ESD Protection *
- 500kHz Clock Rate

* Normal ESD handling precautions should be observed.

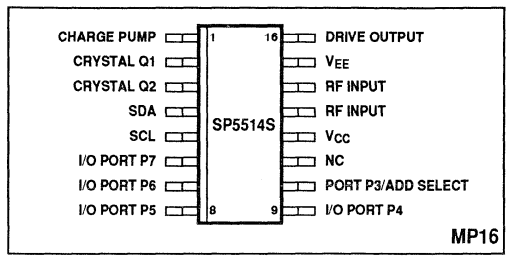


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5514S NA MP (16-lead miniature plastic package)

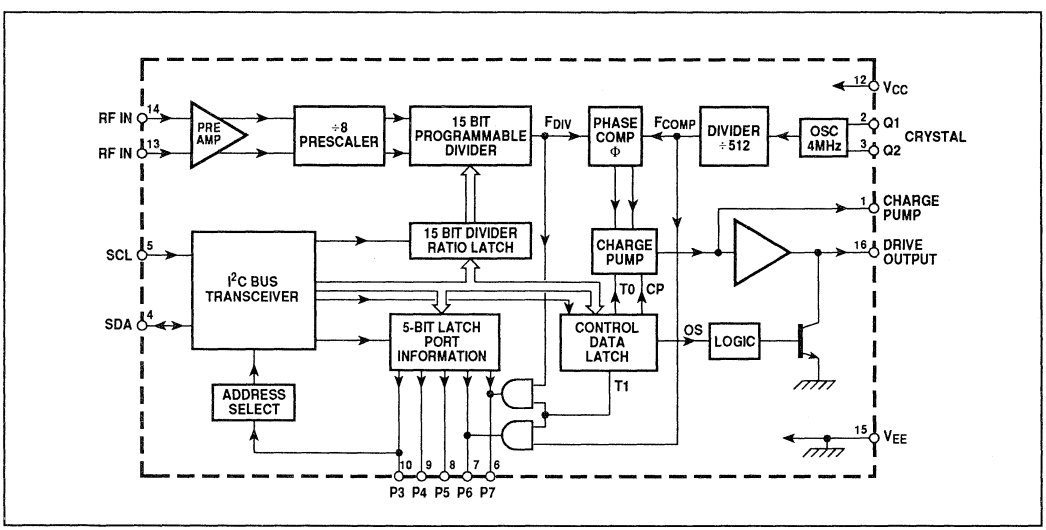


Fig. 2 Block diagram of SP5514S

ELECTRICAL CHARACTERISTICS

T_{AMB} = −10°C to +80°C, V_{CC} = +4·5V to +5·5V.
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		43	53	mA	V_{CC} = 5V
Prescaler input voltage	13,14	12·5		300	mVrms	50MHz to 1GHz
Prescaler input voltage		30		300	mVrms	1·3GHz, see Fig. 5
Prescaler input impedance	13,14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		5·5	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			−10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
SCL clock rate	5			0·5	MHz	
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±1	µA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500				V pin 16 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 1)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator source impedance	2		−400		Ω	Nominal spread = ±15%
Output Ports						
P3 sink current	10	0·7	1	1·5	mA	V_{OUT} = 12V
P3 leakage current	10			10	µA	V_{OUT} = 13·2V
P4-P7 sink current	6-9	10			mA	V_{OUT} = 0·7V
P4-P7 leakage current	6-9			10	µA	V_{OUT} = 13·2V
Input Port						
P3 input current high	10			+10	µA	V pin 10 = 5·5V
P3 input current low	10			−10	µA	V pin 10 = 0V

NOTE 1. Maximum resistance quoted refers to all conditions, including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	14	−0·3	7	V	
RF input voltage	13,14		2·5	V p-p	
Port voltage	6-10	−0·3	14	V	Port in off state
	6-9	−0·3	6	V	Port in on state
	10	−0·3	14	V	Port in on state
Total port output current	6-10		50	mA	
RF input DC offset	13-14	−0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	−0·3	V_{CC}+0·3	V	
Drive output DC offset	16	−0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	−0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	−0·3	V_{CC}+0·3	V	With V_{CC} applied
		−0·3	5·5	V	V_{CC} not applied
Storage temperature		−55	+150	°C	
Junction temperature			+150	°C	
Thermal resistance, chip-to-ambient			111	°C/W	
Thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5·5V			321	mW	

FUNCTIONAL DESCRIPTION

The SP5510 is programmed from an I²C BUS. The data is fed in on the SDA line and clock on the SCL line as dictated by the I²C Bus format at an increased clock rate of 0·5MHz. The Tables in Fig. 3 illustrate the format of the data in write mode. The device can be programmed to respond to several addresses, which allows the use of more than one synthesiser in an I²C BUS system. Table 2 shows how the address is selected by applying a voltage to P3. The LSB of the address Byte (R/$\overline{W}$) must be set to 0 for correct write operation. When the SP5514S receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as Byte 2 or 4, a logic 0 for Byte 2, frequency information and a logic 1 for Byte 4, control information. Byte 2 must be followed by Byte 3 or STOP; similarly, Byte 5 follows Byte 4. Until an I²C stop condition is recognised, additional data bytes can be entered without the need to re-address the device. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (e.g., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig. 6.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the 7·8125kHz reference obtained by dividing the output of the 4MHz crystal oscillator by 512.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170μA and a logic 0 for ±50μA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7.

Byte 5 programs the output ports P3-P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

When any of the optional address are used, P3 must be programmed in its high impedance state.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 7.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	X	X	X	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ to 13·2V

Table 2 Address selection

A : Acknowledge bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6, P5, P4, P3 : Control output port states
X : Don't care

Fig. 3 Data formats

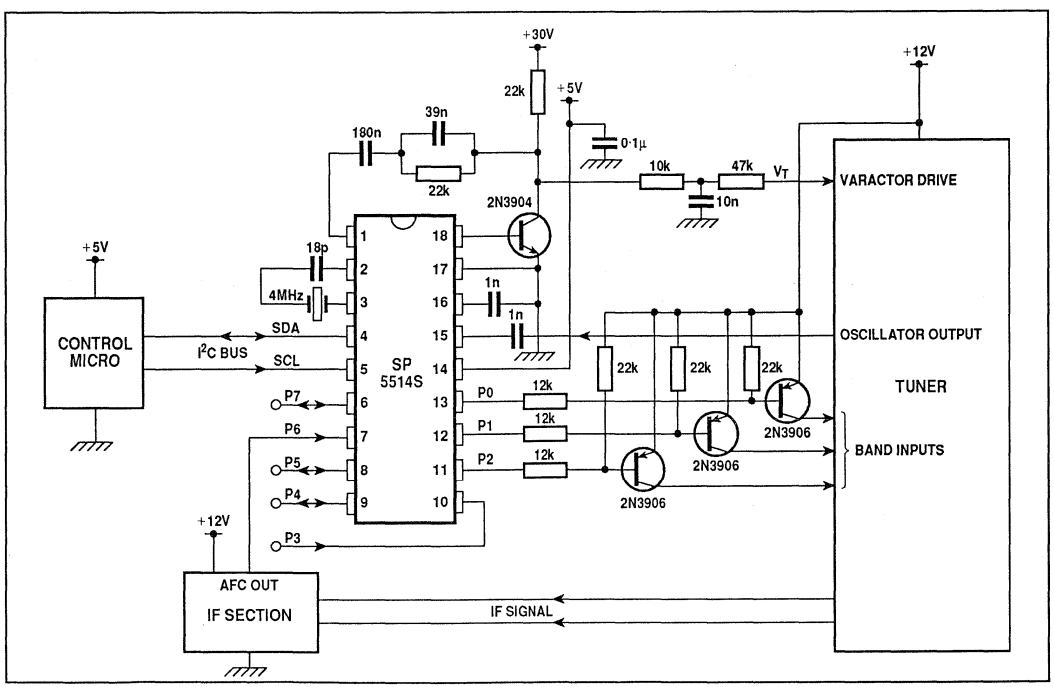


Fig. 4 Typical application

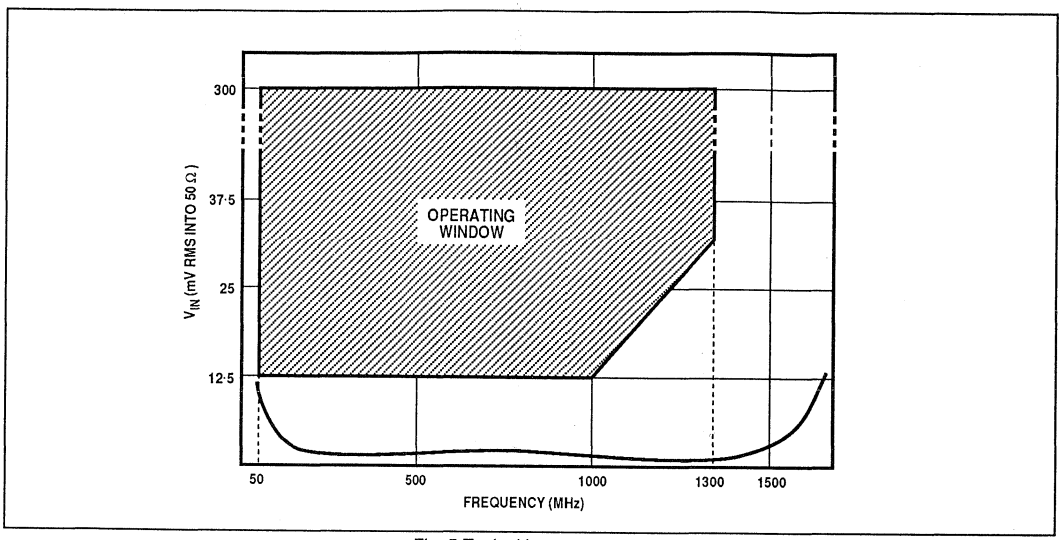


Fig. 5 Typical input sensitivity

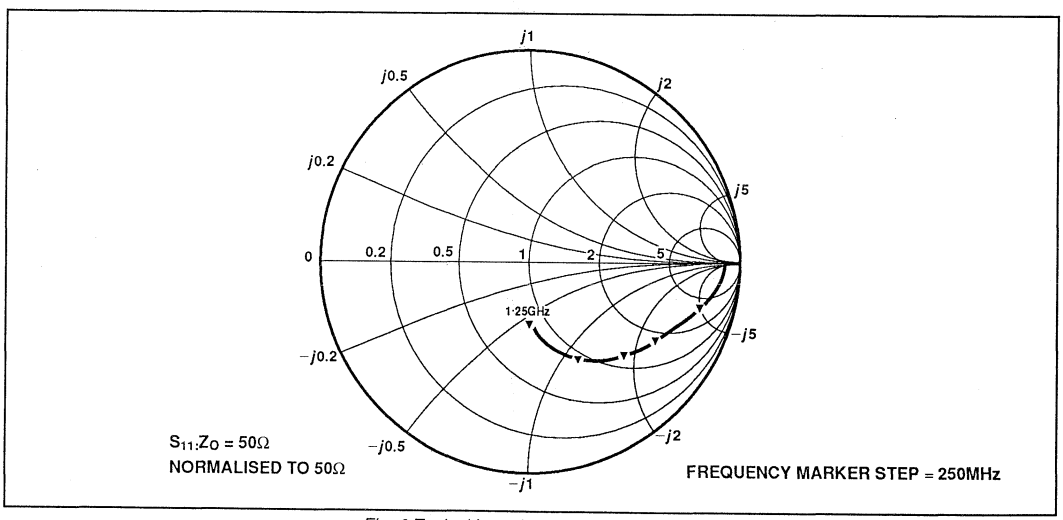


Fig. 6 Typical input impedance, SP5514S

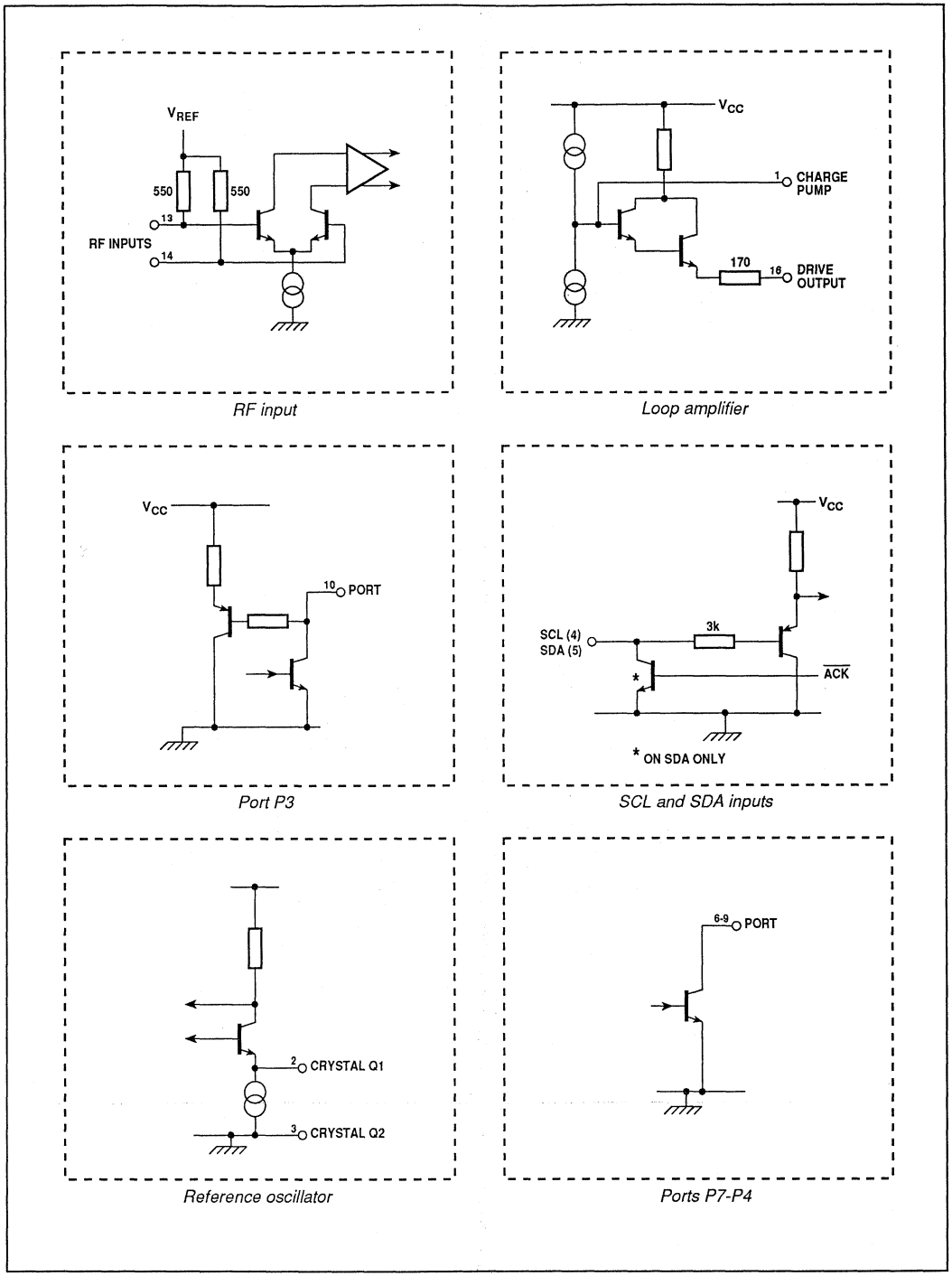


Fig. 7 SP5514S input/output interface circuits

SP5524

1·3 GHz BIDIRECTIONAL I^2C BUS CONTROLLED SYNTHESISER

The SP5524 is a single-chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I^2C BUS format. The device has six controllable open-collector output ports (P0-P3, P6 and P7), each capable of sinking 10mA. In addition, P1 is a 3-bit 5-level ADC input. The information on these ports can be read via the I^2C BUS.

The device has one fixed I^2C BUS address and three programmable addresses, allowing two or more synthesisers to be used in a system.

FEATURES

- Complete 1·3GHz Single Chip System
- Programmable via the I^2C BUS
- Low Power Consumption (215mW Typ.)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bi-directional
- 5-Level ADC
- Variable I^2C BUS Address for Picture in Picture TV
- ESD Protection *

* Normal ESD handling precautions should be observed.

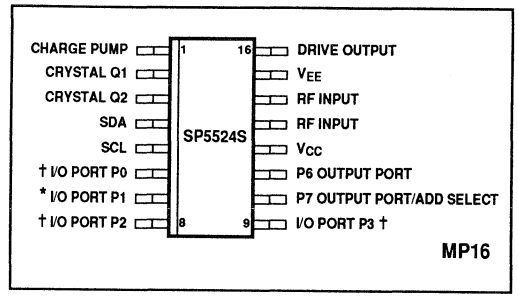


Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV when Combined with SP4902 2·5GHz Prescaler
- Cable Tuning Systems
- VCRs

ORDERING INFORMATION

SP5524S KG MPAS (Tubes)
SP5524S KG MPAD (Tape and Reel)

ELECTRICAL CHARACTERISTICS

T_{AMB} = -10°C to +80°C, V_{CC} = +4·5V to +5·5V.
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		43	53	mA	V_{CC} = 5V
Prescaler input voltage	13,14	12·5		300	mVrms	100MHz to 1GHz
		30		300	mVrms	50MHz and 1·3GHz, see Fig. 5
Prescaler input impedance	13,14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4,5	3		5·5	V	
Input low voltage	4,5	0		1·5	V	
Input high current	4,5			10	µA	Input voltage = V_{CC}
Input low current	4,5			-10	µA	Input voltage = 0V
Leakage current	4,5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0·4	V	Sink current = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500			µA	V pin 16 = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	Parallel resonant crystal (note 2)
Crystal oscillator drive level			40		mV p-p	
Crystal oscillator source impedance	2		-400		Ω	Nominal spread = ±15%
Output Ports						
P0-P3, P6, P7 sink current (see note 1)	6-11	10			mA	V_{OUT} = 0·7V, see note 1
P0-P3, P6, P7 leakage current (see note 1)	6-11			10	µA	V_{OUT} = 13·2V
Input Ports						
P7 input current high	10			+10	µA	V pin 10 = 13·2V
P7 input current low	10			-10	µA	V pin 10 = 0V
P0, P2, P3 input voltage low	6,8,9			0·8	V	
P0, P2, P3 input voltage high	6,8,9	2·7			V	
P1 input current high	7			+10	µA	See Table 3 for ADC levels
P1 input current low	7			-10	µA	

NOTES
1. Source impedance between all output ports and ground is approximately 5Ω. This should be taken into account when calculating output port saturation voltages.
2. The recommended crystal series resistance quoted refers to all conditions including start-up.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	12	-0·3	6	V	
RF input voltage	13,14		2·5	V p-p	
Port voltage	6-11	-0·3	14	V	Port in off state
	6-11	-0·3	6	V	Port in on state
Total port output current	6-11		50	mA	
RF input DC offset	13-14	-0·3	V_{CC}+0·3	V	
Charge pump DC offset	1	-0·3	V_{CC}+0·3	V	
Drive output DC offset	16	-0·3	V_{CC}+0·3	V	
Crystal oscillator DC offset	2	-0·3	V_{CC}+0·3	V	
SDA, SCL input voltage	4,5	-0·3	V_{CC}+0·3	V	With V_{CC} applied
		-0·3	5·5	V	V_{CC} not applied
Storage temperature		-55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip-to-ambient			111	°C/W	
MP16 thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5·5V			321	mW	

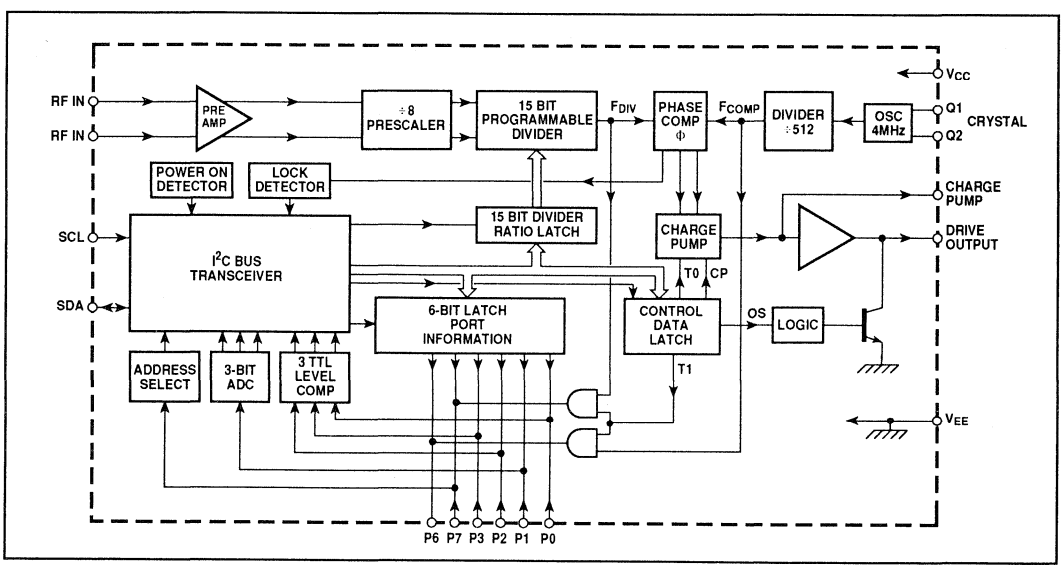


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5524 is programmed from an I^2C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I^2C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I^2C BUS system. Table 4 shows how the address is selected by applying a voltage to P7. The LSB of the address byte (R/$\overline{W}$) sets the device into read mode if it is high and write mode if it is low. When the SP5524 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5524 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2+3 select the synthesised frequency while Bytes 4+5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as Byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I^2C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (e.g., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from Bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-8 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-chip 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of Byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170μA and a logic 0 for ±50μA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of Byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of Byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{COMP} to P6 and F_{DIV} to P7.

Byte 5 programs the output ports P0-P3, P6 and P7, a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power on reset indicator and is set to a logic 1 if the power supply to the device has dropped below a nominal 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P0, P2 and P3 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic1). These inputs will then respond to data complying with standard TTL voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5-level ADC.

The 5-level ADC can be used to feed AFC information to the microprocessor from the IF section of the television, as illustrated in Fig. 4.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	X	X	P3	P2	P1	P0	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format

A2	A1	A0	Voltage input to P1
1	0	0	$0{\cdot}6V_{CC}$ to 13·2V
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0V to $0{\cdot}15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P7
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ to 13·2V

Table 4 Address selection

A : Acknowledge bit
MA1, MA0 : Variable address bits (see Table 4)
CP : Charge Pump current select
T1 : Test mode selection
T0 : Charge pump disable
OS : Varactor drive Output disable Switch
P7, P6 : Control output port states
P3, P2, P1, P0
POR : Power On Reset indicator
FL : Phase lock detect flag
I2, I1, I0 : Digital information from ports P0, P2 and P3 respectively
A2, A1, A0 : 5-level ADC data from P1 (see Table 3)
X : Don't care

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

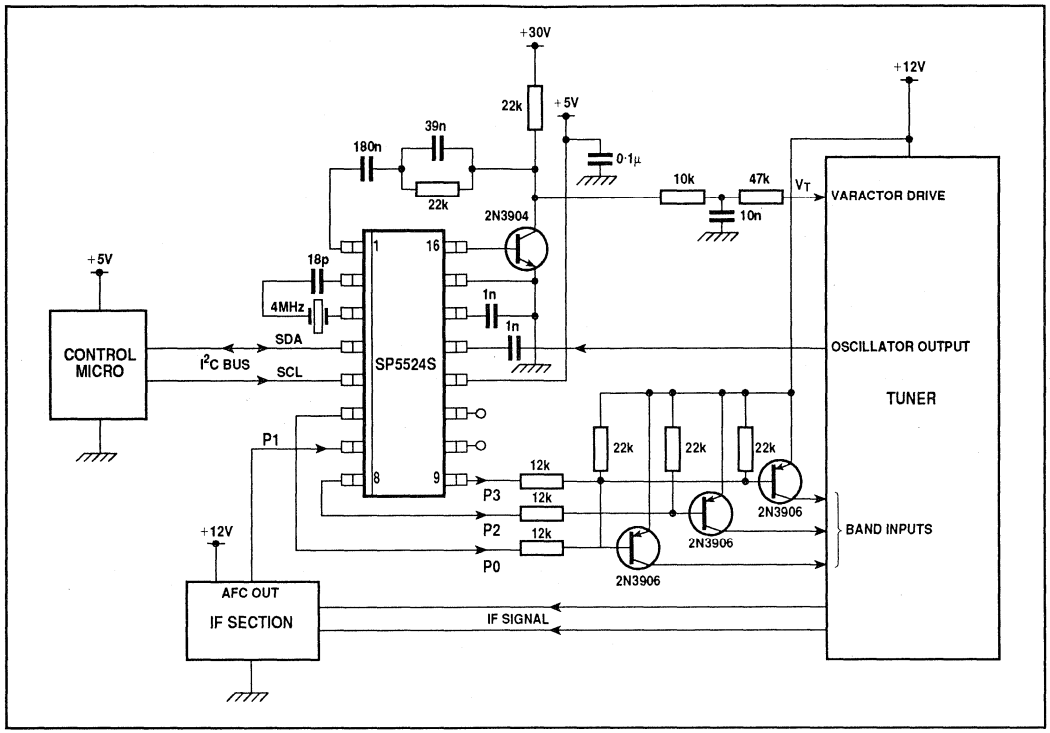


Fig. 4 Typical application

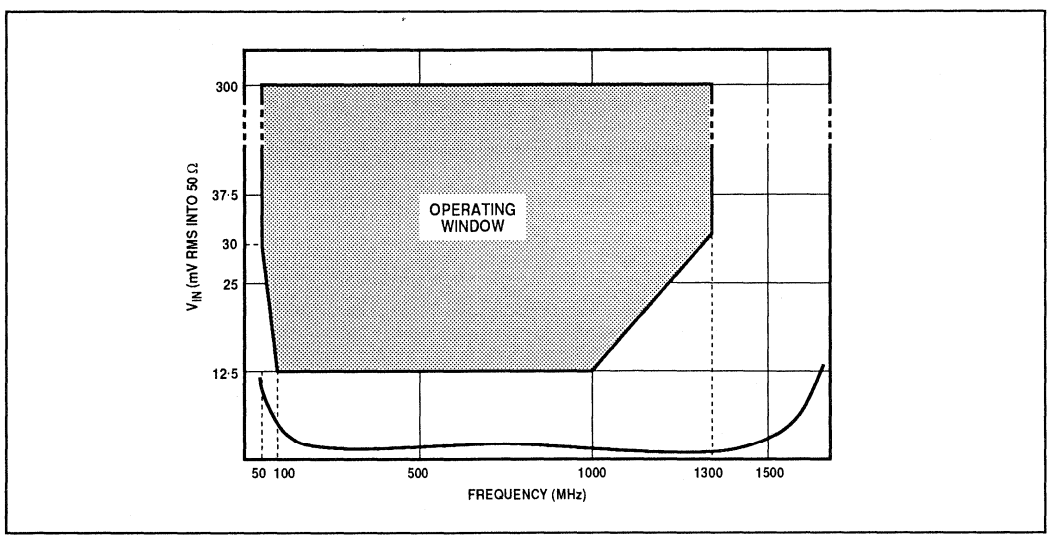
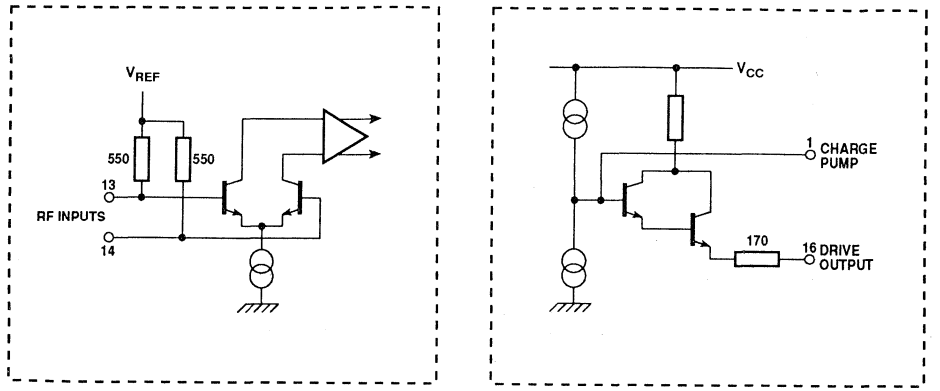
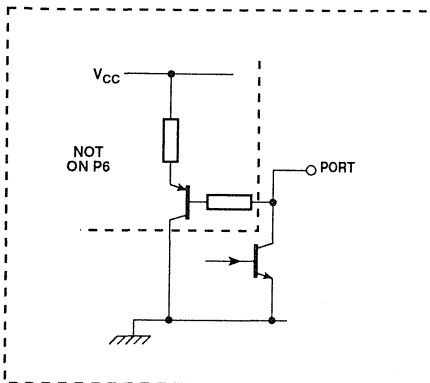


Fig. 5 Typical input sensitivity

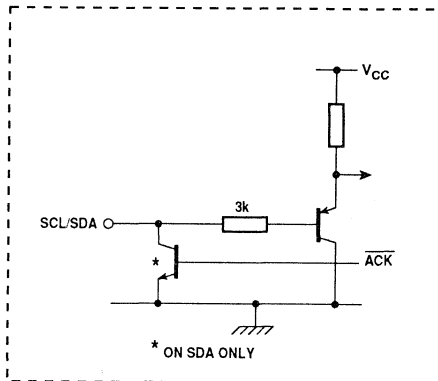


RF input

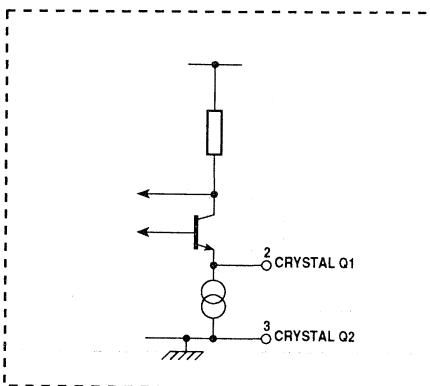
Loop amplifier



Ports P0 - P3, P6 and P7



SCL and SDA inputs



Reference oscillator

Fig. 6 Input/output interface circuits

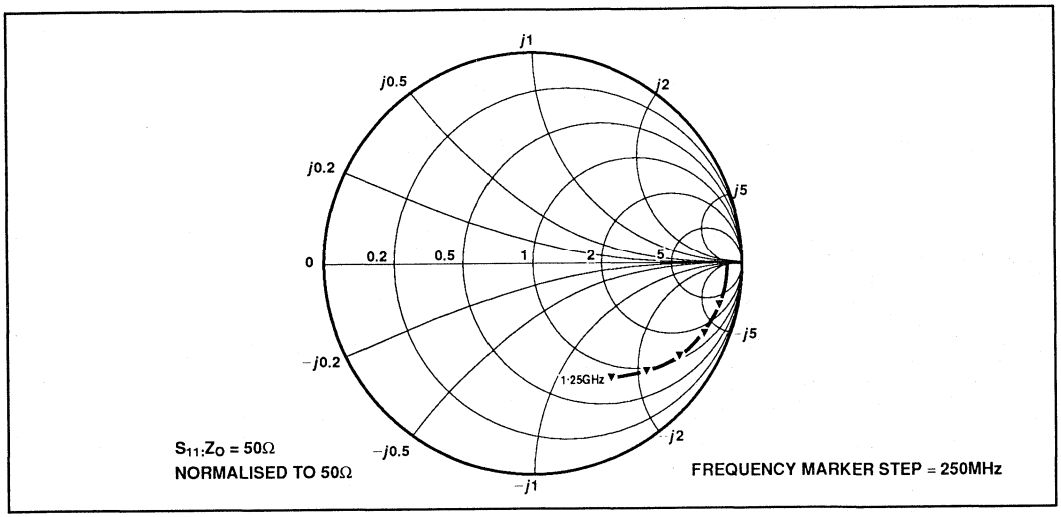


Fig. 7 Typical input impedance

SP5610

1.3GHz BI–DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

The SP5610 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 4 addressable current limited outputs and 4 addressable bi–directional open collector ports one of which is a 3 bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

The device is available in two variants: the SP5610 in 18–lead plastic DIL (DP18) and the SP5610S in 16–lead miniature plastic (MP16). See features below for functional differences between the devices.

FEATURES

- Complete 1.3GHz Single Chip System
- High Sensitivity RF Inputs
- Programmable via I²C Bus
- On–Chip Oscillator with 1kΩ Source Impedance
- Low power consumption (5V 20mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 8 Controllable Outputs, 4 Bi–Directional (SP5610)
- 5 Controllable Outputs, 4 Bi–Directional (SP5610S)
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- ESD Protection *
- Switchable ÷512/1024 Reference Divider
- Pin and Function Compatible with SP5510/SP5510S †

* Normal ESD handling procedures should be observed.

† The SP5510/SP5510S does not have a switchable reference division ratio.

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz prescaler
- Cable Tuning Systems
- VCR's

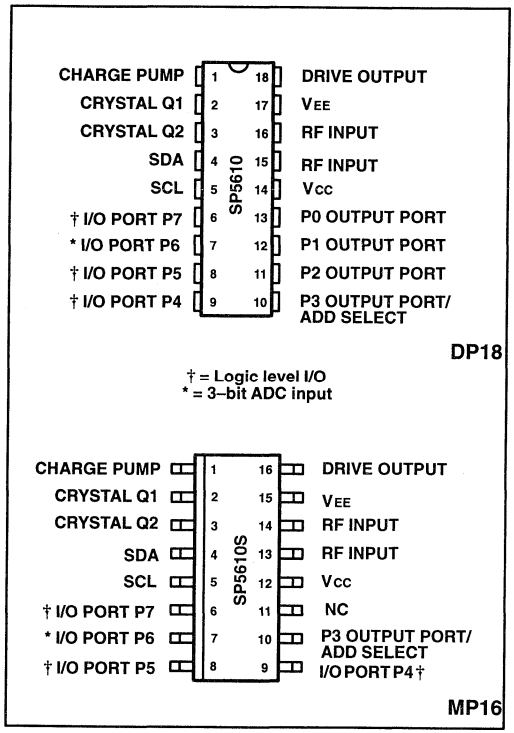


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SP5610/KG/DPAS
SP5610S/KG/MPAS (Tubes)
SP5610S/KG/MPAD (Tape and Reel)

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}= +4.5V to +5.5V.
All pin connections refer to DP package
These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		20	27	mA	V_{CC} = 4.5V to 5.5V
Prescaler Input Voltage	15, 16	12.5		300	mV_{rms}	50MHz to 1.3GHz sinewave See Fig. 5.
Prescaler Input Impedance Input Capacitance	15, 16		50 2		Ω pF	
SDA, SCL Input High Voltage Input Low Voltage Input High Current Input Low Current Leakage Current	4, 5 4, 5 4, 5 4, 5 4, 5	3 0		5.5 1.5 10 –10 10	V V µA µA µA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output Voltage	4			0.4	V	I_{sink} = 3mA
Charge Pump Current Low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge Pump Current High	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge Pump Output Leakage Current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge Pump Drive Output Current	18	500			µA	V_{pin} 18 = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended Crystal series Resistance		10		200	Ω	"Parallel Resonant" crystal. Resistance specified is max under all conditions
Crystal Oscillator Drive Level	2		80		mVp–p	
Crystal Oscillator Source Impedance	2		–1		kΩ	Nominal Spread ±15%
External Reference Input Frequency	2	2		8	MHz	AC coupled sinewave
External Reference Input Amplitude	2	70		200	mVrms	AC coupled sinewave
Output Ports						
P0–P3 Sink Current*	13 – 10	0.7	1	1.5	mA	V_{out} = 12V
P0–P3 Leakage Current*	13 – 10			10	µA	V_{out} = 13.2V
P4–P7 Sink Current	9–6	10			mA	V_{out} = 0.7V
P4–P7 Leakage Current	9–6			10	µA	V_{out} = 13.2V
Input Ports						
P3 Input Current High	10			+10	µA	$V_{pin\ 10}$ = 13.2V
P3 Input Current Low	10			–10	µA	$V_{pin\ 10}$ = 0V
P4,P5,P7 Input Voltage Low	9,8,6			0.8	V	
P4,P5,P7 Input Voltage High	9,8,6	2.7			V	
P6 Input Current High	7			+10	µA	See Table 3 for ADC Levels
P6 Input Current Low	7			–10	µA	

* Ports P0 – P2 not present on the SP5610S

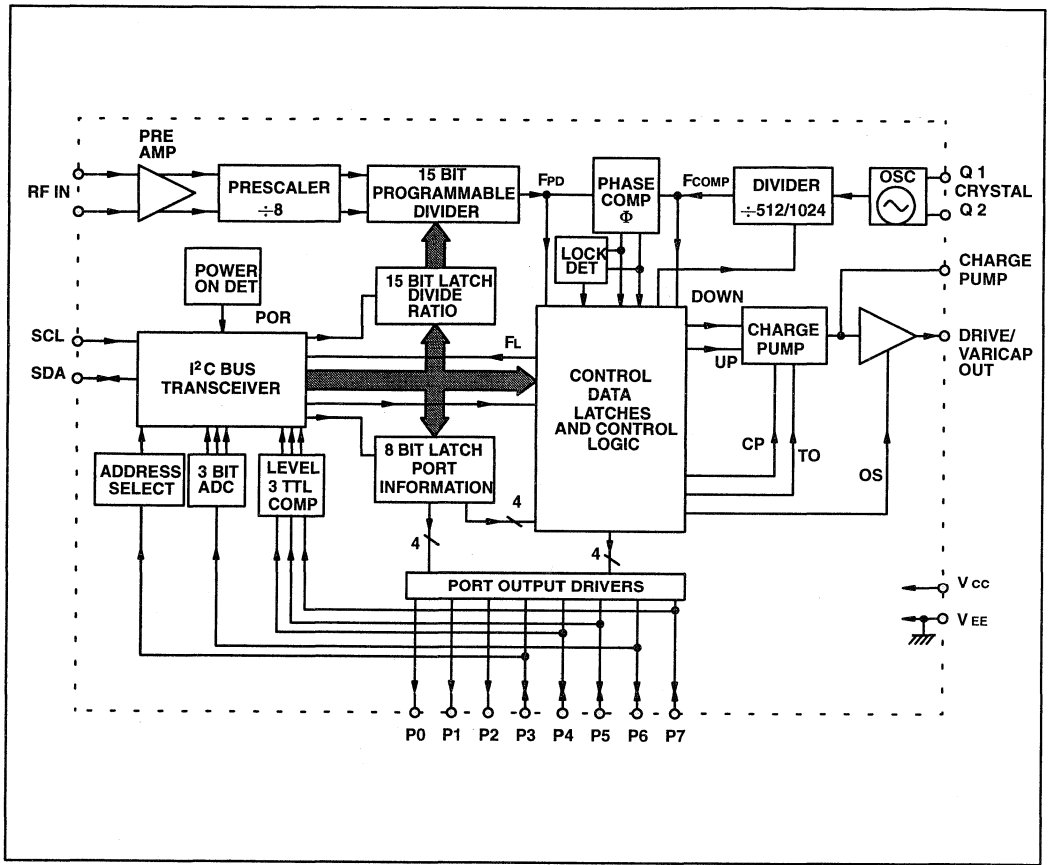


Fig 2. Block diagram (ports P0–P2 not available on SP5610S)

FUNCTIONAL DESCRIPTION

The SP5610 is programmed from an I²C Bus. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 4 shows how the address is selected by applying a voltage to P3. When the device receives a correct address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are programmed. When the device is programmed into the read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

WRITE MODE (Frequency Synthesis)

When the device is in write mode bytes 2+3 select the synthesised frequency, while bytes 4+5 control the output port states, charge pump, reference divider ratio and various test modes.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for frequency information and a logic 1 for control and output port information. When byte 2 is received the device always expects byte 3 next. Similarly, when byte 4 is received the device expects byte 5 next. Additional data bytes can be entered without the need to re–address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid–byte (e.g. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15–bit register and is used to control the division ratio of the 15–bit programmable divider. This is preceded by a divide–by–8 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP} .

When frequency data is entered, the phase comparator, via a charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2, or provided by an on–board crystal controlled oscillator. The comparison frequency F_{COMP} is derived from the reference frequency via the reference divider. The reference divider division ratio is switchable from 512 to 1024, and is controlled by bit 7 of byte 4 (TS0); a logic 1 for 512; a logic 0 for 1024. The SP5610 differs from the SP5510 in this respect, only 512 being available on the SP5510. Note, the comparison frequency is 7.8125kHz when a 4MHz reference is used, and divide by 512 is selected.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170μA and a logic 0 for ±50μA allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. When the device is 'frequency locked' the charge pump current is internally set to ±50μA regardless of CP.

Bit 4 of byte 4 (T0) disables the charge pump when it is set to a logic 1.

Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1.

Bit 3 of byte 4 (T1) enables various test modes when set high. These modes are selected by bits 5, 6, 7 of byte 4 (TS2, TS1, TS0) as detailed in Table 5. When T1 is set low TS2 and TS1 are assigned a 'don't care' condition, and TS0 selects the reference divider ratio as previously described.

Byte 5 programs the output ports P0 to P7; a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ MODE

When the device is in read mode the status byte read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power–on reset indicator and is set to a logic 1 if the V_{CC} supply to the device has dropped below 3V (at 25°C), e.g. when the device is initially turned on. The POR is reset to 0 when the read sequence is terminated by a stop command. When POR is set high (at low V_{CC}), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked, and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels.

Bits 6, 7 and 8 (A2, A1, A0) combine to give the output of the 5 level ADC. The ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6. The SP5610 is function and pin equivalent to the SP5510 device apart from the switchable reference divider, and has much lower power dissipation, improved RF sensitivity and better ESD performance.

MSB								LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	Byte 1
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	Byte 2
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	Byte 3
CONTROL DATA	1	CP	T1	T0	TS2	TS1	TS0	OS	A	Byte 4
IO PORT CONTROL DATA	P7	P6	P5	P4	P3	P2*	P1*	P0*	A	Byte 5

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	Byte 1
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	Byte 2

Table 2 Read data format (MSB is transmitted first)

A:	Acknowledge bit
MA1, MA0:	Variable address bits (see Table 4)
CP:	Charge pump current select
T1:	Test mode enable
T0:	Charge pump disable
TS2, TS1, TS0:	Operation mode control bits (see Table 5)
OS:	Varactor drive Output disable Switch
P7,P6,P5,P4,P3,P2*,P1*,P0:	Control output states
POR:	Power On Reset indicator
FL:	Phase Lock detect Flag
I2, I1, I0:	Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0:	5 Level ADC data from P6 (see Table 3)

* = Don't care condition on SP5610S

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 - 0.2V_{CC}$
0	1	ALWAYS VALID
1	0	$0.3 - 0.7V_{CC}$
1	1	$0.8V_{CC} - 13.2V$

Table 4 Address selection

T1	TS2	TS1	TS0	OPERATION MODE DESCRIPTION
0	d	d	0	Normal operation, test modes disabled, reference divider ratio=1024
0	d	d	1	Normal operation, test modes disabled, reference divider ratio=512
1	0	0	d	Charge pump down. Status byte bit FL set to 0
1	0	1	d	Charge pump up. Status byte bit FL set to 1
1	1	0	0	Ports P4,P5,P6,P7 set to state d
1	1	0	1	Port P7=$F_{PD}/2$; P4,P5,P6 set to state d
1	1	1	d	Port P7=F_{PD}; P6=F_{COMP}; P4, P5 set to state d

d=don't care

Table 5 Operation modes

Fig. 3 Data formats

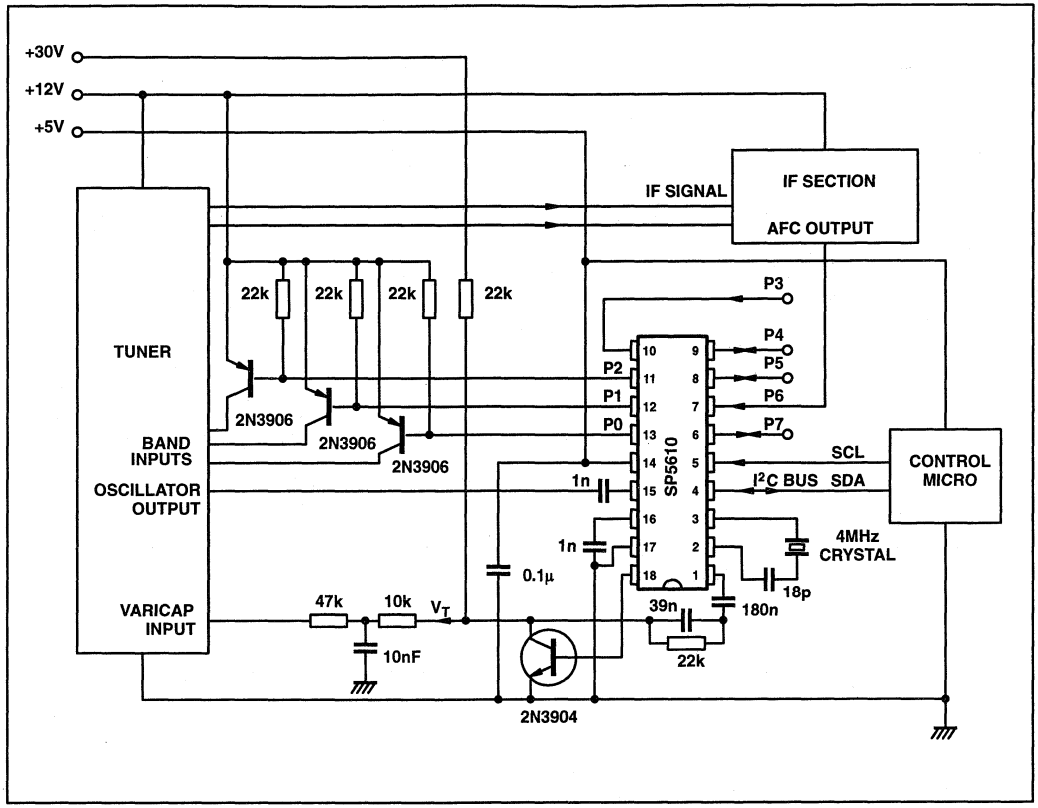


Fig. 4 Typical application

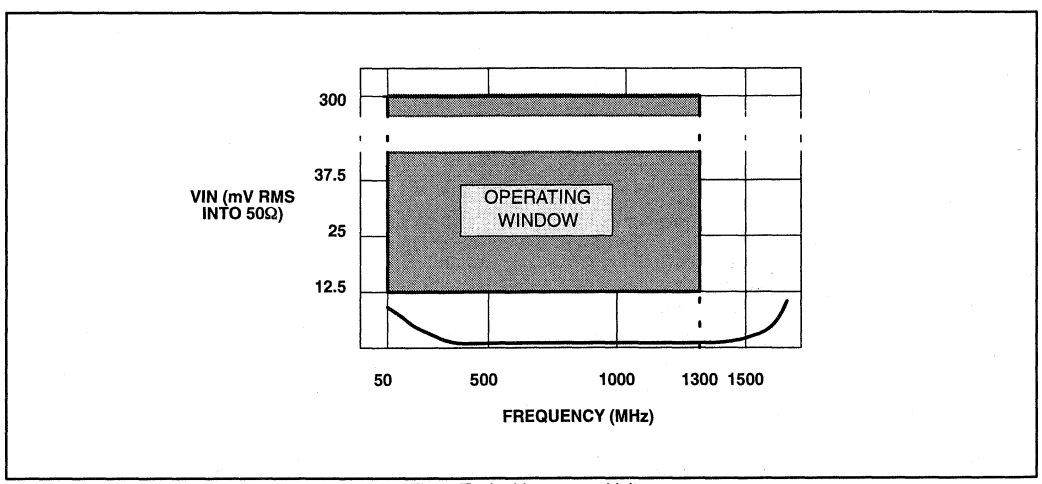


Fig. 5 Typical input sensitivity

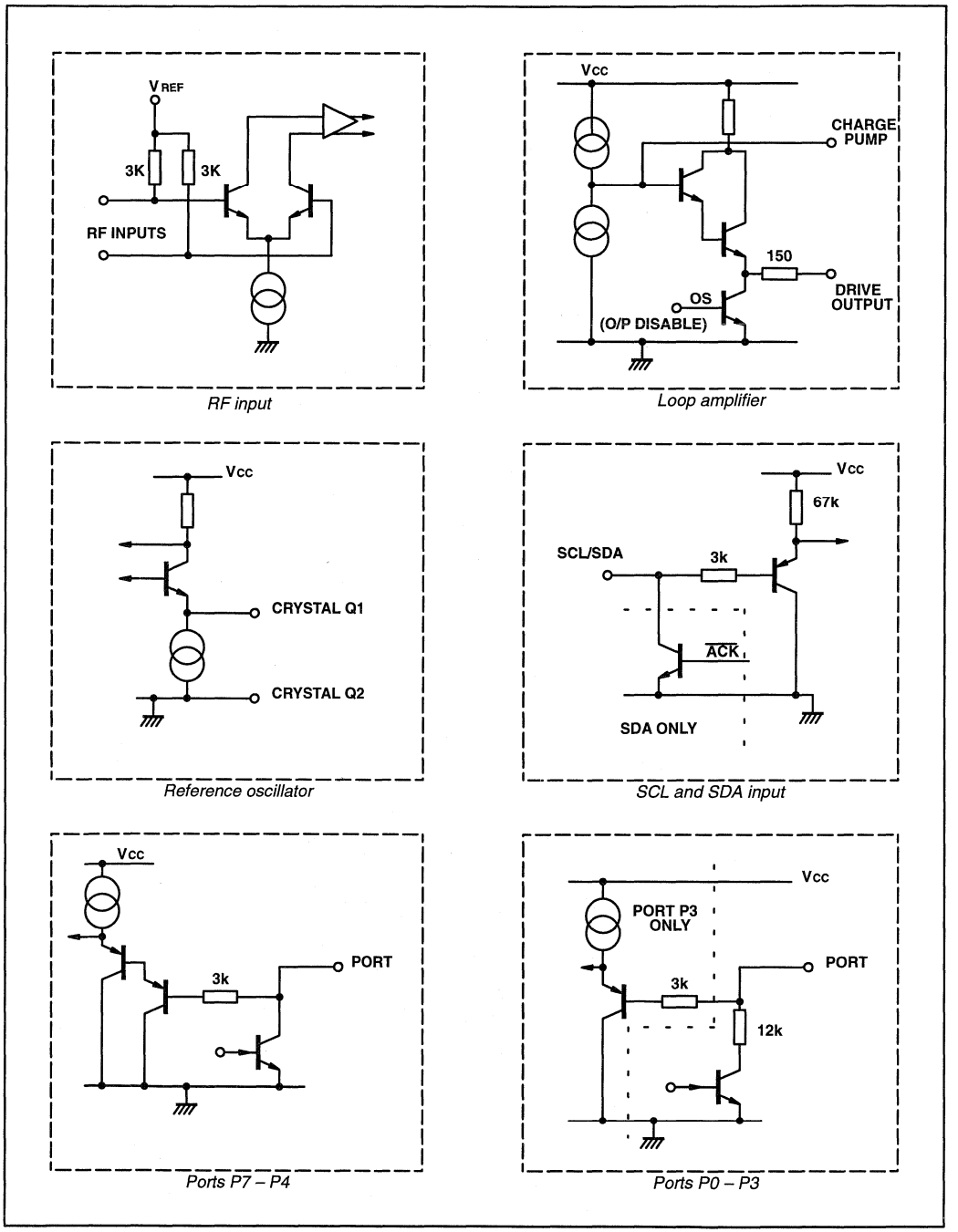


Fig. 6 Input/output interface circuits

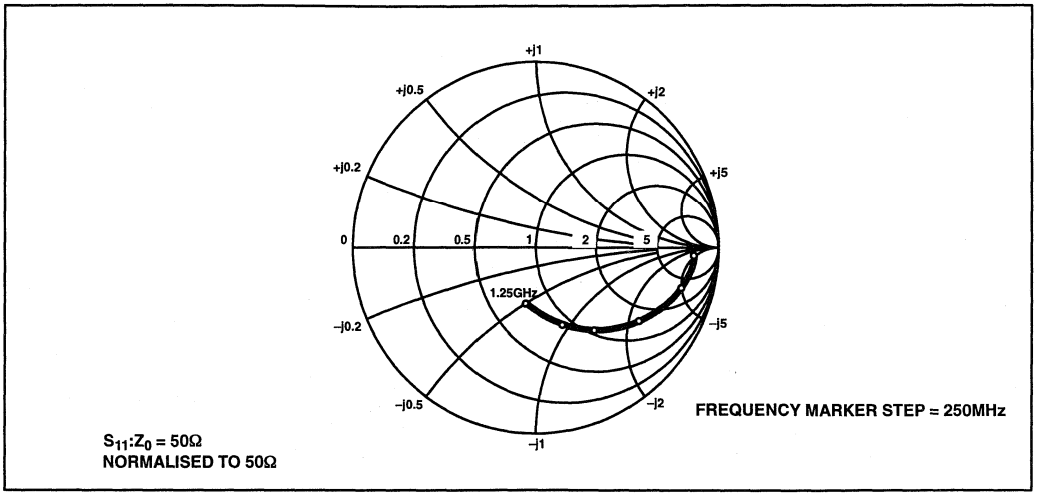


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin SP5610	Pin SP5610S	Value		Units	Conditions
			Min	Max		
Supply voltage	14	12	– 0.3	7	V	
RF input voltage	15, 16	13, 14		2.5	Vp–p	
Port voltage	6–13 6–9 10–13	6–10 6–9 10	– 0.3 – 0.3 – 0.3	14 6 14	V V V	Port in off state Port in on state Port in on state
Total port output current	6–13	6–10		50	mA	
RF input DC offset	15, 16	13, 14	– 0.3	V_{CC} +0.3	V	
Charge Pump DC offset	1	1	– 0.3	V_{CC}+0.3	V	
Drive DC offset	18	16	– 0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	2	– 0.3	V_{CC}+0.3	V	
SDA,SCL input voltage	4, 5	4, 5	– 0.3	6	V	
Storage temperature			– 55	+150	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip–to–ambient				78	°C/W	
DP 18 thermal resistance, chip–to–case				24	°C/W	
MP16 thermal resistance, chip–to–ambient				111	°C/W	
MP16 thermal resistance, chip–to–case				41	°C/W	
Power consumption at 5.5V				150	mW	All ports off
ESD protection	ALL	ALL	3		kV	Mil STD 883 TM 3015–7

SP5611

1.3GHz BI–DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

(Supersedes July 1993 Edition)

The SP5611 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 3 addressable current limited outputs (P0–P2) and 4 addressable bi–directional open collector ports (P4–P7) one of which is a 3 bit ADC. The information on these ports can be read via the I²C BUS. The SP5611S is a variant in a 16 lead miniature plastic package, without P0–P2, but identical in other respects to the SP5611. Each device has 4 programmable I²C BUS addresses, programmed by applying a specific input voltage to the P3 address select input. This enables 2 or more synthesisers to be used in a system.

FEATURES

- Complete 1.3GHz Single chip System
- High Sensitivity RF Inputs
- Programmable via I²C Bus
- On chip oscillator with 1kΩ source impedance
- Low power consumption (5V, 20mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 7 Controllable Outputs, 4 Bi–Directional (SP5611)
- 4 Bi–Directional Controllable Outputs (SP5611S)
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- ESD Protection *
- Switchable ÷512/1024 Reference Divider
- Pin and Function Compatible with SP5511/SP5511S †

* Normal ESD handling procedures should be observed.

† The SP5511/SP5511S does not have a switchable reference division ratio.

APPLICATIONS

- Satellite TV when combined with SP4902 2.5GHz prescaler
- Cable Tuning Systems
- VCR's

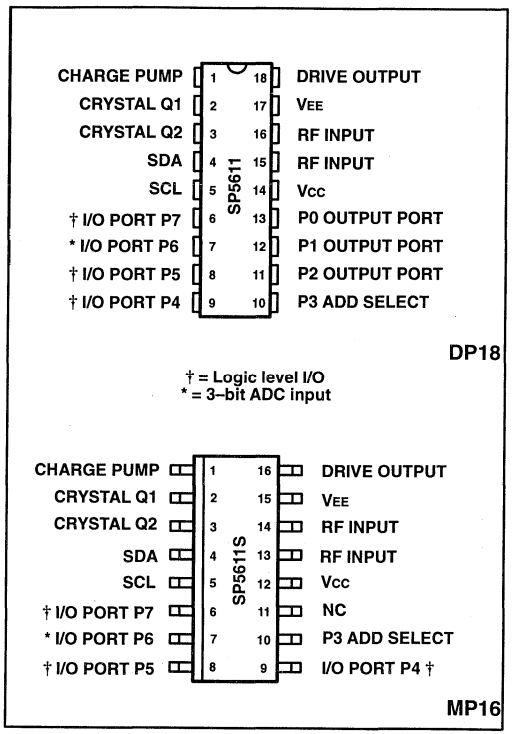


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SP5611/KG/DPAS
SP5611S/KG/MPAS (Tubes)
SP5611S/KG/MPAD (Tape and Reel)

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}= +4.5V to +5.5V.
All pin connections refer to DP package
These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	14		20	27	mA	V_{CC} = 4.5V to 5.5V
Prescaler Input Voltage	15, 16	12.5		300	mV_{rms}	50MHz to 1.3GHz sinewave See Fig. 5.
Prescaler Input Impedance Input Capacitance	15, 16		50 2		Ω pF	
SDA, SCL Input High Voltage Input Low Voltage Input High Current Input Low Current Leakage Current	4, 5 4, 5 4, 5 4, 5 4, 5	3 0		5.5 1.5 10 –10 10	V V µA µA µA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output Voltage	4			0.4	V	I_{sink} = 3mA
Charge Pump Current Low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge Pump Current High	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge Pump Output Leakage Current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge Pump Drive Output Current	18	500			µA	V_{pin} 18 = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended Crystal series Resistance		10		200	Ω	"Parallel Resonant" crystal. Resistance specified is max under all conditions
Crystal Oscillator Drive Level	2		80		mVp–p	
Crystal Oscillator Source Impedance	2		–1		kΩ	Nominal Spread ±15%
External Reference Input Frequency	2	2		8	MHz	AC coupled sinewave
External Reference Input amplitude	2	70		200	mVrms	AC coupled sinewave
Output Ports						
P0–P2 Sink Current*	13 – 11	0.7	1	1.5	mA	V_{out} = 12V
P0–P2 Leakage Current*	13 – 11			10	µA	V_{out} = 13.2V
P4–P7 Sink Current	9–6	10			mA	V_{out} = 0.7V
P4–P7 Leakage Current	9–6			10	µA	V_{out} = 13.2V
Input Ports						
P3 Input Current High	10			1	mA	$V_{pin\ 10} = V_{cc}$
P3 Input Current Low	10			–0.5	mA	$V_{pin\ 10}$ = 0V
P4,P5,P7 Input Voltage Low	9,8,6			0.8	V	
P4,P5,P7 Input Voltage High	9,8,6	2.7			V	
P6 Input Current High	7			+10	µA	See Table 3 for ADC Levels
P6 Input Current Low	7			–10	µA	

* Ports P0 – P2 not present on the SP5611S

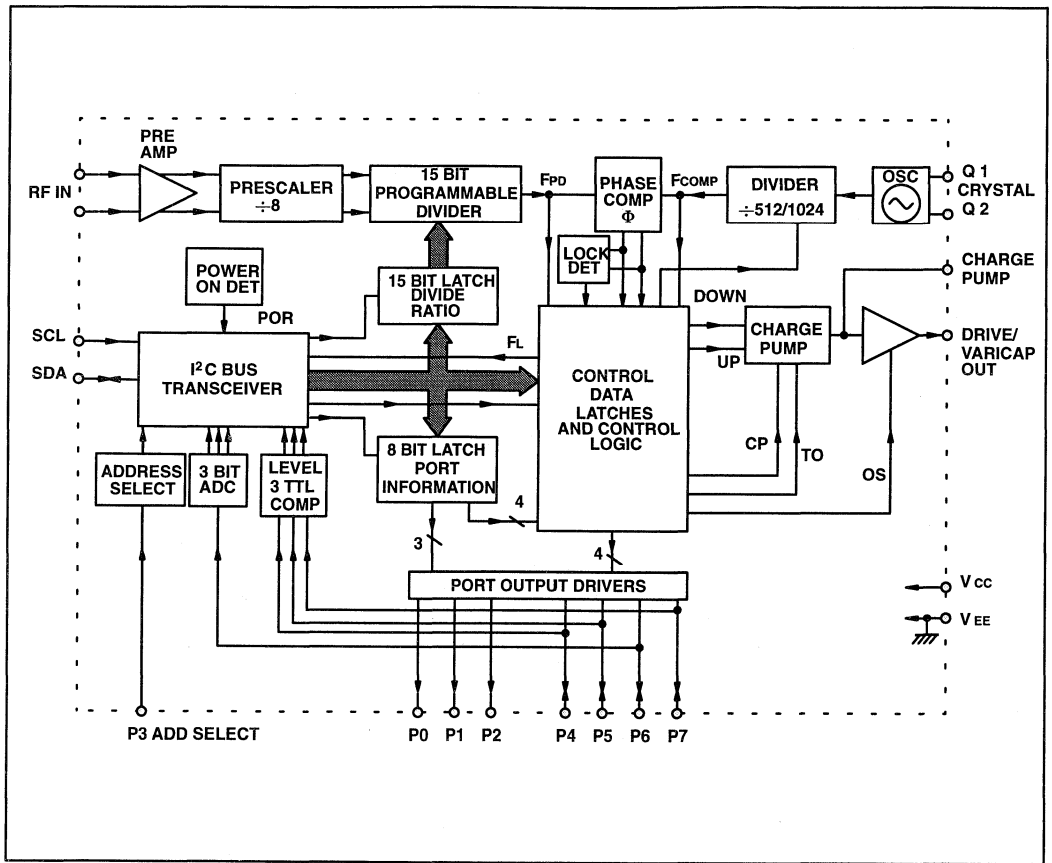


Fig 2. Block diagram (ports P0–P2 not available on SP5611S)

FUNCTIONAL DESCRIPTION

The SP5611 is programmed from an I²C Bus. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 4 shows how the address is selected by applying a voltage to P3. When the device receives a correct address byte it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes, are programmed. When the device is programmed into the read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

WRITE MODE (Frequency Synthesis)

When the device is in write mode bytes 2+3 select the synthesised frequency, while bytes 4+5 control the output port states, charge pump, reference divider ratio and various test modes.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for frequency information and a logic 1 for control and output port information. When byte 2 is received the device always expects byte 3 next. Similarly, when byte 4 is received the device expects byte 5 next. Additional data bytes can be entered without the need to re–address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid–byte (e.g. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15–bit register and is used to control the division ratio of the 15–bit programmable divider. This is preceded by a divide–by–8 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 8 times the comparison frequency F_{COMP} .

When frequency data is entered, the phase comparator, via a charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2, or provided by an on–board crystal controlled oscillator. The comparison frequency F_{COMP} is derived from the reference frequency via the reference divider. The reference divider division ratio is switchable from 512 to 1024, and is controlled by bit 7 of byte 4 (TS0); a logic 1 for 512; a logic 0 for 1024. The SP5611 differs from the SP5511 in this respect, only 512 being available on the SP5511. Note, the comparison frequency is 7.8125kHz when a 4MHz reference is used, and divide by 512 is selected.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170μA and a logic 0 for ±50μA allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. When the device is 'frequency locked' the charge pump current is internally set to ±50μA regardless of CP.

Bit 4 of byte 4 (T0) disables the charge pump when it is set to a logic 1.

Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1.

Bit 3 of byte 4 (T1) enables various test modes when set high. These modes are selected by bits 5, 6, 7 of byte 4 (TS2 TS1, TS0) as detailed in Table 5. When T1 is set low, TS2 and TS1 are assigned a 'don't care' condition, and TS0 selects the reference divider ratio as previously described.

Byte 5 programs the output ports P0 to P7; a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ MODE

When the device is in read mode the status byte read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power–on reset indicator and is set to a logic 1 if the V_{CC} supply to the device has dropped below 3V (at 25°C), e.g. when the device is initially turned on. The POR is reset to 0 when the read sequence is terminated by a stop command. When POR is set high (at low V_{CC}), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked, and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels.

Bits 6, 7 and 8 (A2, A1, A0) combine to give the output of the 5 level ADC. The ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6. The SP5611 is function and pin equivalent to the SP5511 device apart from the switchable reference divider, and has much lower power dissipation, improved RF sensitivity and better ESD performance.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	Byte 1
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	Byte 2
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	Byte 3
CONTROL DATA	1	CP	T1	T0	TS2	TS1	TS0	OS	A	Byte 4
IO PORT CONTROL DATA	P7	P6	P5	P4	d	P2*	P1*	P0*	A	Byte 5

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	Byte 1
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	Byte 2

Table 2 Read data format (MSB is transmitted first)

A:	Acknowledge bit
MA1, MA0:	Variable address bits (see Table 4)
CP:	Charge pump current select
T1:	Operation mode enable
T0:	Charge pump disable
TS2, TS1, TS0:	Operation mode control bits (see Table 5)
OS:	Varactor drive Output disable Switch
P7,P6,P5,P4,P2*,P1*,P0*:	Control output states
POR:	Power On Reset indicator
FL:	Phase Lock detect Flag
I2, I1, I0:	Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0:	5 Level ADC data from P6 (see Table 3)

* = Don't care condition on SP5611S d=don't care

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 3 ADC levels

MA1	MA0	Address select input voltage
0	0	0 – 0.1 V_{CC}
0	1	OPEN CIRCUIT
1	0	$0.4V_{CC}$–$0.6V_{CC}$
1	1	$0.9V_{CC}$–V_{CC}

Table 4 Address selection

T1	TS2	TS1	TS0	OPERATION MODE DESCRIPTION
0	d	d	0	Normal operation, test modes disabled, reference divider ratio=1024
0	d	d	1	Normal operation, test modes disabled, reference divider ratio=512
1	0	0	d	Charge pump down. Status byte bit FL set to 0
1	0	1	d	Charge pump up. Status byte bit FL set to 1
1	1	0	0	Ports P4,P5,P6,P7 set to state d
1	1	0	1	Port P7=F_{PD}/2; P4,P5,P6 set to state d
1	1	1	d	Port P7=F_{PD}; P6=F_{COMP}; P4, P5 set to state d

d=don't care

Table 5 Operation modes

Fig. 3 Data formats

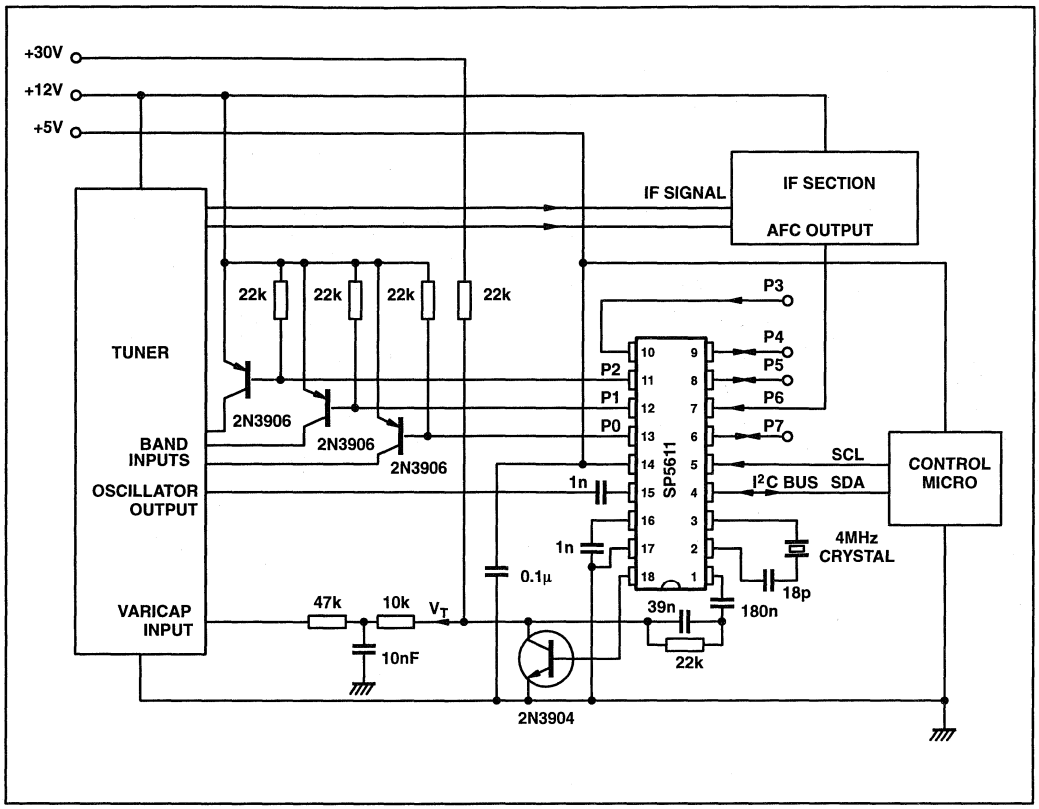


Fig. 4 Typical application

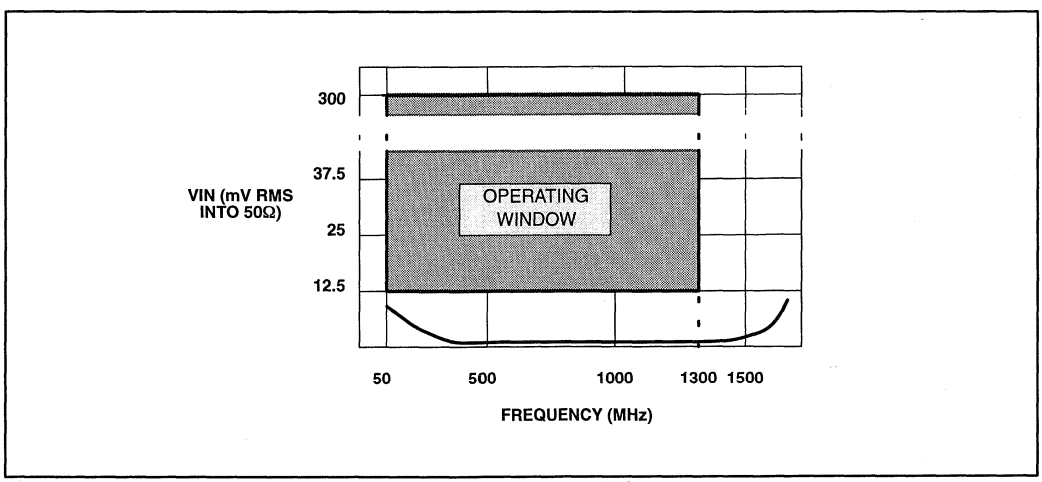


Fig. 5 Typical input sensitivity

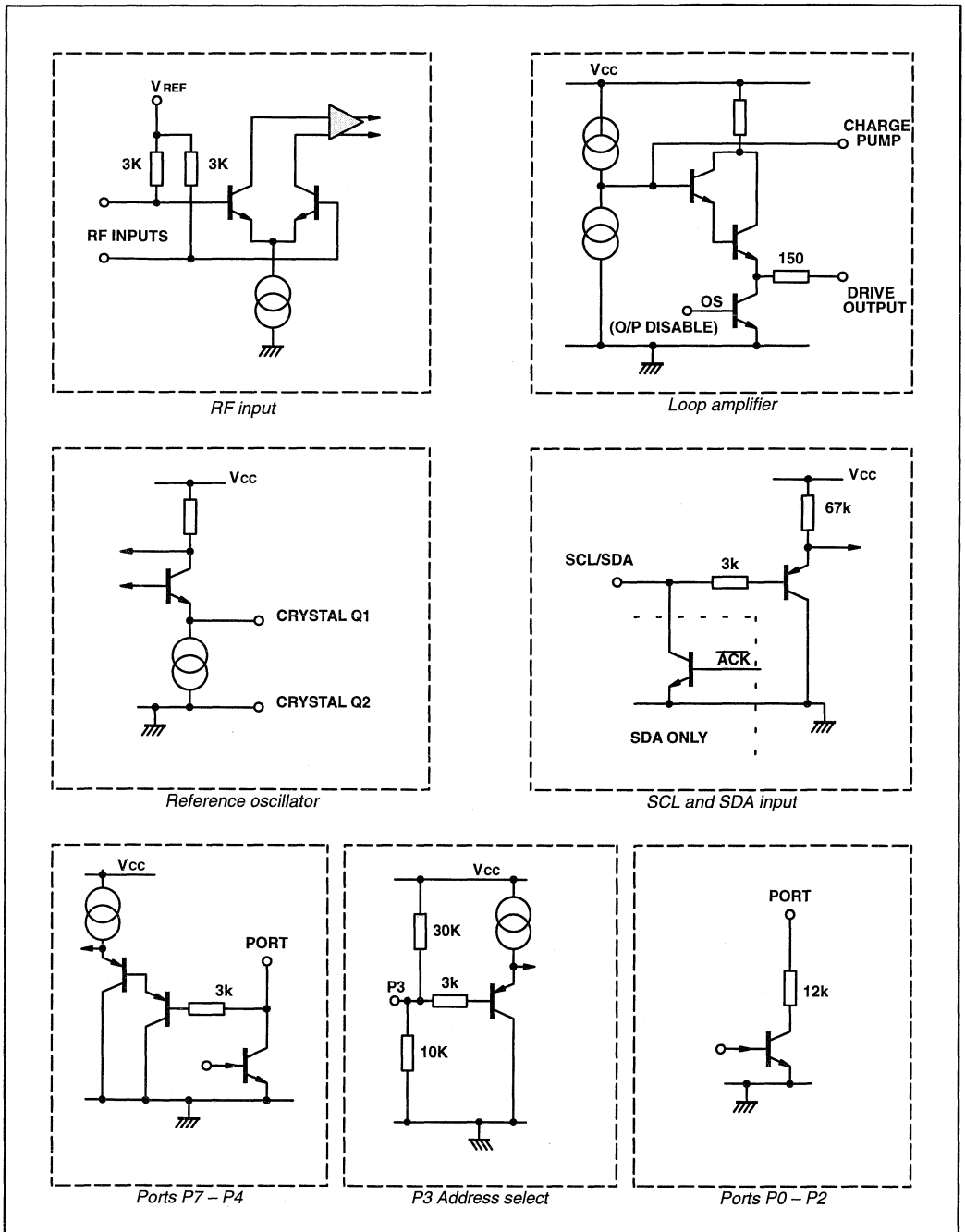


Fig. 6 Input/output interface circuits

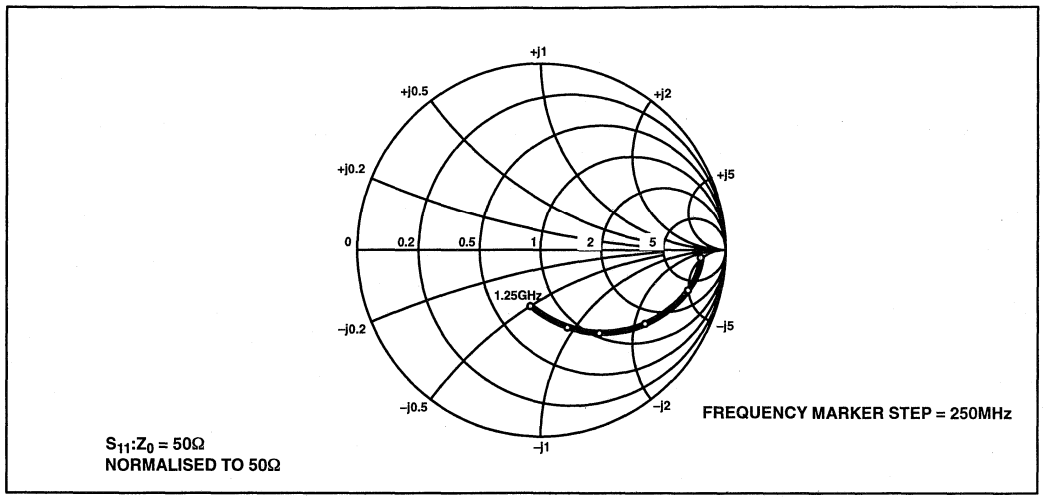


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin SP5611	Pin SP5611S	Value		Units	Conditions
			Min	Max		
Supply voltage	14	12	–0.3	7	V	
RF input voltage	15, 16	13, 14		2.5	Vp–p	
Port voltage	6–9,11–13 6–9 11–13	6–9 6–9 –	– 0.3 – 0.3 – 0.3	14 6 14	V V V	Port in off state Port in on state Port in on state
Total port output current	6–13	6–9		50	mA	
Add Select voltage	10	10	– 0.3	V_{CC}+0.3	V	
RF input DC offset	15, 16	13, 14	– 0.3	V_{CC} +0.3	V	
Charge Pump DC offset	1	1	– 0.3	V_{CC}+0.3	V	
Drive DC offset	18	16	– 0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	2	– 0.3	V_{CC}+0.3	V	
SDA,SCL input voltage	4, 5	4, 5	– 0.3	6	V	
Storage temperature			– 55	+150	°C	
Junction temperature				+150	°C	
DP18 thermal resistance, chip–to–ambient				78	°C/W	
DP 18 thermal resistance, chip–to–case				24	°C/W	
MP16 thermal resistance, chip–to–ambient				111	°C/W	
MP16 thermal resistance, chip–to–case				41	°C/W	
Power consumption at 5.5V				150	mW	All ports off
ESD protection	ALL	ALL	3		kV	MIL STD 883C TM 3015–7

SP5655

2.7GHz BI–DIRECTIONAL I²C BUS CONTROLLED SYNTHESISER

(Supersedes July 1993 Edition)

The SP5655 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 2 addressable current limited outputs and 4 addressable bi–directional open collector ports one of which is a 3 bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

FEATURES

- Complete 2.7GHz Single chip System
- High Sensitivity RF Inputs
- Programmable via I²C Bus
- On chip oscillator with 1kΩ source impedance
- Low power consumption (5V 30mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bi–Directional
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- ESD Protection *
- Switchable ÷512/1024 Reference Divider
- Pin and Function Compatible with SP5055S †

* Normal ESD handling procedures should be observed.

† The SP5055S does not have a switchable reference division ratio.

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

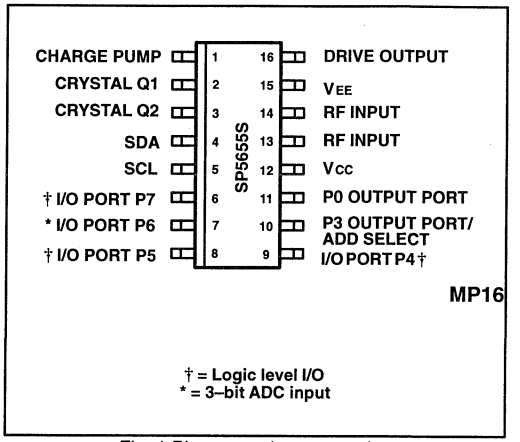


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SP5655S/KG/MPAS (Tubes)
SP5655S/KG/MPAD (Tape and Reel)

ELECTRICAL CHARACTERISTICS

T_{amb}= –20°C to +80°C, V_{CC}= +4.5V to +5.5V.
These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	12		30	40	mA	V_{CC} = 4.5V to 5.5V
Prescaler Input Voltage	13, 14	50		300	mV_{rms}	120MHz to 2.7GHz sinewave See Fig. 5.
Prescaler Input Impedance Input Capacitance	13, 14		50 2		Ω pF	
SDA, SCL Input High Voltage Input Low Voltage Input High Current Input Low Current Leakage Current	4, 5 4, 5 4, 5 4, 5 4, 5	3 0		5.5 1.5 10 –10 10	V V µA µA µA	 Input Voltage = V_{CC} Input Voltage = 0V When V_{CC} = 0V
SDA Output Voltage	4			0.4	V	I_{sink} = 3mA
Charge Pump Current Low	1		±50		µA	Byte 4 Bit 2 = 0, Pin 1 = 2V
Charge Pump Current High	1		±170		µA	Byte 4 Bit 2 = 1, Pin 1 = 2V
Charge Pump Output Leakage Current	1			±5	nA	Byte 4 Bit 4 = 1, Pin 1 = 2V
Charge Pump Drive Output Current	16	500			µA	V_{pin} 16 = 0.7V
Charge Pump Amplifier Gain			6400			
Recommended Crystal series Resistance		10		200	Ω	"Parallel Resonant" crystal. Resistance specified is max under all conditions
Crystal Oscillator Drive Level	2		80		mVp–p	
Crystal Oscillator Source Impedance	2		–1		kΩ	Nominal Spread ±15%
External Reference Input Frequency	2	2		8	MHz	AC coupled sinewave
External reference Input Amplitude	2	70		200	mVrms	AC coupled sinewave
Output Ports						
P0, P3 Sink Current	11 – 10	0.7	1	1.5	mA	V_{out} = 12V
P0, P3 Leakage Current	11 – 10			10	µA	V_{out} = 13.2V
P4–P7 Sink Current	9–6	10			mA	V_{out} = 0.7V
P4–P7 Leakage Current	9–6			10	µA	V_{out} = 13.2V
Input Ports						
P3 Input Current High	10			+10	µA	$V_{pin\ 10}$ = 13.2V
P3 Input Current Low	10			–10	µA	$V_{pin\ 10}$ = 0V
P4,P5,P7 Input Voltage Low	9,8,6			0.8	V	
P4,P5,P7 Input Voltage High	9,8,6	2.7			V	
P6 Input Current High	7			+10	µA	See Table 3 for ADC Levels
P6 Input Current Low	7			–10	µA	

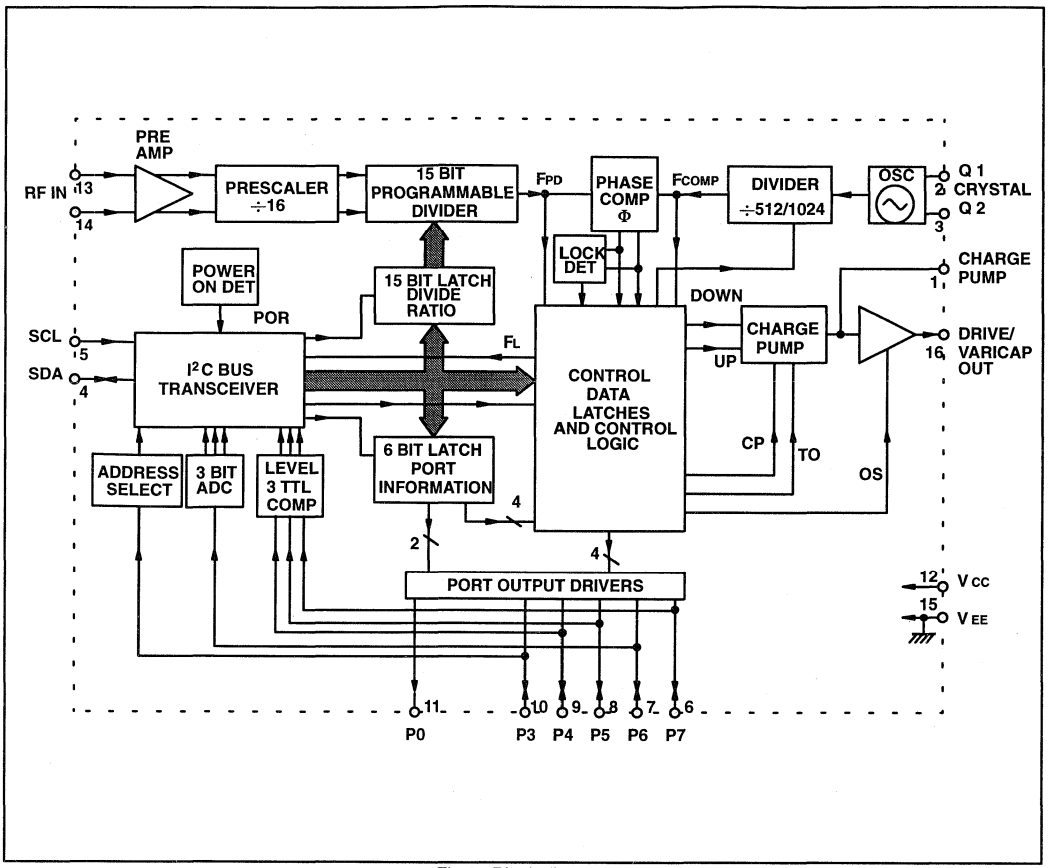


Fig 2. Block diagram

FUNCTIONAL DESCRIPTION

The SP5655 is programmed from an I²C Bus. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C Bus format. The synthesiser can either accept new data (write mode) or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low and read mode if it is high. The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 4 shows how the address is selected by applying a voltage to P3. When the device receives a correct address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are programmed. When the device is programmed into the read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

WRITE MODE (Frequency Synthesis)

When the device is in write mode bytes 2+3 select the synthesised frequency, while bytes 4+5 control the output port states, charge pump, reference divider ratio and various test modes.

Once the correct address is received and acknowledged, the first bit of the next byte determines whether that byte is interpreted as byte 2 or 4; a logic 0 for frequency information and a logic 1 for control and output port information. When byte 2 is received the device always expects byte 3 next. Similarly, when byte 4 is received the device expects byte 5 next. Additional data bytes can be entered without the need to re–address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid–byte (e.g. by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15–bit register and is used to control the division ratio of the 15–bit programmable divider. This is preceded by a divide–by–16 prescaler and amplifier to give excellent sensitivity at the local oscillator input, see Fig. 5. The input impedance is shown in Fig. 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{COMP}.

When frequency data is entered, the phase comparator, via a charge pump and varicap drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2, or provided by an on–board crystal controlled oscillator. The comparison frequency F_{COMP} is derived from the reference frequency via the reference divider. The reference divider division ratio is switchable from 512 to 1024, and is controlled by bit 7 of byte 4 (TS0); a logic 1 for 512; a logic 0 for 1024. The SP5655 differs from the SP5055 in this respect, only 512 being available on the SP5055. Note, the comparison frequency is 7.8125kHz when a 4MHz reference is used, and divide by 512 is selected.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170µA and a logic 0 for ±50µA allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. When the device is 'frequency locked' the charge pump current is internally set to ±50µA regardless of CP.

Bit 4 of byte 4 (T0) disables the charge pump when it is set to a logic 1.

Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1.

Bit 3 of byte 4 (T1) enables various test modes when set high. These modes are selected by bits 5, 6, 7 of byte 4 (TS2, TS1, TS0) as detailed in Table 5. When T1 is set low, TS2 and TS1 are assigned a 'don't care' condition, and TS0 selects the reference divider ratio as previously described.

Byte 5 programs the output ports P0, P3 to P7; a logic 0 for a high impedance output and a logic 1 for low impedance (on).

READ MODE

When the device is in read mode the status byte read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power–on reset indicator and is set to a logic 1 if the V_{CC} supply to the device has dropped below 3V (at 25°C), e.g. when the device is initially turned on. The POR is reset to 0 when the read sequence is terminated by a stop command. When POR is set high (at low V_{CC}), the programmed information is lost and the output ports are all set to high impedance.

Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked, and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2, I1, I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels.

Bits 6, 7 and 8 (A2, A1, A0) combine to give the output of the 5 level ADC. The ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6. The SP5655 is function and pin equivalent to the SP5055 device apart from the switchable reference divider, and has much lower power dissipation, improved RF sensitivity and better ESD performance.

	MSB							LSB		
ADDRESS	1	1	0	0	0	MA1	MA0	0	A	Byte 1
PROGRAMMABLE DIVIDER	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	Byte 2
PROGRAMMABLE DIVIDER	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	Byte 3
CONTROL DATA	1	CP	T1	T0	TS2	TS1	TS0	OS	A	Byte 4
IO PORT CONTROL DATA	P7	P6	P5	P4	P3	X	X	P0	A	Byte 5

Table 1 Write data format (MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	Byte 1
STATUS BYTE	POR	FL	I2	I1	I0	A2	A1	A0	A	Byte 2

Table 2 Read data format (MSB is transmitted first)

A:	Acknowledge bit
MA1, MA0:	Variable address bits (see Table 4)
CP:	Charge pump current select
T1:	Test mode enable
T0:	Charge pump disable
TS2, TS1, TS0:	Operation mode control bits (see Table 5)
OS:	Varactor drive Output disable Switch
P7,P6,P5,P4,P3,P0:	Control output states
POR:	Power On Reset indicator
FL:	Phase Lock detect Flag
I2, I1, I0:	Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0:	5 Level ADC data from P6 (see Table 3)
X	Don't care

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0.45V_{CC}$ to $0.6V_{CC}$
0	1	0	$0.3V_{CC}$ to $0.45V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	$0 - 0.2V_{CC}$
0	1	ALWAYS VALID
1	0	$0.3 - 0.7V_{CC}$
1	1	$0.8V_{CC} - 13.2V$

Table 4 Address selection

T1	TS2	TS1	TS0	OPERATION MODE DESCRIPTION
0	d	d	0	Normal operation, test modes disabled, reference divider ratio=1024
0	d	d	1	Normal operation, test modes disabled, reference divider ratio=512
1	0	0	d	Charge pump down. Status byte bit FL set to 0
1	0	1	d	Charge pump up. Status byte bit FL set to 1
1	1	0	0	Ports P4,P5,P6,P7 set to state d
1	1	0	1	Port P7=$F_{PD}/2$; P4,P5,P6 set to state d
1	1	1	d	Port P7=F_{PD}; P6=F_{COMP}; P4, P5 set to state d

d=don't care

Table 5 Operation modes

Fig. 3 Data formats

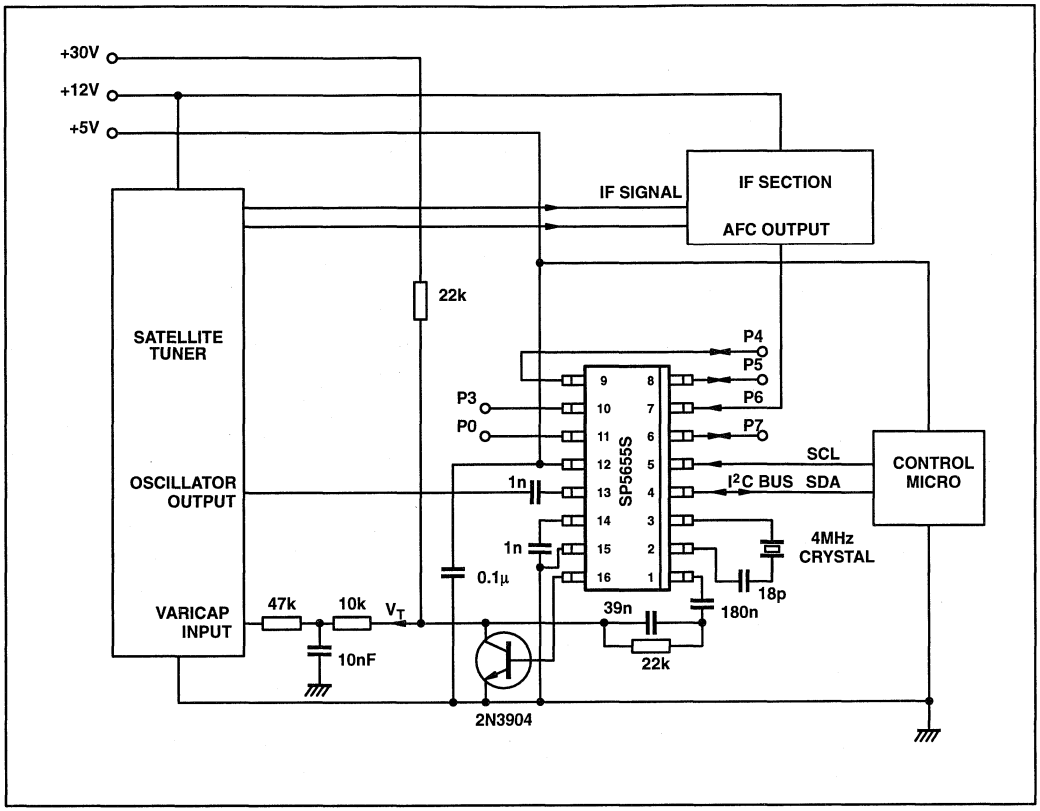


Fig. 4 Typical application

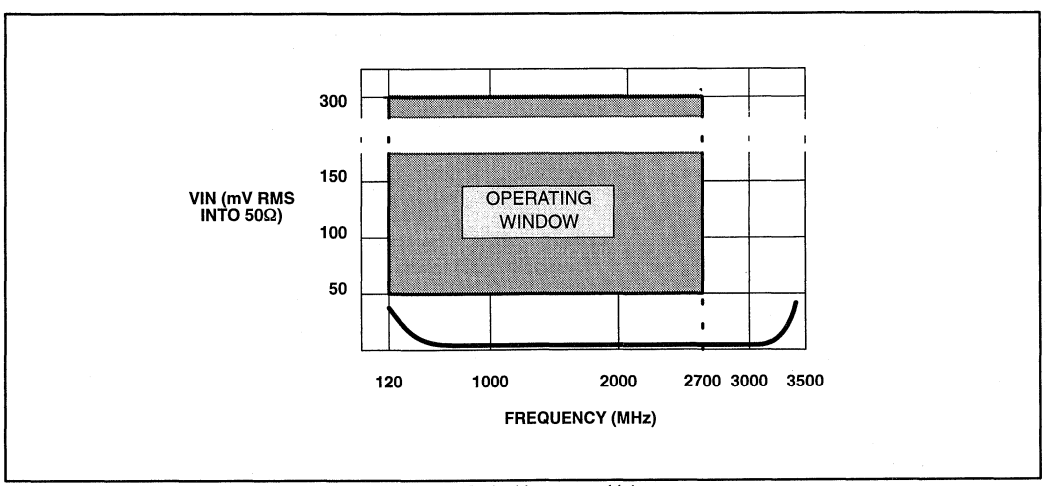


Fig. 5 Typical input sensitivity

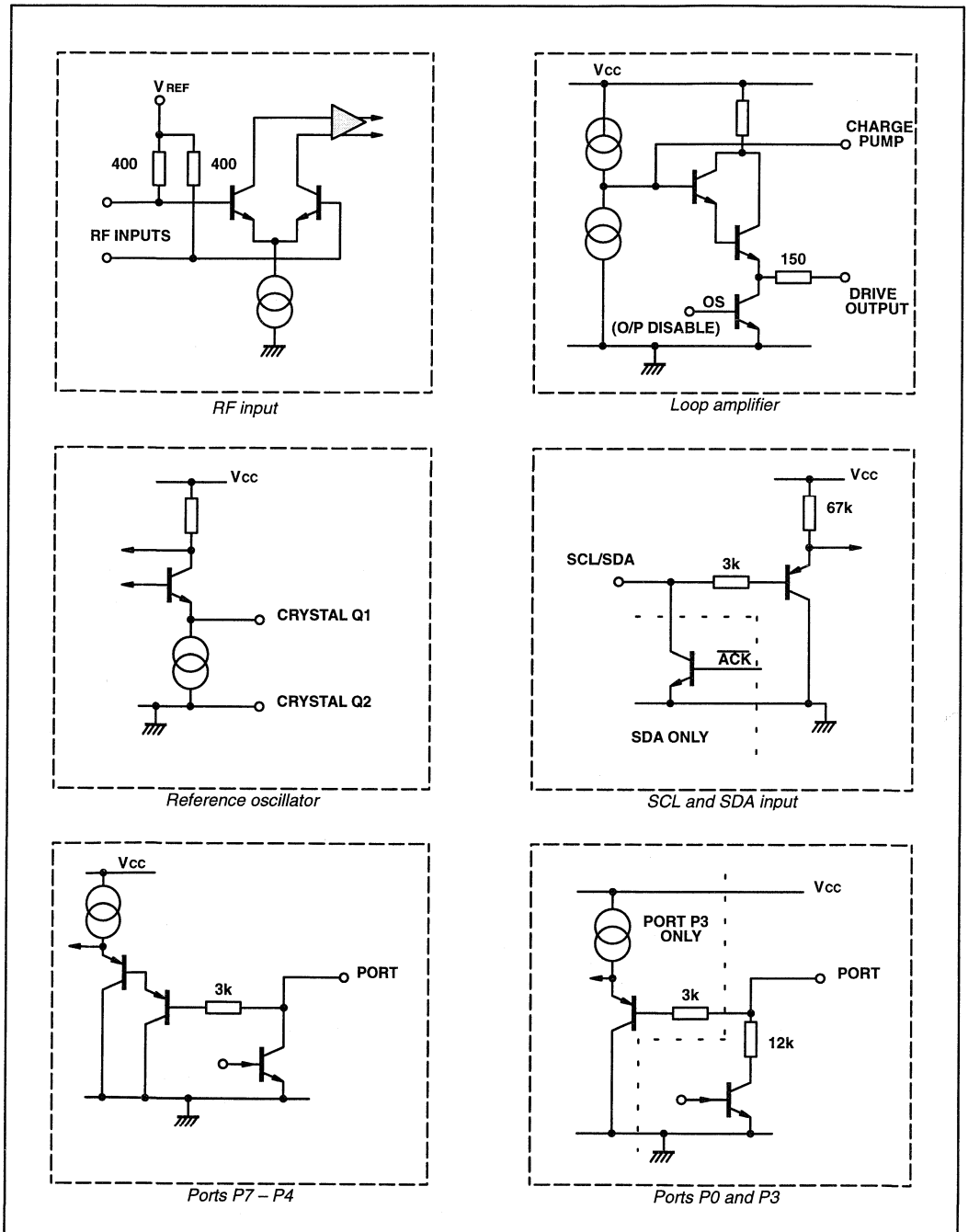


Fig. 6 Input/output interface circuits

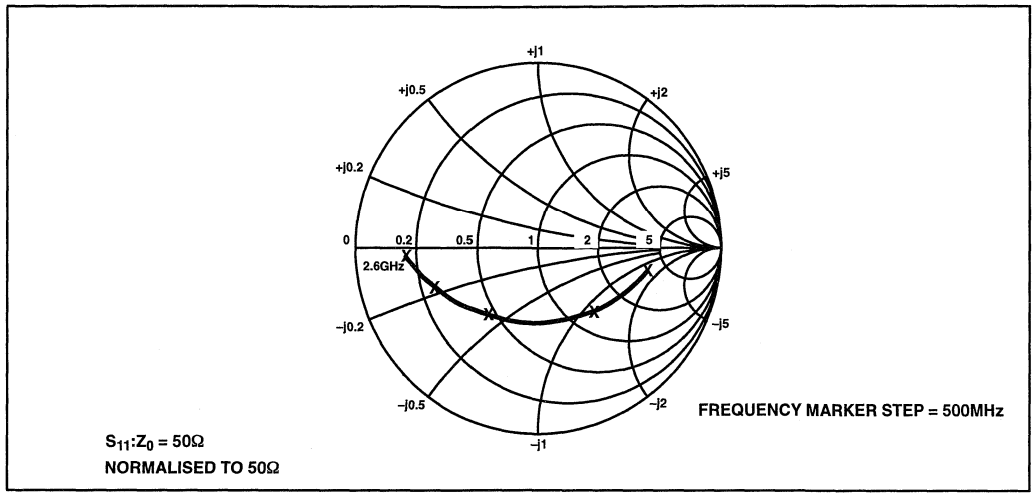


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V.

Parameter	Pin SP5655S	Value		Units	Conditions
		Min	Max		
Supply voltage	12	– 0.3	7	V	
RF input voltage	13, 14		2.5	Vp–p	
Port voltage	6–11 6–9 10, 11	– 0.3 – 0.3 – 0.3	14 6 14	V V V	Port in off state Port in on state Port in on state
Total port output current	6–11		50	mA	
RF input DC offset	13, 14	– 0.3	V_{CC} +0.3	V	
Charge Pump DC offset	1	– 0.3	V_{CC}+0.3	V	
Drive DC offset	16	– 0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	– 0.3	V_{CC}+0.3	V	
SDA,SCL input voltage	4, 5	– 0.3	6	V	
Storage temperature		– 55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance, chip–to–ambient			111	°C/W	
MP16 thermal resistance, chip–to–case			41	°C/W	
Power consumption at 5.5V			220	mW	All ports off
ESD protection	ALL	3		kV	MIL STD 883C TM 3015–7

Section 3
Video Modulation

GEC PLESSEY
SEMICONDUCTORS

SL5067

MULTI – STANDARD VIDEO MODULATOR

The SL5067 is a video up converter, capable of operating at frequencies up to 900MHz. It is compatible with both PAL and NTSC, accepting baseband video and sound inputs and modulating up to any desired VHF or UHF channel.

Modulated UHF outputs consist of open collectors driving external 75Ω load resistors for line matching requirements. Prescaler outputs are also provided enabling the use of a synthesiser to control oscillator frequency. The SL5067 operates from a 5V supply.

FEATURES

- 5V Operation
- Symmetrical RF Oscillator Operating to 900MHz
- Symmetrical RF drive to a frequency synthesiser
- Video Signal Input Clamp
- Video Peak White Level Detection and Automatic Gain Control
- Control of Video Modulation Index
- Direct Drive into 75Ω, via Symmetrical open Collector Outputs
- ESD Protection †
- Picture Carrier to Sound Carrier Ratio Adjustment
- Low External Component Count

† ESD Precautions must be observed

APPLICATIONS

- Video Recorders
- Cable Systems
- Video Cameras
- Personal Computers
- Video Security Systems
- In Home Rebroadcast System (LPTV)

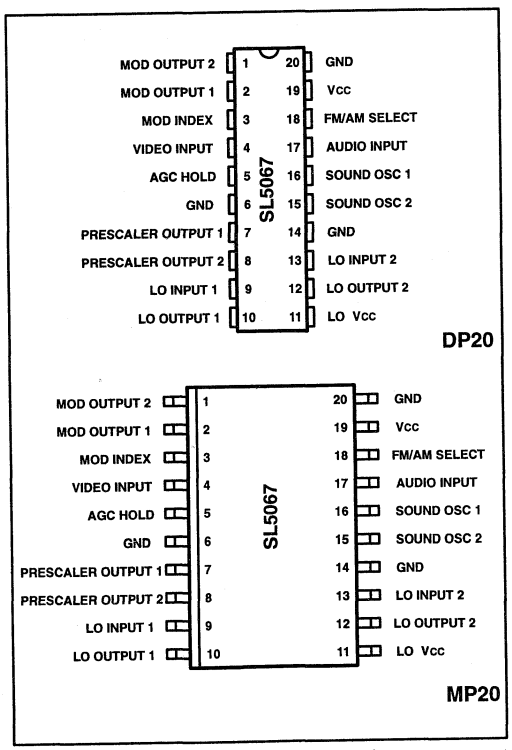


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SL5067 /KG/DPAS
SL5067 KG/MPES
SL5067/KG/MPEF (Tape and Reel)

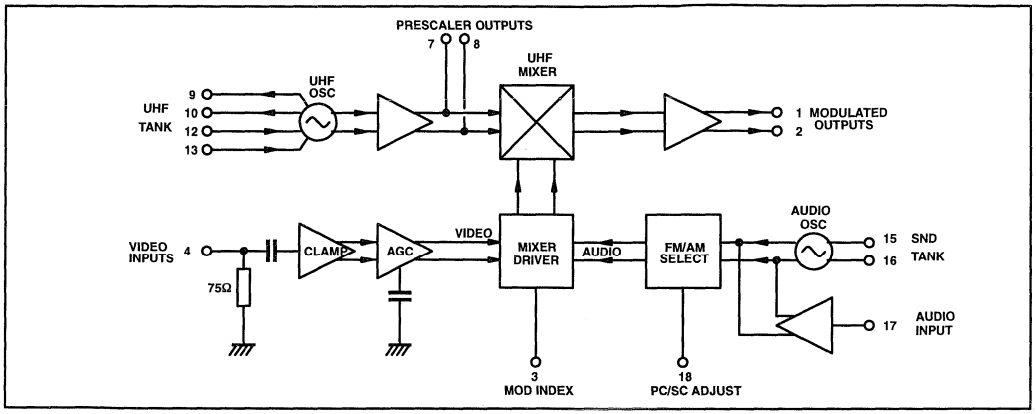


Fig. 2 SL5067 block diagram

ELECTRICAL CHARACTERISTICS

T_{amb}= −10°C to +80°C, V_{CC}= +4.5V to +5.5V. These characteristics are guaranteed over the following conditions (unless otherwise stated). They apply within the specified ambient temperature and supply voltage ranges.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage	11, 19	4.5		5.5	V	
Supply Current	11, 19		52		mA	V_{CC}=5V
LO Prescaler Output Level	7, 8		10		mV RMS	Single ended into 50Ω
LO Prescaler Output Impedance	7, 8		50		Ω	
LO drift with temp from switch on	10, 12		70		kHz	See note 1
LO variation with supply	10, 12		330		kHz	See note 1, V_{CC} = 4.5 to 5.5 V
RF carrier output level	1,2		84		dBμV	unmodulated into 50Ω
Video Input	4	0.5	1.0	1.5	Vp–p	
Video mod index	1, 2	70	80		%	See note 2
Video Signal/Noise Ratio	1, 2		59		dB	Weighted PAL 200kHz – 5.5MHz
Sound Subcarrier temperature drift from switch on	15, 16		4		kHz	See note1
Sound drift with supply	15, 16		2.5		kHz	V_{CC} = 4.5 to 5.5V
Audio Input Impedance	17		25		kΩ	
Audio Input Voltage reference	17		2		V	
Audio Input Level	17		0.88	1	Vp–p	Measured at pin 17
FM THD	1, 2		1		%	Q = 9, Δf = ±35kHz
AM THD	1.2		1		%	Input level 880mV p–p
Picture/Sound Carrier Ratio (FM)	1, 2	10	13	20	dB	R = 0, See note 3

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= −10°C to +80°C, V_{CC}=+4.5V to +5.5V. These characteristics are guaranteed over the following conditions (unless otherwise stated). They apply within the specified ambient temperature and supply voltage ranges.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Sound Oscillator FM Deviation	1, 2		250		kHz/V	C = 120pF, L = 5.6µH (Q_L = 9)

NOTES
1. Including external components effects
2. May be increased by use of external resistor, see Fig. 3
3. May be adjusted by use of external resistor dependent on video content, see Fig. 4
4. The above measurements assume nominal 80% modulation depth on vision and sound carriers

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE}=0V

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply Voltage	11, 19	−0.3	7	V	
Modulation index	3	−0.3	V_{CC}+0.3	V	
Video input	4	−0.3	V_{CC}+0.3	V	
Audio input	17	−0.3	V_{CC}+0.3	V	
FM/AM select	18	−0.3	V_{CC}+0.3	V	
Storage temperature		−55	+125	°C	
DP20 thermal resistance, chip–to–ambient			78	°C/W	
DP20 thermal resistance, chip–to–case			30	°C/W	
MP20 thermal resistance, chip to ambient			93	°C/W	
MP20 thermal resistance, chip–to–case			34	°C/W	
Power consumption at 5.5V			300	mW	

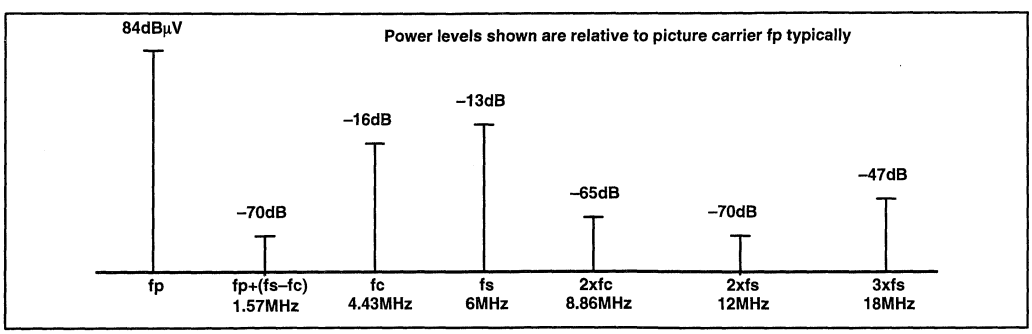


Fig. 3 Frequency spectrum above the Video picture carrier (Q_{TANK} = 9)

VIDEO

The video signal is applied to pin 4 via a coupling capacitor, (see Fig.9). This capacitor provides both clamping and black level hold. The internal peak white AGC can cope with an input signal of between 0.5 and 1.5 volts peak to peak.The full 9.5 dB AGC range is handled within a 600mV span on this storage capacitor.

Pin 3 (MOD INDEX) is used to control both RF carrier amplitude and video polarity, see Fig. 3. Since the video input is internally AGC'd, varying the carrier amplitude will also adjust the video modulation index, see Fig. 4.

For example, for a negative modulation (PAL or NTSC) with an 80% modulation index, pin 3 should be set to 1.1Volts (see Fig. 4). This voltage corresponds to an unmodulated RF output level of 82dBμV, see Fig. 3.

AUDIO

The sound IF oscillator can operate from 4.5MHz to 6.5MHz to cover all sound standards. The centre frequency is determined by the Sound IF Tank LC connected between pins 15 and 16.

The centre frequency is given by.

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

The Q factor of the TANK is given by.

$$Q = \frac{1770}{2\pi f_0 L} = 1770 \times 2\pi f_0 C$$

The Q factor of the coil must be high, e.g. >20

Good temperature stability can be achieved by the correct choice of temperature coefficients for C_{sound} and L_{sound}.

The Audio signal should be coupled into pin 17 via a 470nF capacitor. The maximum input level is 1 volts peak to peak.

Selection of AM or FM sound is made via pin 18 (FMAMSEL). The DC value on this pin controls the level of the sound subcarrier. The crossover point between FM and AM sound occurs at $\frac{1}{2}V_{CC}$ (measured at pin 18). Below this voltage, the modulator is set to FM sound; above it to AM. Graphs for AM and FM sound subcarrier output levels are shown in Figs. 6 and 7.

If AM sound is required, it is recommended that a modulated carrier is fed into the Audio input. Further details of this are mentioned at the end of the datasheet in the paragraph marked "Positive Modulation"

MODULATED RF OUTPUT

The modulated RF outputs from pin 1 and pin 2 consist of open collectors which should be externally connected to V_{CC} via 75Ω resistors. Great care must be taken with the decoupling of the supply to these outputs.

Both outputs are suitable for driving either 75Ω line, or for connection to a balun or impedance matching transformer.

This has the added benefit of minimising common mode coupling, thus giving improved RF performance.

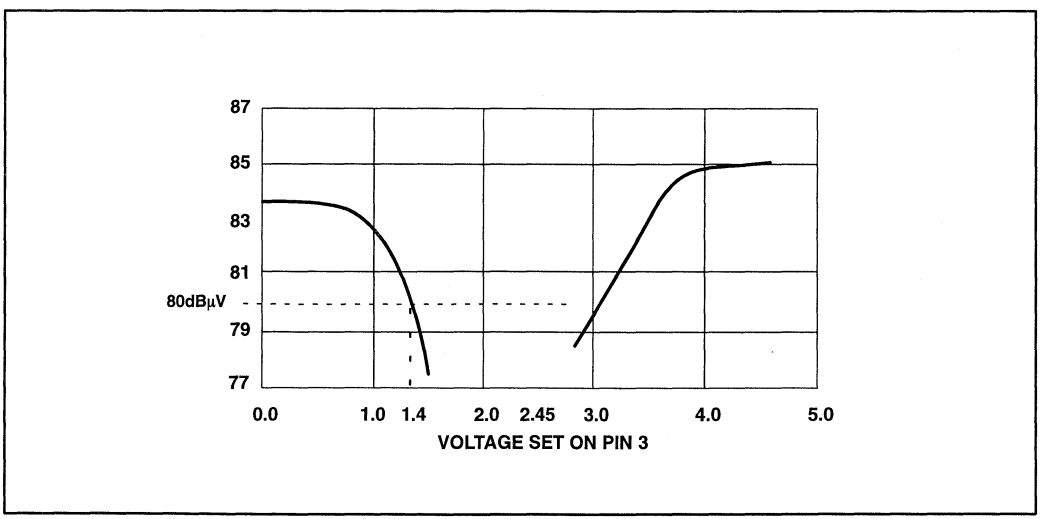


Fig. 4. Picture carrier, unmodulated RF output level

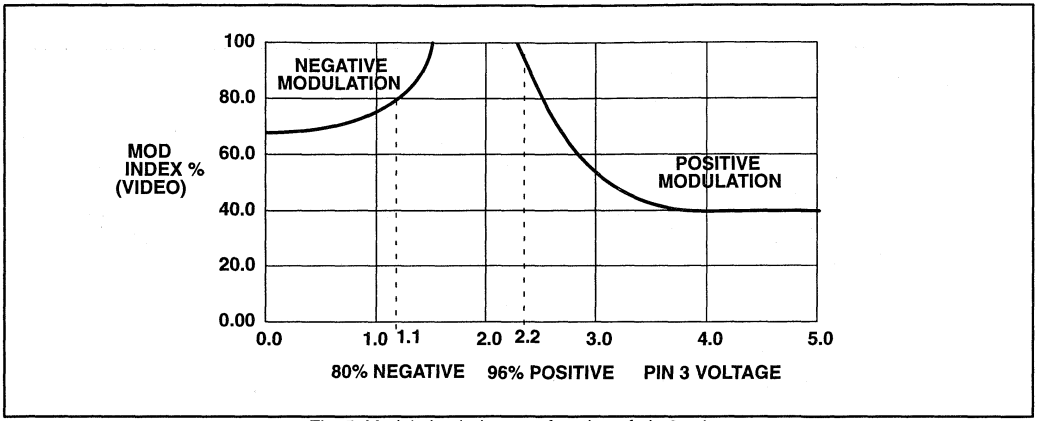


Fig. 5. Modulation index as a function of pin 3 voltage

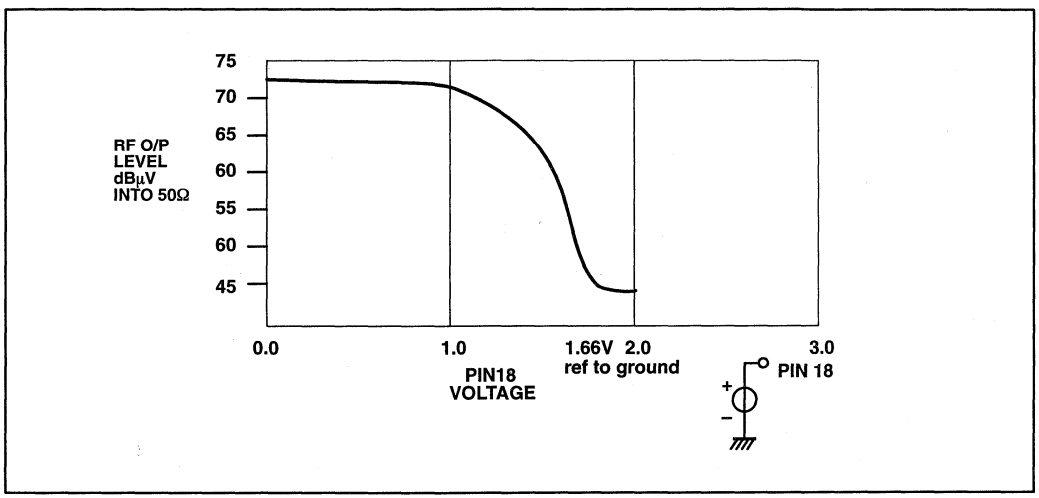


Fig. 6 FM sound carrier amplitude dBμV.

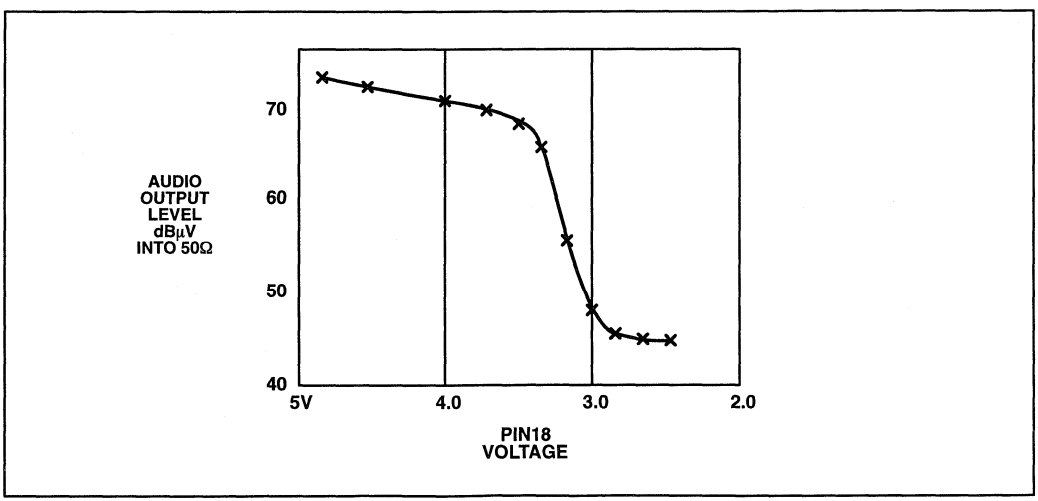


Fig. 7 AM sound carrier amplitude dBμV unmodulated

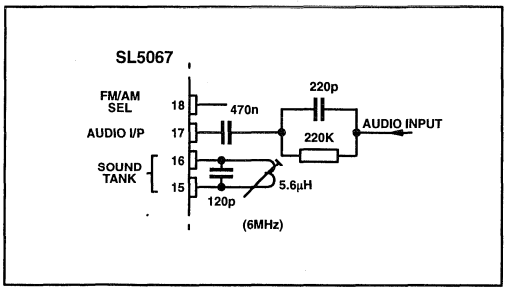


Fig. 8. Typical FM sound section

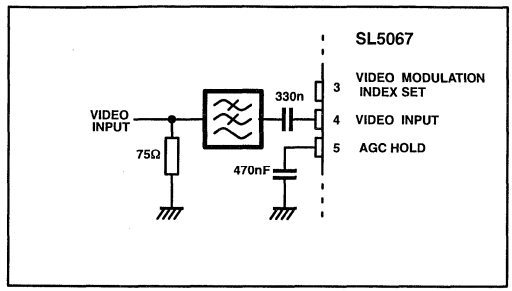


Fig. 9 Video input

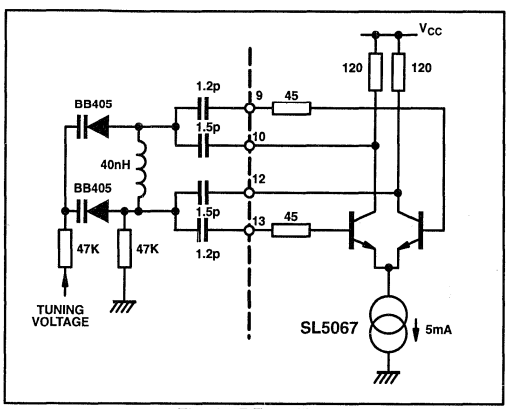


Fig. 10 RF oscillator

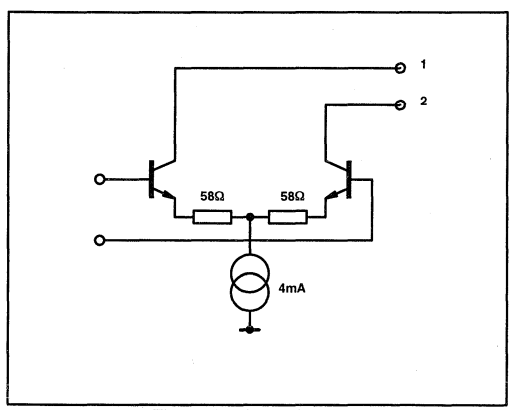


Fig. 11 Modulated outputs

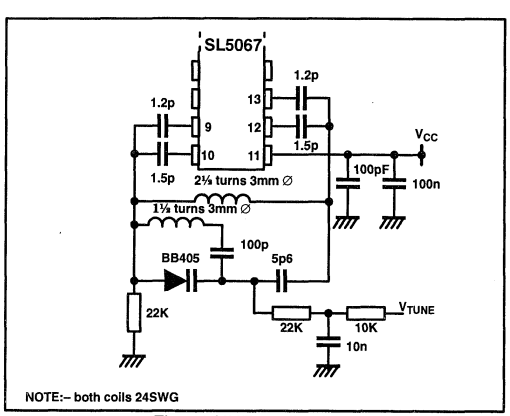


Fig. 12 UHF application

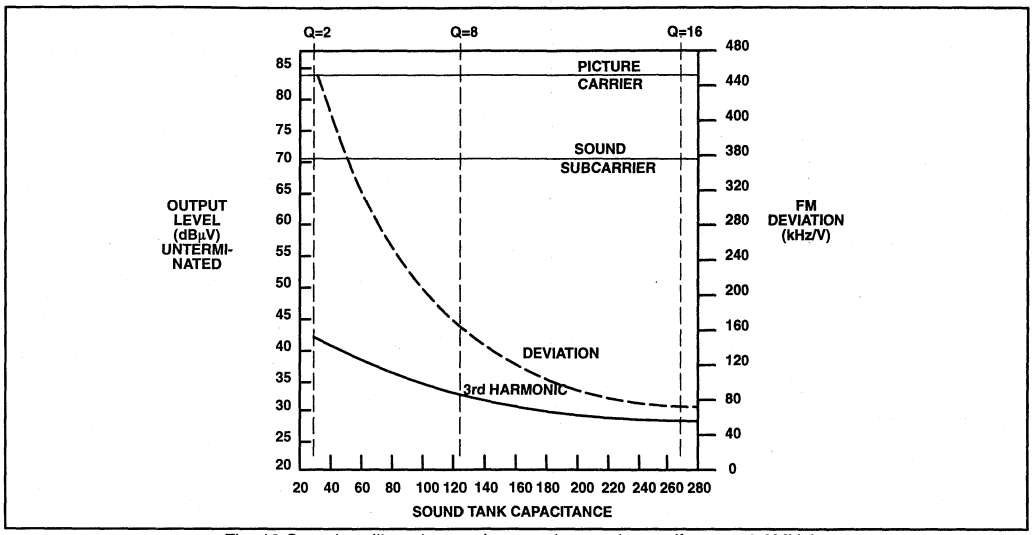
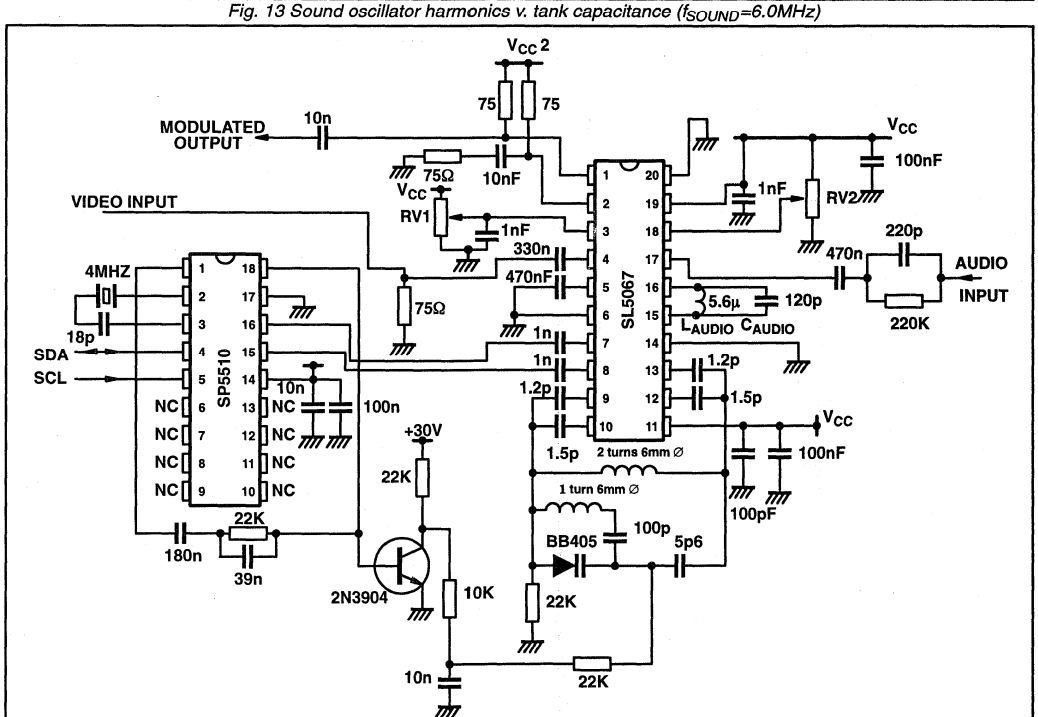


Fig. 13 Sound oscillator harmonics v. tank capacitance (f_{SOUND}=6.0MHz)



NOTES:– RV1 adjusts the modulation index
RV2 adjusts the picture carrier to sound carrier ratio
In applications the potentiometers should be replaced by 1% fixed resistors connected between Vcc and Gnd
The values chosen must reproduce the correct bias voltages on the relevant input pins

Fig.14 typical application showing video modulator with synthesised oscillator

APPLICATION NOTES

Overview

The key to good modulator performance is to ensure good and compact circuit layout with adequate grounding of all supplies. Earth loops must be avoided or kept as small as possible since RF coupling either through the air, or through the ground plane itself is the single most important factor in degrading modulator performance. Double sided board with a groundplane should be used, and all sensitive pins must be properly decoupled as close to the device as practicable.

Oscillator design and layout

The oscillator should be kept as small as possible to minimise parasitics. It is recommended that the circuit diagram shown in these application notes is used if the entire UHF band is to be covered. For lower frequencies or for applications requiring less tuning range, component values can be adjusted. Surface mount components should be used throughout the circuit and particular care must be taken with placement as the two coils should be as close to the oscillator pins as possible.(See Figs. 16 and 17)

For applications at low VHF frequencies, it is suggested that the values of the coupling capacitors on pins 9, 10, 11 and 12 are increased, 2.2pF capacitors (or greater) may be used for frequencies up to 500MHz but it must be remembered that the larger the coupling capacitor used, the smaller the tuning range will be, as the varactor diode capacitance will form a lower percentage of the total tuning capacitance of the loop.

For fixed frequencies (or small tuning ranges) up to 100MHz, 15pF or 18pF capacitors may be used.

Varactor tuning of the SL5067 should not be attempted unless the application either uses a synthesiser, or a temperature compensating network is used. The capacitance of most varactor diodes changes greatly with temperature, and this must be compensated for if the modulator is to remain on tune to the correct channel.

For applications requiring tuning over only a few channels, an air variable capacitor plus appropriate temperature compensation may be used.

Modulated outputs

Care must be taken with the routing of the modulated outputs and also with the mod index pin, pin3. It is suggested that pin 1 is used, and that the unused modulated output on pin 2 is terminated in a way which looks as physically and electrically similar to the used output on pin 1.

Experiments have shown that a RF coupling problem can exist between pins 2 and 3. This manifests itself at frequencies over 600MHz in applications where pin 3 is not taken directly to ground. Good decoupling of pin 3 (with 10pF and 10nF) will help to reduce these effects.

The modulated outputs must be routed away from the oscillator tank as there is danger of the local oscillator signal coupling directly into the modulated outputs. This will produce distortions in the modulated signal giving bad performance in such characteristics as differential phase and gain. For VHF and other applications below 500MHz RF coupling is not such a problem, however similar care should still be taken with layout in order to maximise device performance.

Use of a balun

It is possible to further improve device performance with the use of a balun to remove the effects of common mode coupling. Although using a balun will add to component cost, it may be the only way to achieve acceptable performance at higher frequencies where common mode noise has made it impossible to achieve a low enough minimum power signal to give the necessary dynamic range in the output signal. A low cost balun wound on a ferrite bead former should be sufficient to provide adequate performance in the majority of applications.

Sound tank circuit

Care must also be taken with the layout of the sound tank, in order to minimise harmonics,and reduce coupling between the audio and video parts of the circuit. The sound tank must be situated as close to the device pins as possible. If this is not done, RF may couple into the sound tank, via the tracks connecting the sound oscillator to the inductor and capacitor. In practice, it is easiest to mount the sound tank capacitor close to, or directly on pin 15 and 16, with the inductor slightly further away. This appears to give the best linearity.

In some cases where some coupling and/or distortion problems are occurring, the addition of small 2p2 capacitors from either side of the tank circuit to ground may improve both FM deviation and linearity.

For optimum performance (in the FM case) the sound tank should be selected to give a Q of around 10. The circuits shown in the datasheet give a value of approximately 9, and are the suggested normalised values to be used.

Lower values of Q will give greater FM deviation per volt input (kHz/Volt), but also increase the level of the 3rd harmonic of the sound subcarrier. This is shown in Fig. 10.

The Q of the inductor chosen should be at least 2.5 times the Q of the tank circuit itself.

It is not recommended that a Q of over 16 is used, as the amplitude of the sound subcarrier fundamental will start to decrease once a Q of approx 12 has been reached. Thus if a Q of 20 were used in order to give good harmonic performance, there would be an unacceptable trade off in terms of picture carrier to sound subcarrier ratio, which would be approx 20dB.

MISCELLANEOUS POINTS

Board layout and decoupling

Good decoupling techniques must be used throughout with the use of surface mount components wherever possible. For best performance, all supplies and sensitive pins should be decoupled as close to the device as possible, with a combination of capacitors, say 100pF and 10nF to ground. The use of double sided board with a groundplane is strongly advised. This should be of particular help in the reduction of oscillator coupling.

Mod index pin

As already stated, great care must be taken with the mod index pin, pin 3. This should be decoupled with chip components as close to the pin as possible. Ideally the mod index should be defined with a DC voltage, thus requiring the use of two external resistors, see Figs 4 and 5. It is also possible to define mod index through the use of a single resistor connected to ground or V_{CC} depending on whether negative or positive modulation is required.

Synthesiser drive

It is suggested that any synthesiser (if used) is driven differentially. This is done by taking both of the prescaler outputs (pin 7 and 8) to the synthesiser via 1nF or 10nF capacitors.

FM/AM select

The voltage on the FM/AM select pin should be defined by two external resistors between v_{cc} and ground, see Figs 6 and 7. The application diagram Fig. 14 shows a potentiometer, RV2 which is used to define the voltage on this pin in the demo board in practice it is suggested that in low total resistance value (5V or less) is used between V_{CC} and GND since this will ensure a constant voltage on pin 18 irrespective of any small internal resistance variations between devices, thus ensuring a constant PC/SC ratio. It should be noted that the sound subcarrier level is referenced to the AGC sidebands rather

than the picture carrier itself. Thus if the picture carrier level is reduced by using a resistor on pin 3 (mod index set), the level of the sound subcarrier will not change. This should be remembered when setting up a modulator to give the desired modulation index and vision/sound carrier ratio.

POSITIVE MODULATION

Several references are made in the text to positive video modulation and AM sound. Whilst it is possible to switch the device into these modes, it should be noted that the SL5067 will not perform to full SECAM specifications.

Use of AM sound may produce sound–in–vision interference at higher modulation depths. It should be possible, however to AC couple in modulated audio. If this is attempted, the sound tank circuit on pins 15 and 16 would not be required. The modulated audio signal should be fed into the Audio input pin (pin 17) via a 470nF capacitor.

The FM/AM select pin can be used as a gain control pin, but will not switch the device between FM and AM modes.

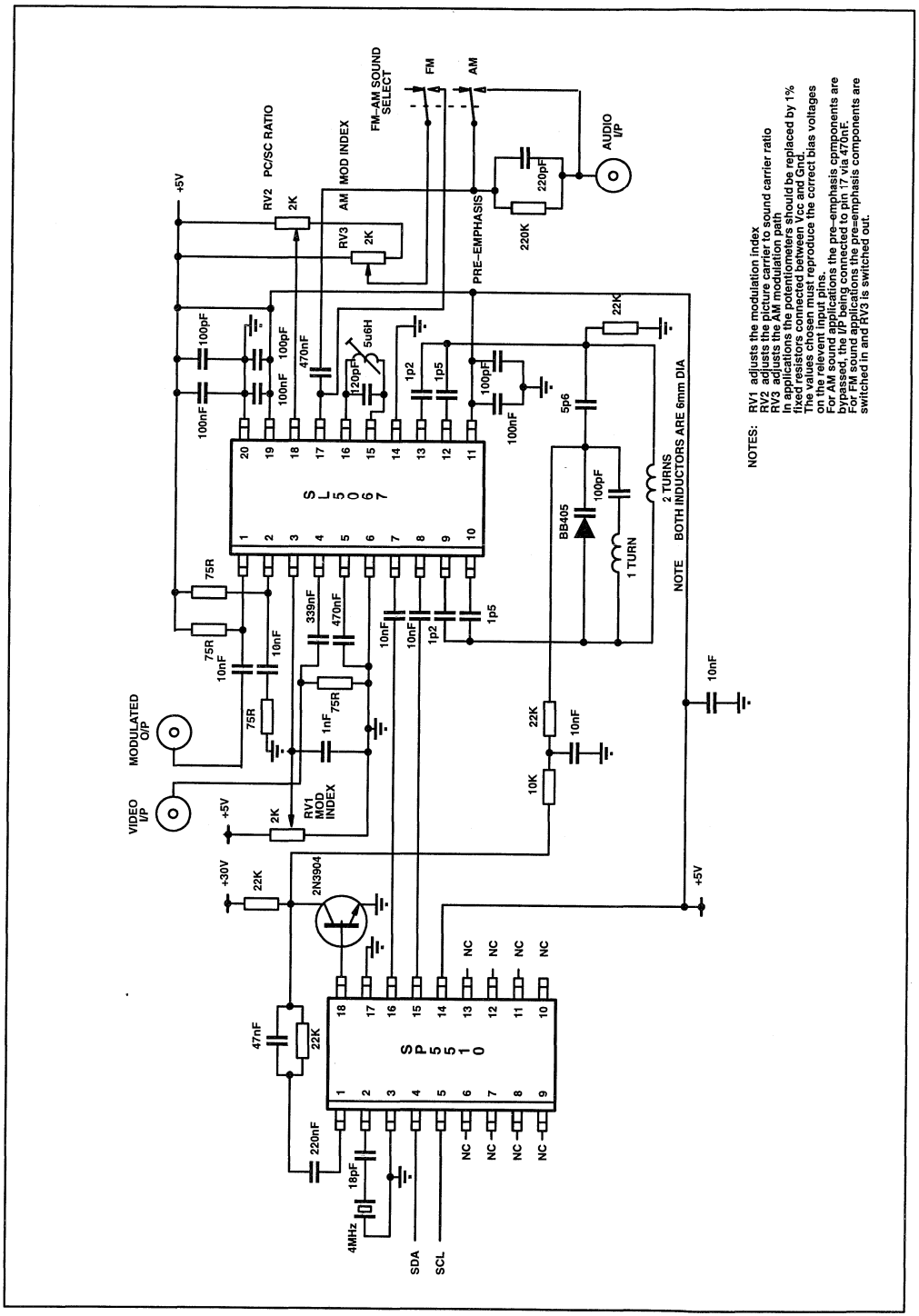
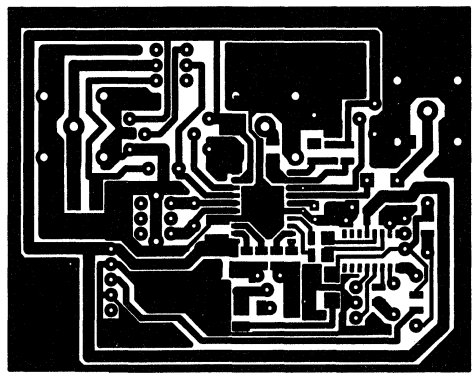
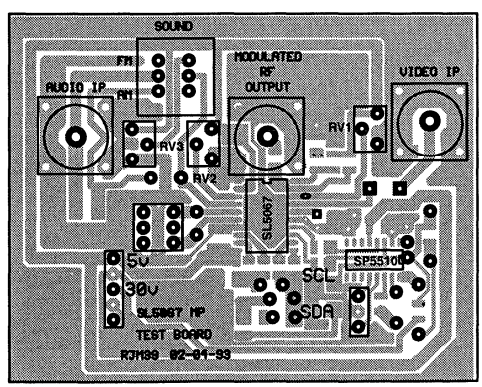


Fig. 16 Video modular test board circuit diagram



TRACK LAYOUT



SL5067 TEST BOARD LAYOUT

Fig. 17

Section 4

Satellite TV Receiver Circuits

SL1451

WIDEBAND PLL FM DETECTOR FOR SATELLITE TV

The SL1451 is a phase locked loop demodulator for use in wideband FM systems. It is intended for use with an IF input frequency from 300MHz to 700MHz in satellite receivers. It consists of an input RF amplifier, signal level detector, UHF phase detector UHF oscillator and video/loop amplifier. Both positive and negative going video outputs are available.

FEATURES

- Complete PLL System for Wideband FM Demodulator
- Noise Threshold Performance: 8dB (Typ.)
- Low External Component Count
- Positive and Negative going Video Output
- Demodulates FM Signals with up to 28MHz p-p Deviation

APPLICATIONS

- DBS Receivers
- Wideband Data Communications Demodulation

ORDERING INFORMATION

SL1451 NA DP (16-lead plastic DIL package)

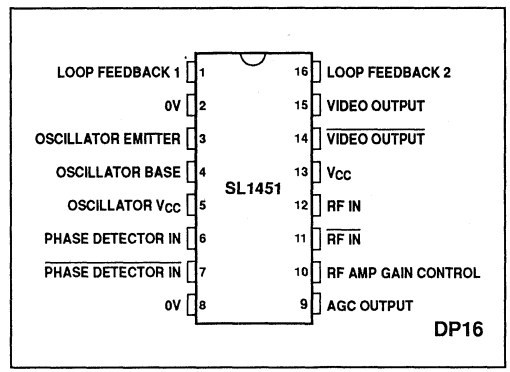


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	−10°C to+80°C
Supply voltage, V_{CC}	11V
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

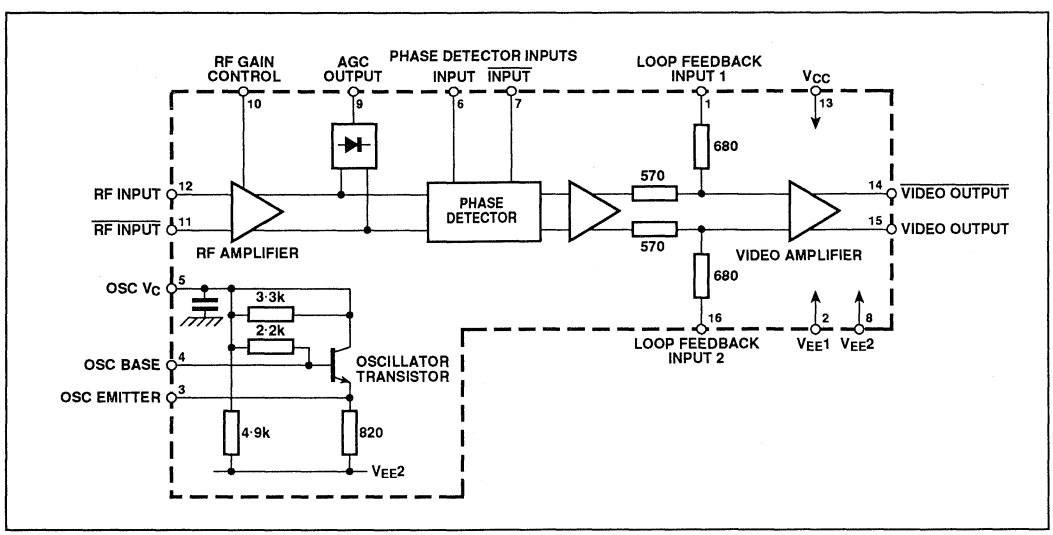


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = +25°C, V_{CC} = 7·4V to 9V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	13,5	40	55	70	mA	
Supply voltage	13,5	7·4	8·2	9	V	
Minimum oscillator frequency			300		MHz	
Maximum oscillator frequency			700		MHz	
Phase detector input level from oscillator	6,7	400	70	100	mV	
RF input level	11,12	12·5	40	125	mV	
Phase detector gain			0·5		V/Radian	
AGC output	9		300		µA	No input signal
			140		µA	−20dBm input signal
Oscillator lock range			50		MHz	See note 1
VCO slope			14		MHz/V	
Video output voltage	14,15		1·5		V p-p	21·4MHz p-p deviation
Intermodulation products			−40		dBm	See note 2
Video bandwidth			18		MHz	

NOTES
1. All characteristics from Oscillator Lock Range to Video Bandwidth are measured using the application circuit Fig. 3.
2. Signal 1: 4·433MHz, deviation = 21·4MHz p-p.
   Signal 2: 6MHz, deviation = 3MHz p-p.

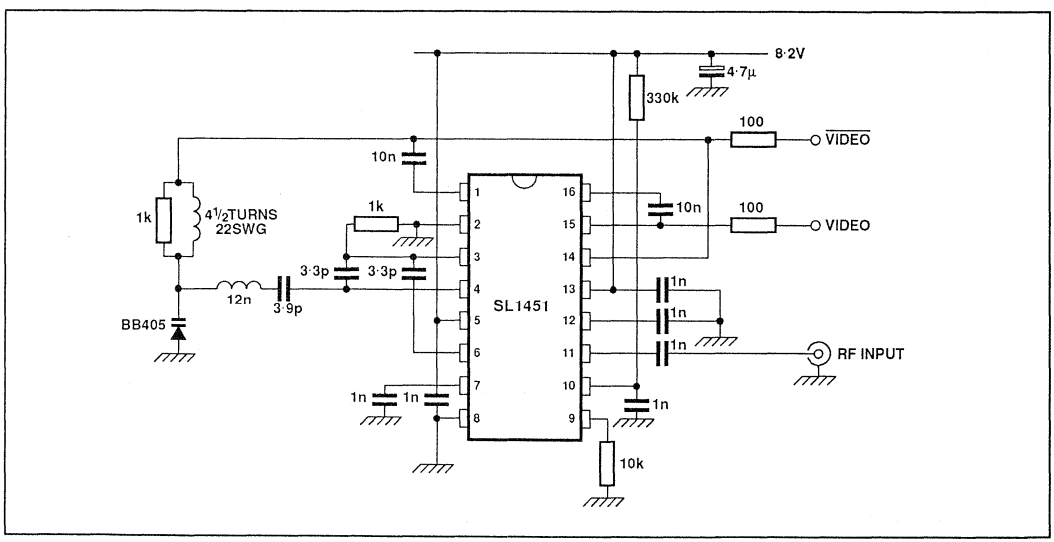


Fig. 3 Typical application circuit

SL1452

WIDEBAND LINEAR FM DETECTOR FOR SATELLITE TV

With a minimum of external components, the SL1452 forms a complete wideband FM detector suitable for use in satellite TV. The video output and bandwidth may be optimised by adjustment of the working Q of the quadrature coil.

FEATURES

- High Operating Frequency Simplifies Image Filtering
- Negligible Differential Gain and Phase Errors
- Video Bandwidth Suitable for High Definition TV
- High Sensitivity and Wide Dynamic Range
- Wide Operating Frequency Range: 300 to 1000 MHz
- Electrostatic Protection*

* Normal ESD handling precautions should be observed

ORDERING INFORMATION

SL1452 NA DP (8-lead plastic DIL package)
SL1452 NA MP (8-lead miniature plastic DIL package)

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	−10°C to+80°C
Supply voltage, pin 6	7V
Input voltage, pin 7 or 8	2·5V p-p
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

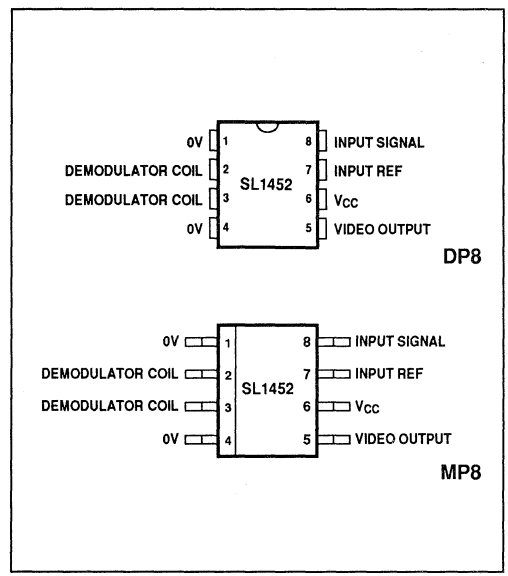


Fig. 1 Pin connections - top view (not to scale)

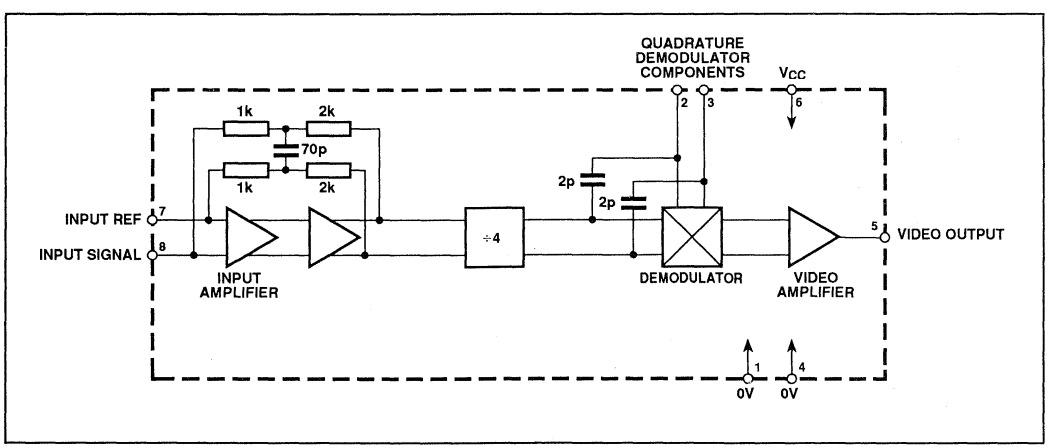


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = +25°C, V_{CC} = +4·5V to +5·5V, Q = 6, f = 612MHz

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	6		40	50	mA	V_{CC} = 5V
Video output voltage	5		0·7		V p-p	Δf = 13·5MHz p-p
Video bandwidth	5		14		MHz	
Minimum operating frequency	8		300		MHz	
Maximum operating frequency	8		1000		MHz	
Input voltage	8	10		300	mVrms	
Intermodulation	5		−60		dB	Product of input modulation: f = 4·4MHz, Δf = 13·5MHz p-p and f = 6MHz,Δf = 2MHz p-p (PAL colour and sound subcarriers).
Differential gain	5		<±1		%	Δf = 13·5MHz p-p. Demodulated staircase referred to input staircase before modulation.
Differential phase	5		<±1		deg	Demodulated colour bar waveform referred to waveform before modulation.
Signal-to-noise ratio	5	70			dB	Ratio of output with Δf = 13·5MHz p-p at 1MHz to output rms noise in 10MHz bandwidth with Δf = 0.

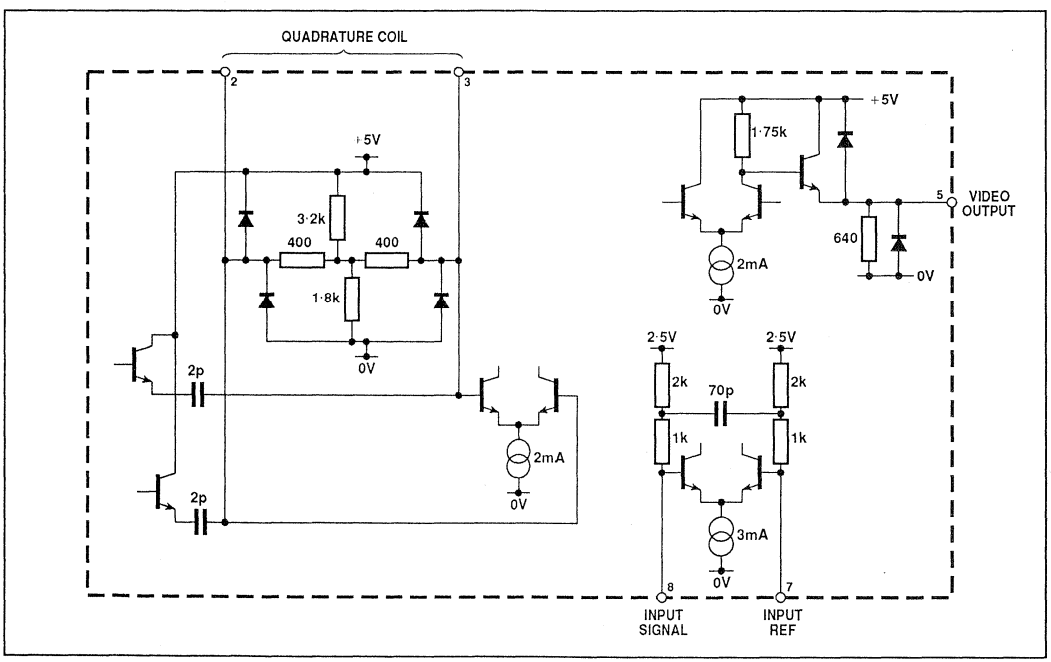


Fig. 3 Input/output interface circuits

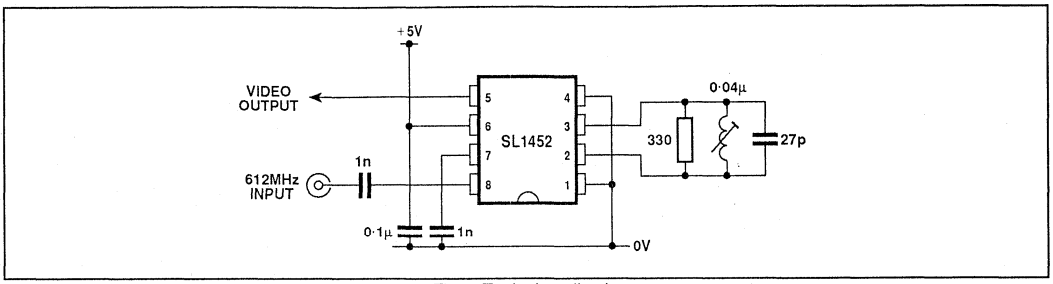


Fig. 4 Typical application

SL1452 QUADRATURE DEMODULATOR

The SL1452 FM demodulator has a simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig. 4, but as with most integrated circuits, particularly those working at high frequencies, some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be ensured by the simple precaution of keeping all components close to the SL1452, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies, multilayer ceramic types usually providing small size and adequate high frequency performance. For the quadrature coil tuning capacitor a fairly stable component should be selected to prevent excessive drift. The power supply decoupling capacitor from pin 6 to ground should be 0.1µF minimum but the input coupling and decoupling values can be smaller, about 330pF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if maximum performance is to be obtained.

First determine the quadrature circuit operating frequency, which is a quarter of the input frequency on pin 8 due to the two internal ÷2 stages (see Fig.2).

Choose suitable values for L and C to resonate at the correct frequency using:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The value of C should by greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive level to the demodulator and thereby restricting the video output available. In general, for operation in the 400MHz to 600MHz range, an inductance value between 40nH and 60nH is recommended.

Once suitable L and C values have been determined, the working Q for the quadrature circuit should be set, the Q value determining the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig. 5.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800Ω resistance between pins 2 and 3 must be allowed for when calculating R.

Example

Design a quadrature circuit to demodulate a carrier on pin 8 with centre frequency 480 MHz and video bandwidth of 10MHz.

For L = 40nH, f_{QUAD} = 120MHz,
C = 43·98pF (nearest preferred value 47pF)
From Table 1, Q required is approximately 6,
therefore total R required is:

$$R = Q2\pi fL$$
$$= 6\times2\times\pi\times\frac{480\times10^{6}\times0{\cdot}04\times10^{-6}}{4}$$
$$= 181 \text{ ohms}$$

Allowing for the internal 800Ω resistance between pins 2 and 3 (see Fig.3), the external resistance required is 234Ω ; choose 270Ω.

It should be remembered that the internal 800Ω resistance is subject to production tolerances and if fairly close control of video bandwidth is required, the L and C ratio may require some adjustment to ensure that the external R is sufficiently low to swamp the effect of internal resistance changes. The value of 270Ω obtained in the example is low enough to allow adequate control.

In order to overcome the effects of component tolerances, it will usually be necessary to make either the L or C a variable component, the value being adjusted to obtain best linearity.

Q	Bandwidth
10	7·5MHz
6	14MHz
4	23MHz

Table 1

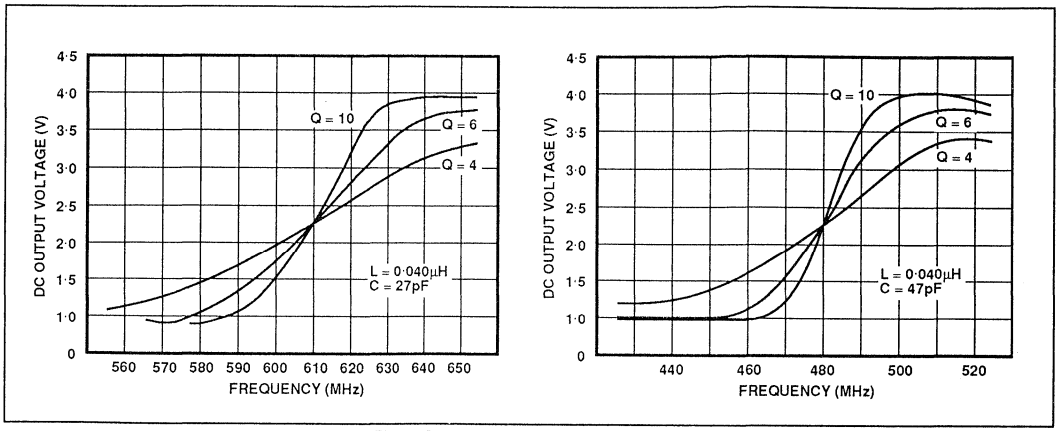


Fig. 5 Output voltage v. input frequency

SL1454

WIDEBAND LINEAR FM DETECTOR FOR SATELLITE TV

The SL1454 is a wideband FM demodulator designed to operate with a carrier frequency between 70MHz and 150MHz. The internal circuitry of the device is similar to that of the SL1452 except that the quadrature demodulator operates at the input frequency.

FEATURES

- Excellent Threshold
- Negligible Differential Gain and Phase Errors
- Video Bandwidth Suitable for High Definition TV
- High Sensitivity and Wide Dynamic Range
- Wide Operating Frequency Range: 70 to 150MHz

ORDERING INFORMATION

SL1454 NA DP (14-lead plastic DIL package)

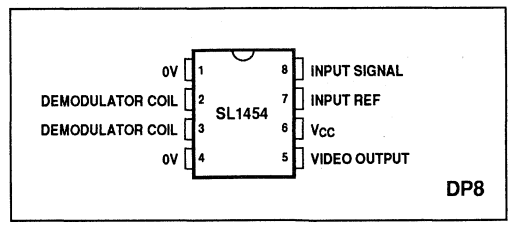


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	−10°C to+80°C
Supply voltage, pin 6	7V
Input voltage, pin 7 or 8	2·5V p-p
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

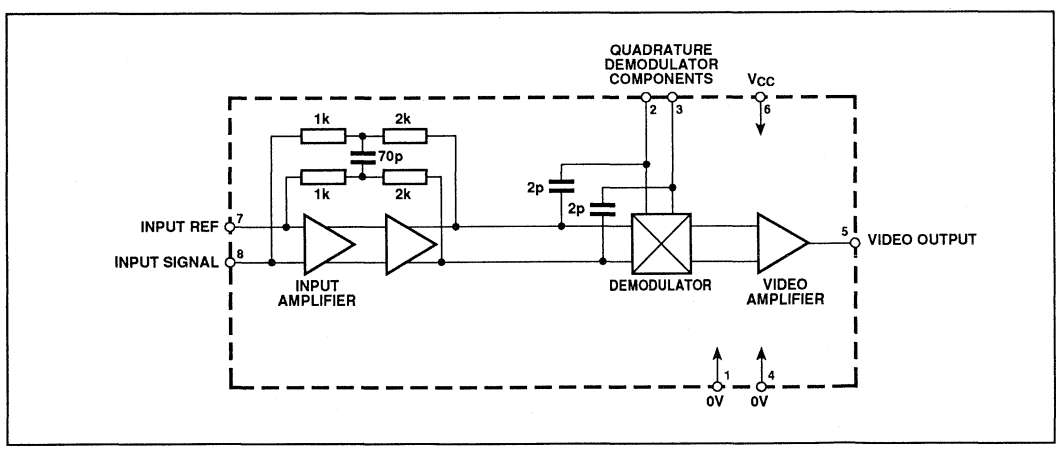


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = +25°C, V_{CC} = +4·5V to +5·5V, Q = 2, f = 140MHz

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	6		30	35	mA	V_{CC} = 5V
Video output voltage	5		0·4		V p-p	Δf = 21·4MHz p-p
Video bandwidth	5		10		MHz	
Minimum operating frequency	8		70		MHz	
Maximum operating frequency	8		150		MHz	
Input voltage	8	10		300	mVrms	
Intermodulation	5		−50		dB	Product of input modulation: f = 4·4MHz, Δf = 21·4MHz p-p and f = 6MHz, Δf = 3MHz p-p (PAL colour and sound subcarriers).
Differential gain	5		<±1		%	Δf = 21·4MHz p-p. Demodulated staircase referred to input staircase before modulation.
Differential phase	5		<±1		deg	Demodulated colour bar waveform referred to waveform before modulation.
Signal-to-noise ratio	5	70			dB	Ratio of output with Δf = 21·4MHz p-p at 1MHz to output rms noise in 10MHz bandwidth with Δf = 0.

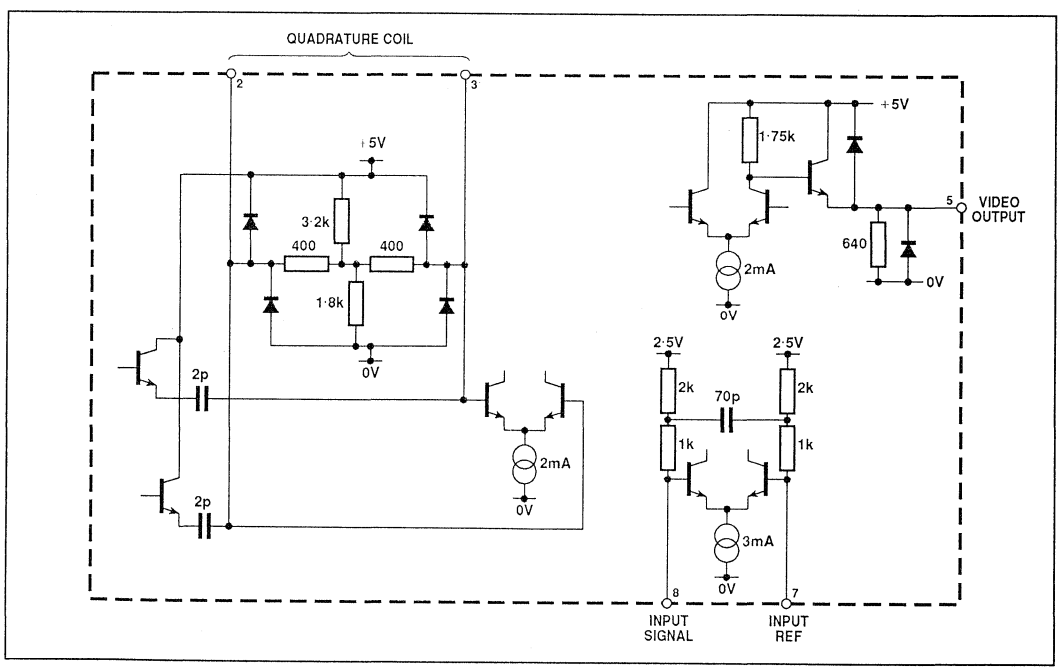


Fig. 3 Input/output interface circuits

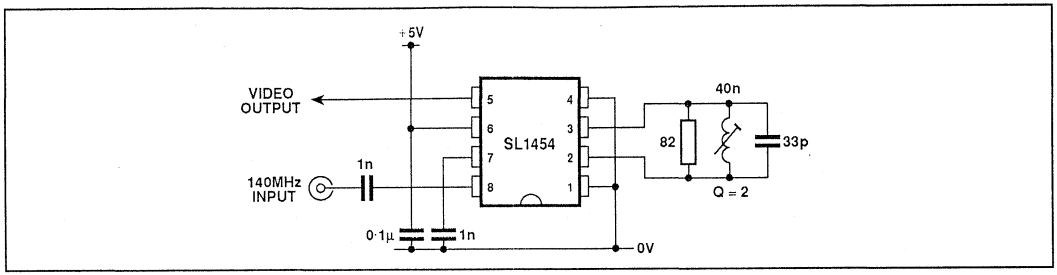


Fig. 4 Typical application for 140MHz

APPLICATION NOTES

The SL1454 FM demodulator has a very simple application with very low external component count. This is demonstrated by the applications circuit diagram Fig. 4, but as with most integrated circuits, particularly those working at high frequencies, some attention to good RF layout techniques and correct component selection will ensure optimum results.

A good layout can usually be ensured by the simple precaution of keeping all components close to the SL1454, maintaining short lead lengths and ensuring a good low impedance ground plane. Double sided board layout enables these objectives to be easily met, but is not essential for satisfactory operation. All coupling and decoupling capacitors should be chosen for low impedance characteristics at high frequencies. A fairly stable component should be selected for the quadrature coil tuning capacitor to prevent excessive drift. The power supply decoupling capacitor from pin 6 to ground should be 0.1µF minimum, but the input coupling and decoupling values can be smaller, about 330pF being adequate.

The only remaining components to be selected are those forming the quadrature circuit on pins 2 and 3 and some care in the determination of values for these is required if maximum performance is to be obtained.

Choose suitable values for L and C to resonate at the intermediate frequency you are applying to the device, using:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

The value of C should by greater than 15pF to prevent stray capacitance effects introducing errors and distortion of the demodulation S-curve, but the use of very large capacitances with small inductance values will lower the impedance of the tuned circuit at the required Q value, reducing the drive level to the demodulator and thereby restricting the video output available.

Once suitable L and C values have been determined, the working Q for the quadrature circuit should be set, the Q value determining the video output level and bandwidth. Video output is proportional to Q whereas video bandwidth is inversely proportional. The effect of Q variations on video bandwidth and amplitude can be determined from Table 1 and the graphs in Fig.5.

A value for total damping resistor value to obtain the required Q can be calculated from:

$$R = Q2\pi fL$$

The internal 800Ω resistance between pins 2 and 3 must be allowed for when calculating R.

As can be seen from the graphs in Fig.5, for the demodulator to demodulate a 20MHz peak to peak deviation signal with optimum linearity a very low Q value needs to be chosen (<2). However, this has the disadvantage of producing a demodulator with a very low peak to peak video output level.

One way of increasing the linear region of the S-curve without reducing the video output level is to incorporate a dual tuned circuit in the quadrature network. This can easily be done by capacitatively coupling another parallel tuned circuit to the normal quadrature tuned circuit.

Fig. 6 shows an example of this form of dual tuned circuit, both sections having the same Q factor and coupling capacitors chosen to give the best linearity (linear phase response). Fig.5(b) shhows the advantages of the dual tuned circuit. The effect of varying the Q factor of the dual tuned circuit on bandwidth is also described by Table 1.

Example

Design a quadrature circuit to demodulate a 140MHz carrier with centre with 21.4MHZ peak to peak deviation, modulated with a 25Hz triangular dispersion wave form of 2MHZ peak to peak deviation. The video bandwidth required is 9MHZ.

Choose L = 40nH
then C = 32.309pF (nearest preferred value 33pF)

The next value to choose is the Q factor. As dispersion is employed, linearity over the full 21.4MHz range needs to be optimised. The graphs in Fig.5 show that either a single tuned circuit with a Q of 2, or a dual tuned circuit with a Q of 3 is adequate. The dual tuned circuit has the advantage that the peak to peak video output is larger than that of the single tuned circuit, but extra components are required. Both circuits have a larger video bandwidth than the required 9MHz. The value of the damping resistor for the required Q is calculated below:

For Q = 2

$$\text{Total } R = Q2\pi fL$$

$$= 2\times2\times\pi\times140\times10^{6}\times0{\cdot}04\times10^{-6}$$

$$= 70{\cdot}3717\Omega$$

Allowing for the internal 800Ω resistance between pins 2 and 3 (see Fig. 3), the external resistance should be 77.1Ω Choose 82Ω.

For Q = 3

$$\text{Total } R = Q2\pi fL$$

$$= 3\times2\times\pi\times140\times10^{6}\times0{\cdot}04\times10^{-6}$$

$$= 105{\cdot}56\Omega$$

Allowing for the internal 800Ω resistance, the external resistance should be 121·5Ω, so choose 120Ω.

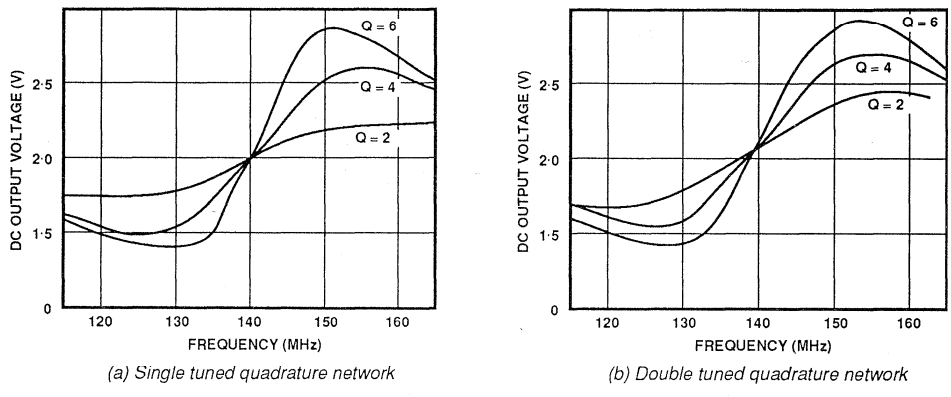
When using a dual tuned circuit the value of coupling capacitor is dependent of the Q factor. Table 2 gives a guide to the values needed for best linearity.

Q	Bandwidth
6	10MHz
4	11MHz
2	12MHz

Table 1

Q	Coupling capacitor
6	3·9pF
4	5·6pF
3	10pF

Table 2



(a) Single tuned quadrature network

(b) Double tuned quadrature network

Fig. 5 Output voltage v. input frequency

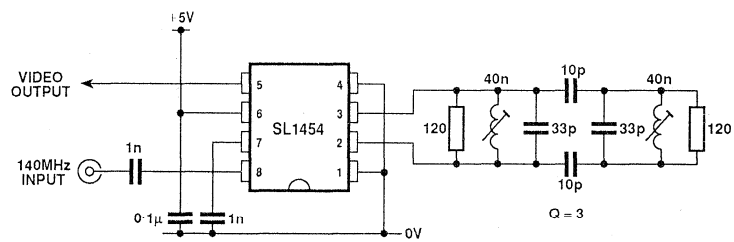


Fig. 6 Example of double tuned quadrature circuit

SL1455

WIDEBAND LINEAR FM DETECTOR WITH THRESHOLD EXTENSION

The SL1455 is a wideband FM demodulator with threshold extension. It is intended for use in satellite receivers with an IF between 300MHz and 700MHz.

FEATURES

- 7dB Noise Threshold Obtainable
- Low External Component Count
- Negligible Differential Gain and Phase Error
- Wide Operating Frequency Range: 300 to 700MHz
- Demodulates FM Signals with up to 28MHz p-p Deviation
- Electrostatic Protection*

* Normal ESD handling precautions should be observed

APPLICATIONS

- DBS Receivers
- Wideband Data Communications Demodulation

ABSOLUTE MAXIMUM RATINGS

Operating temperature range	−10°C to+80°C
Supply voltage	7V
Input voltage	2·5V p-p
Storage temperature	−55°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SL1455 NA DP (14-lead plastic DIL package)
SL1455 NA MP (14-lead miniature plastic DIL package)

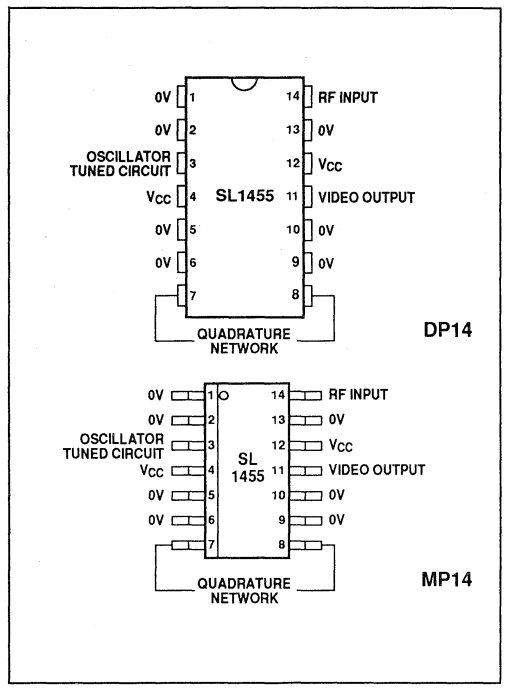


Fig. 1 Pin connections - top view (not to scale)

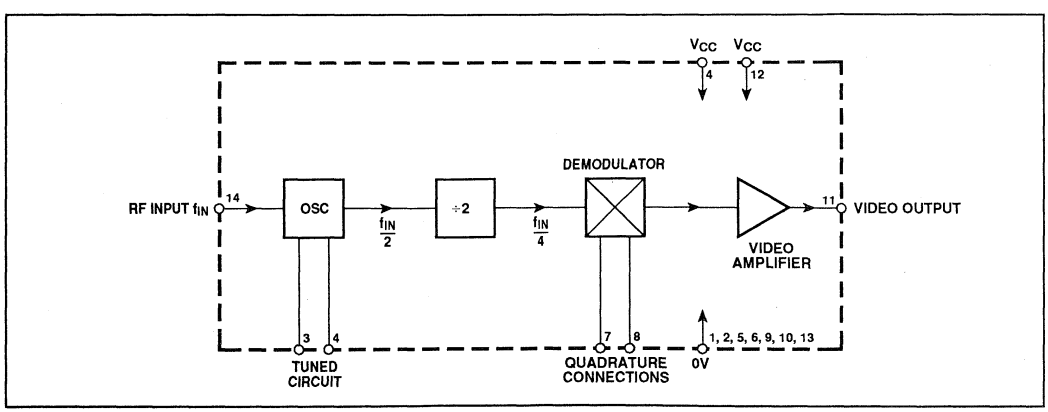


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = +25°C, V_{CC} = +4·5V to +5·5V.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage	12,4	4·5	5·0	5·5	V	V_{CC} = 5V
Supply current	12,4	25	30	35	mA	
Differential gain			<±1		%	Δf = 21·4MHz p-p. Demodulated staircase referred to input staircase before modulation.
Differential phase			<±1		Deg	Demodulated colour bar waveform referred to waveform before modulation.
IF range		300	610	700	MHz	
Input level	14		22	400	mVrms	
Noise threshold			7		dB	See note 1
Output level	11		1·3		V p-p	Δf = 21·4MHz p-p
Intermodulation products	11		−60		dB	See note 2
Video bandwidth			10		MHz	

NOTES
1. All characteristics from Noise Threshold to Video Bandwidth are measured using the application circuit Fig. 3.
2. Signal 1: 4·433MHz, deviation = 21·4MHz p-p.
   Signal 2: 6MHz, deviation = 3MHz p-p (PAL and sound subcarriers).

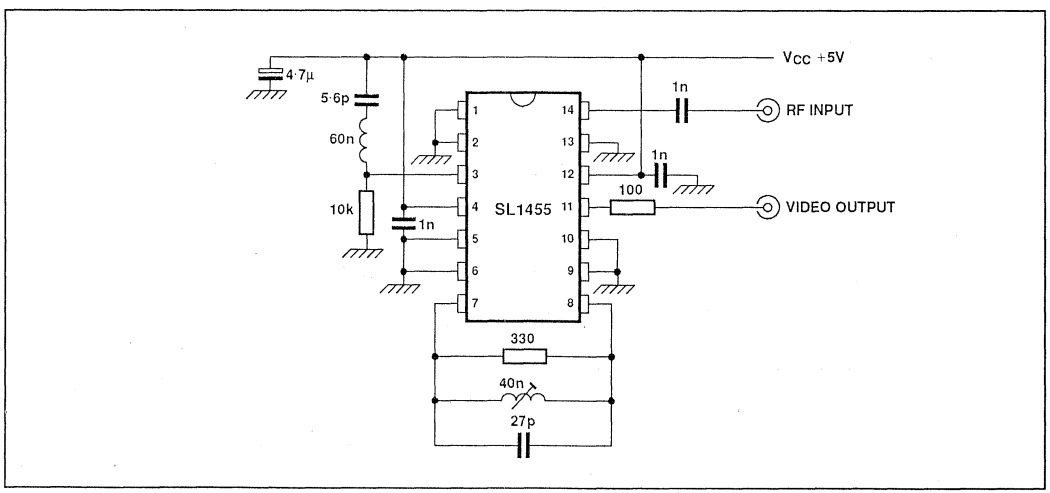


Fig. 3 Typical application: 612MHz threshold extended demodulator

SL1461

WIDEBAND PLL FM DEMODULATOR

The SL1461 is a wideband PLL FM demodulator, intended primarily for application in satellite tuners.

The device contains all elements necessary, with the exception of external oscillator sustaining network and loop feedback components, to form a complete PLL system operating at frequencies up to 800MHz.

An AFC with window adjust is provided, whose output signal can be used to correct for any frequency drift at the head end local oscillator.

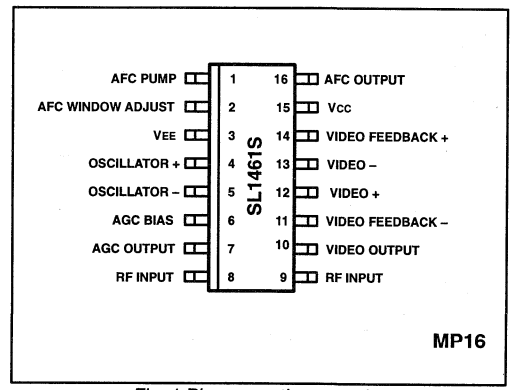


Fig. 1 Pin connections top view

FEATURES

- Single chip PLL system for wideband FM demodulation
- Simple low component count application
- Allows for application of threshold extension
- Fully balanced low radiation design
- High operating input sensitivity
- AGC detect and bias adjust
- 75Ω video output drive with low distortion levels
- Dynamic self biasing analog AFC
- Full ESD protection *

* Normal ESD handling procedures should be observed

APPLICATIONS

- Satellite receiver systems
- Data communications systems

ORDERING INFORMATION

SL1461S/KG/MPAS

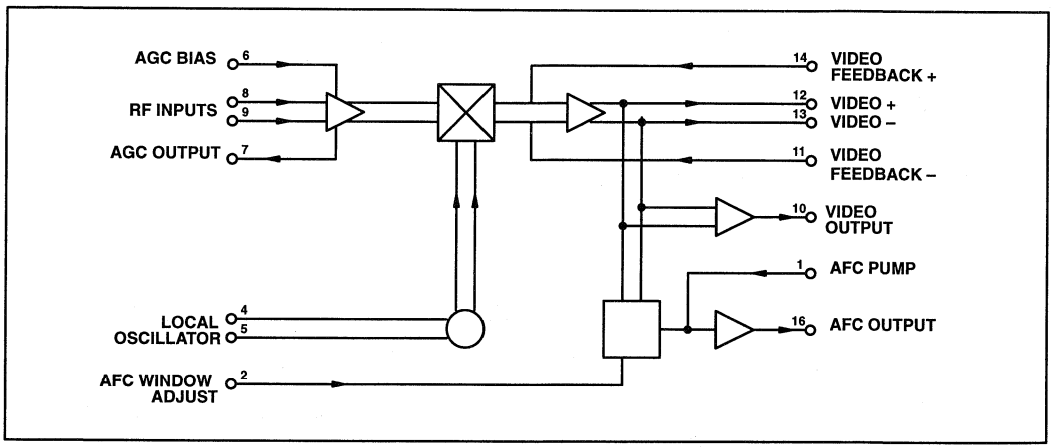


Fig. 2 SL1461 block diagram

ELECTRICAL CHARACTERISTICS

T_{amb}=–20°C to +80°C, V_{CC}=+4.5V to +5.5V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristics	Value			Units	Conditions
	Min	Typ	Max		
Supply current		36	40	mA	
Operating frequency	300		800	MHz	
Input sensitivity		–40		dBm	Preamp limiting
Input overload	0			dBm	
VCO sensitivity (dF/dV)	25	32	39	MHz/V	Refer to application in Fig. 3a
VCO linearity		.25		%	Refer to application in Fig. 3a; with 13.5MHz p–p deviation
Phase detector gain		0.5 0.25		V/rad V/rad	Differential loop filter Single ended loop filter
Loop amplifier input impedance	450	570	700	Ω	Single ended
Loop amplifier output impedance		25		Ω	Single ended
Loop amplifier open loop gain		38		dB	Single ended
Loop amplifier gain bandwidth product		240		MHz	Single ended
Loop amplifier output swing			1.2	Vp–p	Single ended
Video drive output impedance	55	75	95	Ω	
Video drive;					
Luminance nonlinearity		1.9	5	%	1KΩ load, See note 3 & 4
– differential gain		0.5	2.5	%	75Ω load, See note 3 & 4
– differential phase		1.0	3	Degree	75Ω load, See note 3 & 4
– intermodulation			–40	dB	See notes 1+3 & 4
– Signal/noise	66	72		dB	1KΩ load, See note 2 & 4
–Tilt		0.3	3	%	1KΩ load, See note 3 & 4
– baseline distortion		0.4	2	%	1KΩ load, See note 3 & 4
AGC output current	10		400	μA	Maximum load voltage drop 2V
AGC bias current	0		250	μA	
AFC window current	0		400	μA	400 μA gives 1.5V deadband window
AFC charge pump current		50		μA	
AFC leakage current			10	μA	With charge pump disabled
AFC output saturation voltage			0.4	V	AFC output enabled

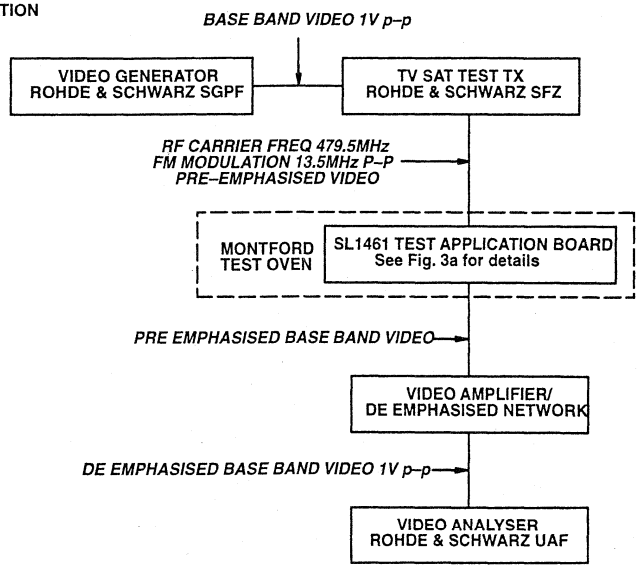
Note 1. Product of input modulation f_1 at 4.43MHz, 13.5MHz p–p deviation and f_2 at 6MHz p–p deviation, (PAL chroma and sound subcarriers).

Note 2. Ratio of output video signal with input modulation at 1MHz, 13.5MHz p–p deviation, to output rms noise in 6MHz bandwidth with no input modulation.

Note 3 Input test signal pre–emphasised video 13.5MHz p–p deviation. Output voltage 600mV pk–pk.

Note 4 See page 3

TEST CONFIGURATION



The video drive characteristics measurements were made using the above test configuration. The maximum figures recorded in the Electrical Characteristics Table coincide with high temperatures and extremes of supply voltage. No adjustment to the recorded figures has been made to compensate for the effects of temperature on the external components of the application test board, in particular the varactor diodes. If operation of the device at high ambient temperatures is envisaged then attention to temperature compensation of the external circuitry will result in performance figures closer to the stated typical figures.

Note 4.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} at 0V.

Characteristic	Min	Max	Units	Conditions
Supply voltage	–0.3	7	V	
RF input voltage		2.5	V p–p	
RF input DC offset	–0.3	V_{CC}+0.3	V	
Oscillator +&–DC offset	–0.3	V_{CC}+0.3	V	
Video +&–DC offset	–0.3	V_{CC}+0.3	V	
Video feedback +&–DC offset	–0.3	V_{CC}+0.3	V	
Video output DC offset	–0.3	V_{CC}+0.3	V	
AFC pump DC offset	–0.3	V_{CC}+0.3	V	
AFC disable DC offset	–0.3	V_{CC}+0.3	V	
AFC deadband DC offset	–0.3	V_{CC}+0.3	V	
AGC bias DC offset	–0.3	V_{CC}+0.3	V	
AGC output DC offset	–0.3	V_{CC}+0.3	V	
Storage temperature	–55	125	°C	
Junction temperature		150	°C	
MP16 package thermal resistance, chip to ambient		111	°C/W	

ABSOLUTE MAXIMUM RATINGS cont.

All voltages are referred to V_{EE} at 0V.

MP16 package thermal resistance chip to case		41	°C/W	
Power consumption at 5.5V		250	mW	
ESD protection – pins 1 to 15	2		kV	Mil–std –883 method 3015 class1
ESD protection – pin 16	1.7		kV	Mil–std –883 method 3015 class1

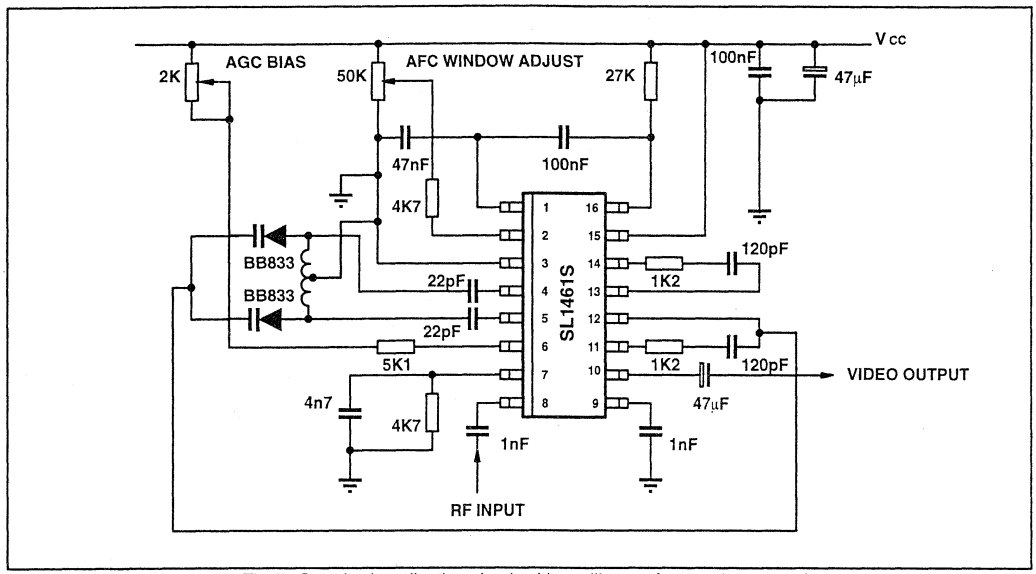


Fig.3. Standard application circuit with oscillator referenced to ground

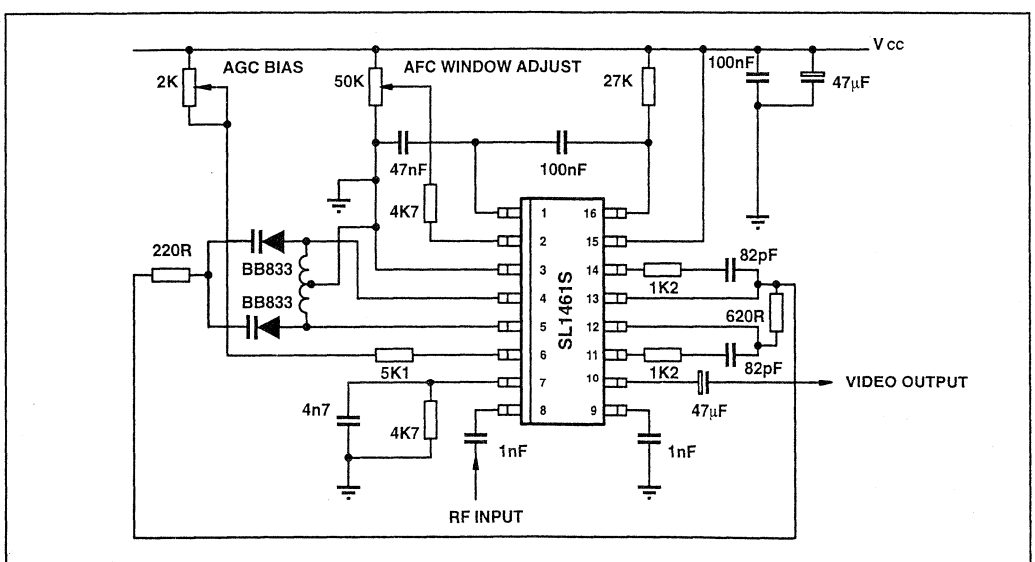


Fig.3a Application circuit used for video drive characterisation measurements

FUNCTIONAL DESCRIPTION

The SL1461 is a wideband PLL FM demodulator, optimised for application in satellite receiver systems and requiring a minimum external component count. It contains all the elements required for construction of a phase locked loop circuit, with the exception of tuning components for the local oscillator, and an AFC detector circuit for generation of error signal to correct for any frequency drift in the outdoor unit local oscillator. A block diagram is contained in Fig. 2 and the typical application in Fig. 3.

The internal pin connections are contained in Fig.6/6a.

In normal applications the second satellite IF frequency of typically 402 or 479.5MHz is fed to the RF preamplifier, which has a working sensitivity of typically –40 dBm, depending on application and layout. The preamplifier contains an RF level detect circuit, which generates an AGC signal that can be used for controlling the gain of the IF amplifier stages, so maintaining a fixed level to the RF input of the SL1461, for optimum threshold performance. The bias point of the AGC circuit can be adjusted to cater for variation in AGC line voltage requirement and device input power. The typical AGC curves are shown in Fig. 9.

The output of the preamplifier is fed to the mixer section which is of balanced design for low radiation. In this stage the RF signal is mixed with the local oscillator frequency, which is generated by an on–board oscillator. The oscillator block uses an external varactor tuned sustaining network and is optimised for high linearity over the normal deviation range. A typical frequency versus voltage characteristic for the oscillator is contained in Fig. 7. The loop output is designed to compensate for first order temperature variation effects; the typical stability is shown in Fig. 8

The output of the mixer is then fed to the loop amplifier around which feedback is applied to determine loop transfer characteristic . Feedback can be applied either in differential or single ended mode; if the appropriate phase detector gains are assumed in calculating loop filters, both modes should give the same loop response.

The loop amplifier drives a 75Ω output impedance buffer amplifier, which can either be connected to a 75Ω load or used to drive a high input impedance stage giving greater linearity and approximately 6dB higher demodulated signal output level.

DESIGN OF PLL LOOP PARAMETERS

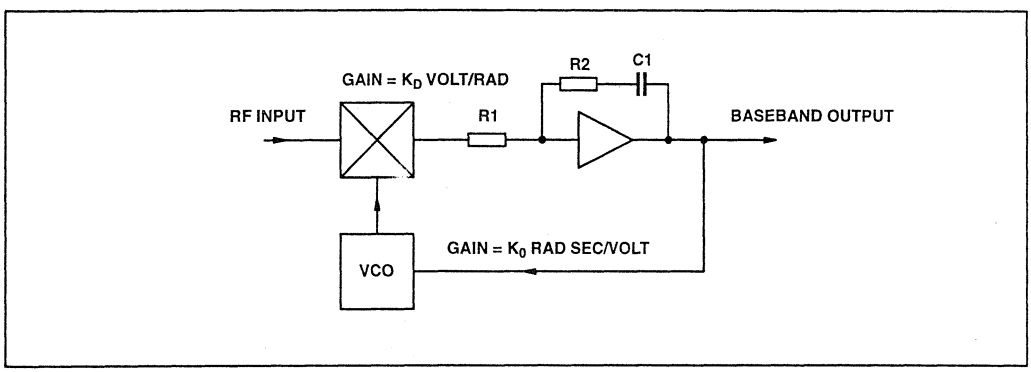


Fig. 4

The SL1461 is normally used as a type 1 second order loop and can be represented by the above diagram. For such a system the following parameters apply;

$$\tau_1 = C1 \cdot R1$$

$$\tau_2 = C1 \cdot R2$$

and

$$\tau_1 = \frac{K_0 K_D}{\omega_n^2}$$

$$\tau_2 = \frac{2\zeta}{\omega_n}$$

where:
K_0 is the VCO gain in radian seconds per volt
K_D is the phase detector gain in volts per radian
ω_n is the natural loop bandwidth
ζ is the loop damping factor
R1 is loop amplifier input impedance

Note: K_O is dependant on sensitivity of VCO used.
K_D = 0.25V/rad single ended, 0.5V/rad differential

From these factors the loop 3dB bandwidth can be determined from the following expression;

$$\omega_{3dB}^2 = \omega_n^2(2\zeta^2 + 1) \pm \omega_n^2\sqrt{(2\zeta^2 + 1)^2 + 1}$$

Which approximates to $\omega_{3dB} = 2\omega_n$ when $\zeta = \frac{1}{\sqrt{2}}$

AFC FACILITY

The SL1461 contains an analog frequency error detect circuit, which generates DC voltage proportional to the integral of frequency error. If the incident RF is high then the AFC voltage increases, if low then the voltage decreases. The AFC voltage can then be converted by an ADC to be read by the micro controller for frequency fine tuning; if used in an I^2C system it is recommended the device is used with either the SP5055 or SP5056 frequency synthesiser which contains an internal ADC readable via the I^2C bus.

The voltage corresponding to frequency alignment is arbitrary and user defined; if used with the SP5055 it is suggested the aligned voltage is 0.375 V_{CC}, corresponding to the centre code of the ADC on port 6.

The AFC detect circuit contains a deadband centred around the aligned frequency. The deadband can be adjusted from zero window to approximately 25MHz width assuming an oscillator dF/dV of 15MHz/V. If the incident RF is within this window the AFC voltage does not integrate, except by component leakage.

With reference to Fig.5; in normal operation the demodulated video is fed to a dual comparator where it is compared with two reference voltages, corresponding to the extremes of the deadband, or window. These voltages are variable and set by the window adjust input.

The comparators produce two digital outputs corresponding to voltages above or below the voltage window, or frequency above or below deadband. These digital control signals are used to control a complimentary current source pump. The current signals are then fed to the input of an amplifier which is arranged as an integrator, so integrating the pulses into a DC voltage.

If the frequency is correctly aligned both the current source and sink are disabled, therefore the DC output voltage remains constant. There will be a small drift due to component leakage; the maximum drift can be calculated from;

$$\frac{dV}{dt} = \frac{I}{2500 \cdot C} \quad \text{where} \quad I = \frac{V_{CC}}{R_{EXT}}, \quad C = C_{EXT}$$

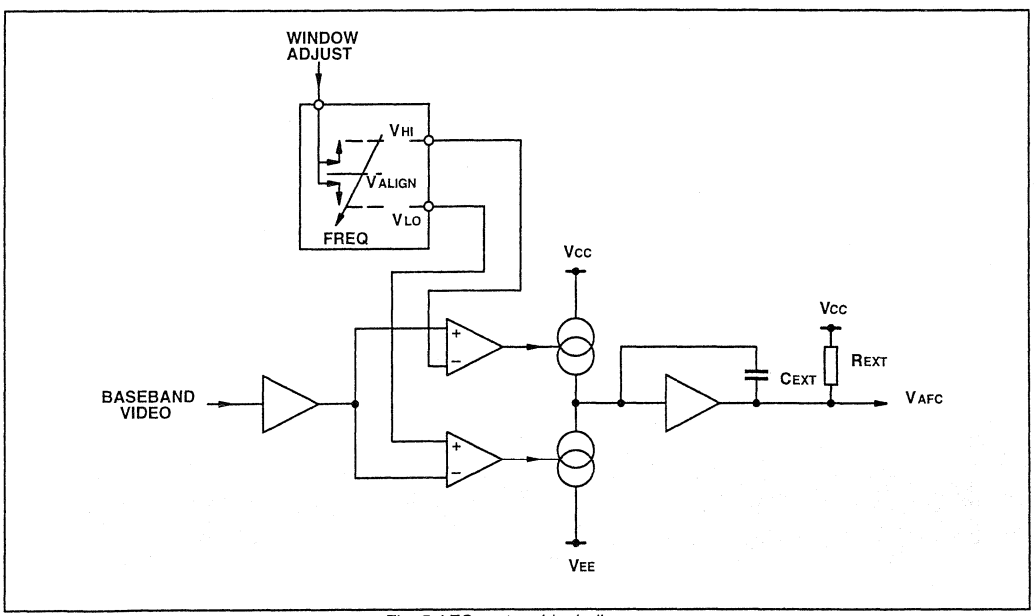
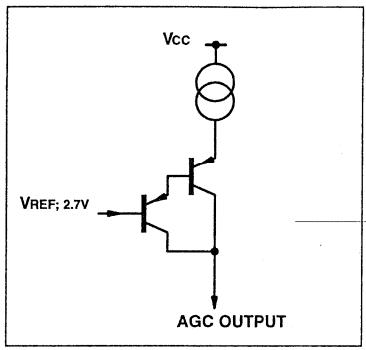
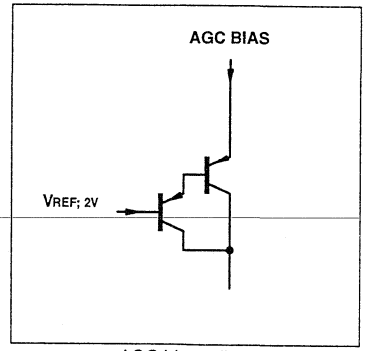


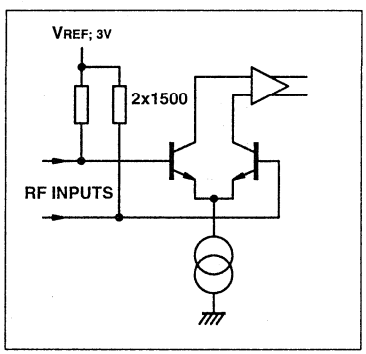
Fig. 5 AFC system block diagram



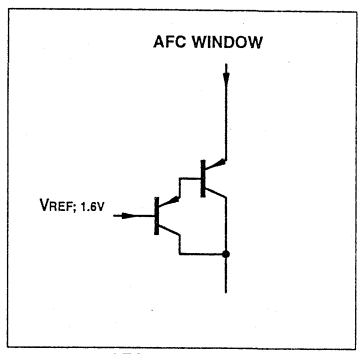
AGC output



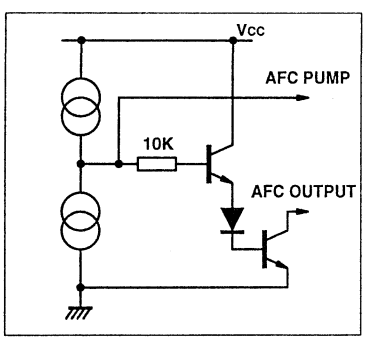
AGC bias adjust



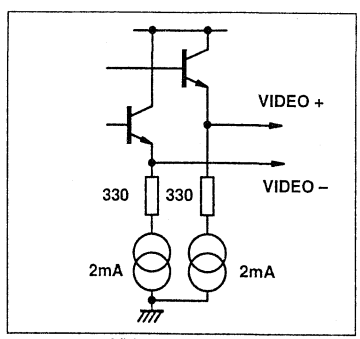
RF inputs



AFC window adjust

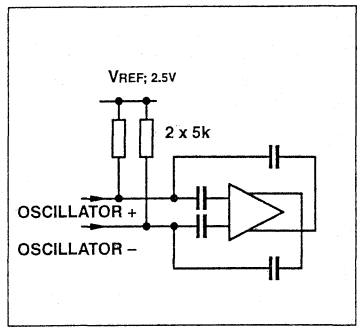


AFC output stage

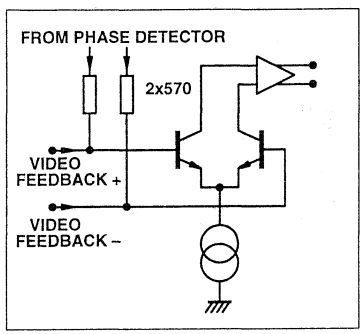


Video amp outputs

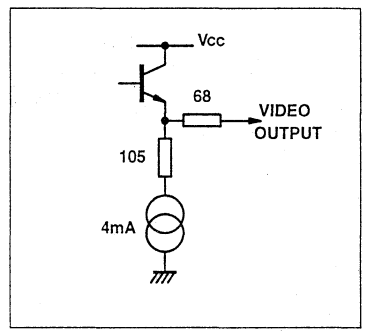
Fig.6 SL1461 I/O port internal circuitry



Local oscillator



Video amp feedback inputs



Video output drive

Fig. 6a SL1461 I/O port internal circuitry

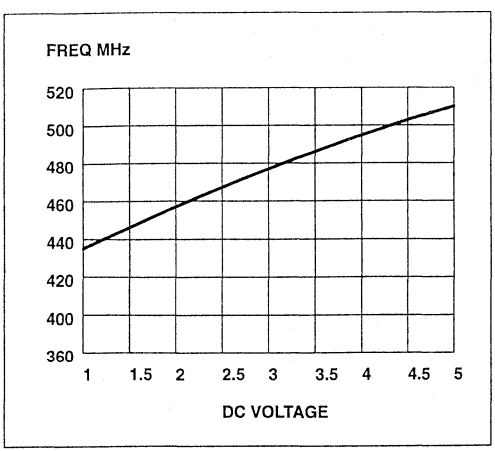


Fig. 7 Typical VCO frequency vs DC control voltage

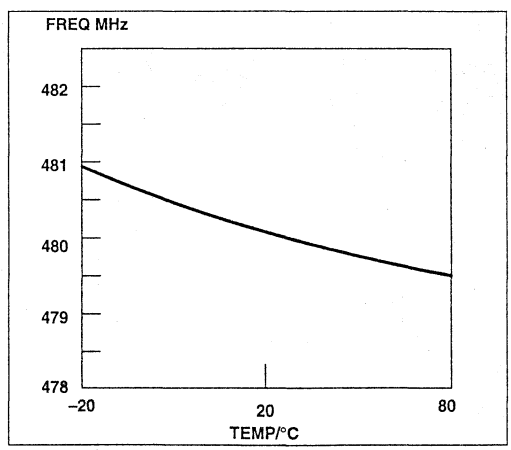


Fig. 8 SL1461 VCO centre frequency uncompensated temperature stability.

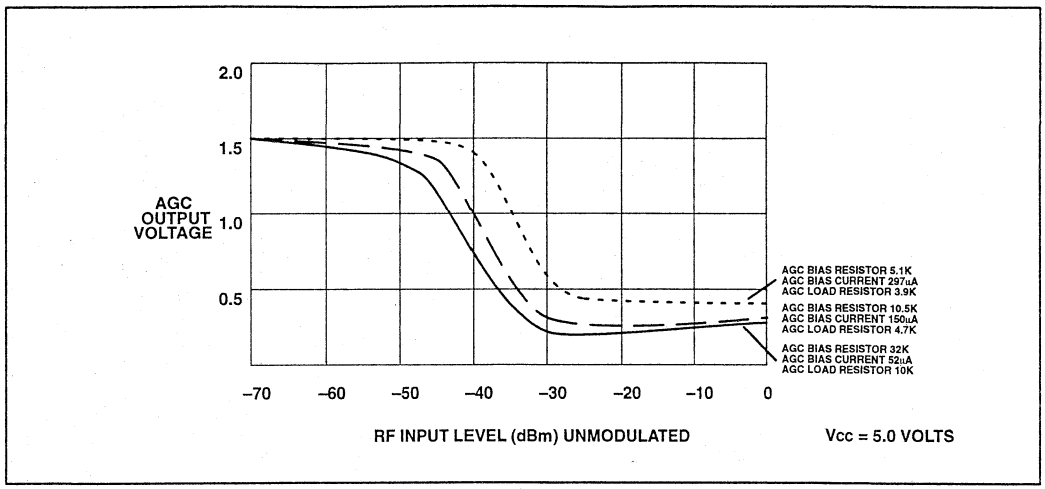


Fig.9 SL1461 AGC output voltage for differing values of AGC bias resistor

APPLICATION NOTES

Capture range

Under conditions when there is no RF input signal present, the SL1461 may react to spurious radiation from the free running oscillator coupling into the RF inputs. Because of the constant phase error between the VCO input to the phase detector and the spuriously coupled signal via the RF input, the phase comparator will drive the control voltage to either the bottom or the top of the range.

In such a case, the capture range will be asymmetrical about the VCO free running frequency, since any control voltage will only be able to tune the VCO in one direction if the tuning voltage is already at the max or min.

This effect can be avoided by driving the RF input differentially or achieving good common mode rejection to the VCO signal.

The lock range is independant of the above effects and will be symmetric about the centre of the phase detector S–curve provided the VCO is correctly aligned.

EXAMPLE

Loop out of lock

Tuning voltage =4.3V (maximum)

frequency =520MHz (maximum

It is only possible to capture signals below this frequency since the VCO is already at its maximum frequency.

Testing of capture range should be done with the device operating under normal conditions. An input signal of between –35dBm to –10dBm is suitable for such a measurement.

Lock range

Lock range should be symmetric about the centre of the S–curve. When the oscillator is sitting in the centre of the S–curve, the two video outputs will be at the same DC voltage.

RF oscillator design

The standard application circuit for the SL1461 is shown in Fig.3 The layout of the VCO tank should follow normal good RF techniques – ie as compact as possible. This will minimise parasitics, thus giving improved VCO linearity and stability. The PCB layout used for testing purpose is shown in Fig. 11.

Setting up of oscillator

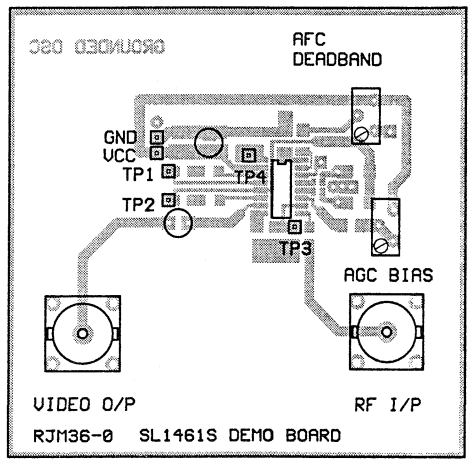
The VCO should be set up so that the desired input RF frequency is at the centre of the lock range. This will coincide with the centre of the S–curve and the point at which the AFC toggles when set to zero deadband.

The easiest way to centralise the VCO is to input an RF carrier which is being modulated by a low frequency squarewave. The tuning coil(s) should be adjusted until the AFC voltage toggles between 0.2V and $V_{CC-0.7V}$. The smaller the FM deviation of the squarewave used, the more accurate the setting will be.

A pre–emphasised video input containing black to white transitions can also be used for this setting, since the DC content in a pre–emphased video is much less than that in non pre–emphasised video. This is important as any dc content in the input waveform will introduce an offset in the AFC transition point.

The setting can be confirmed by measuring the DC voltage on the two video outputs, the voltages should be the same when the oscillator is centred around the incoming frequency. This DC measurement must be carried out with an unmodulated carrier of the required frequency. Modulation must not be present, since by definition, the dc voltages would be changing, thus making accurate measurement difficult.

NOTES
Circuit schematic is shown in Fig. 3.



TP1=VIDEO –
TP2=VIDEO +
TP3=AGC O/P
TP4=AFC O/P

All surface mount components mounted on underside of board

Fig. 11 Layout of demo board with oscillator referenced to GND

Section 5

Teletext and TV Signal Generators

GEC PLESSEY
SEMICONDUCTORS

MV1815

SINGLE CHIP TELETEXT DECODER FOR 625 LINE OPERATION

(Superseds June 1990 Edition and Version in Satellite, Cable and T.V. Handbook October 1988)

The MV1815 is an advanced CMOS single chip Teletext decoder for 625 line World System Teletex. The MV1815 has an on–chip data slicer circuit, dual page acquisition circuits, and direct memory addressing which allow a low cost Teletext decoder to be built with a minimum number of additional components.

FEATURES

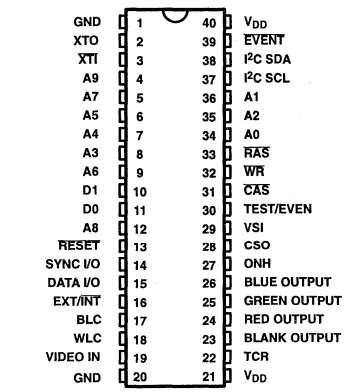
- On–Chip data slicing
- Up to 254 display pages stored, using low cost 150ns DRAMS
- Low external component count
- I²C Bus for low cost interfacing
- Multi–language capability for fourteen European languages
- Special parity inhibit for TOP 8–bit data
- Non–display packets stored for linked page operation, video programming, etc.
- high resolution characters typically 12 dots wide on a 15 by 10 matrix
- Accepts all non–display packets
- On–chip video switch
- Advanced CMOS technology gives low power disipation and high reliability

ABSOLUTE MAXIMUM RATINGS

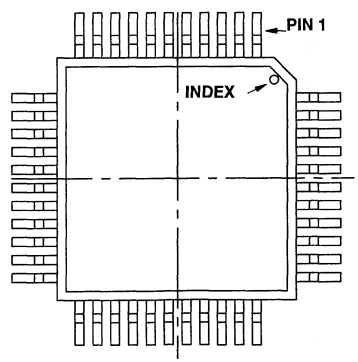
Supply Voltage, V_{DD}	–0.3V to +7.0V
All inputs	–0.3V to V_{DD} + 0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	–65°C to + 150°C

ORDERING INFORMATION

MV1815–2 BA DP	West European version
MV1815–2 BA GP/GPTJ	West European version
MV1815–3 BA DP	West & East European version



DP40



GP44

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	A1	16	D1	31	BLANK
2	SCL	17	D0	32	RED
3	SDA	18	A8	33	GREEN
4	N/C	19	N/C	34	BLUE
5	EVENT	20	RESET	35	OHN
6	V_{DD}	21	SYNC I/O	36	CSO
7	GND	22	DATA I/O	37	VSI
8	XTO	23	EXT/INT	38	N/C
9	XTI	24	BLC	39	TEST/EVEN
10	A9	25	WLC	40	CAS
11	A7	26	VIDEO	41	WR
12	A5	27	GND	42	RAS
13	A4	28	V_{DD}	43	A0
14	A3	29	TCR	44	A2
15	A6	30	N/C		

Fig. 1 Pin connections – top view

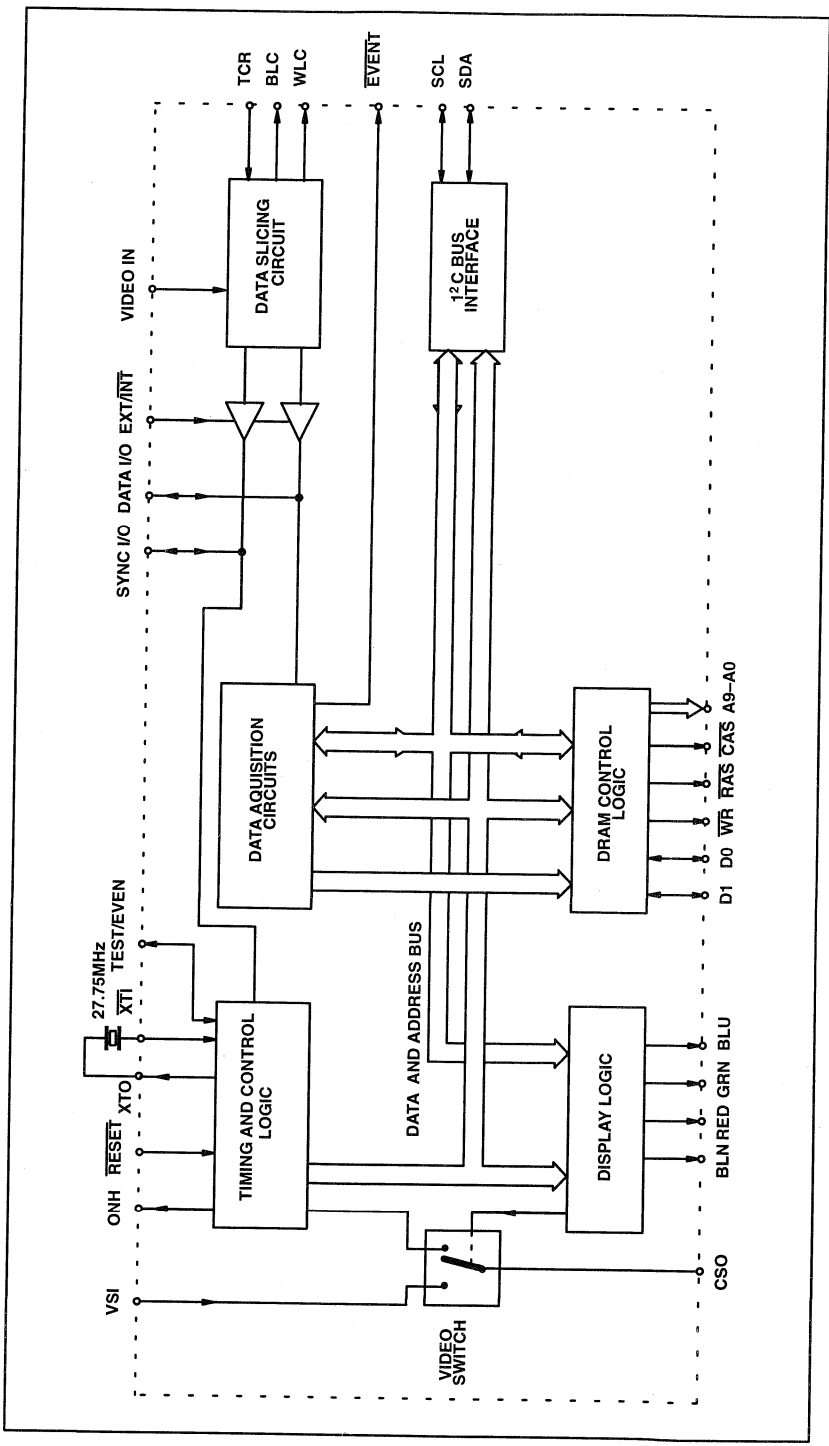


Fig. 2 MV1815 block diagram

<table>
<tr><th>Section</th><th>Specification</th></tr>
<tr><td>Data Acquisition Logic
Line Standard
Teletext data rate
Data line content
TV lines used VBI
TV lines used full field
Packets accepted
Page numbers
Page subcodes</td><td>
625 Lines 50 Fields/second
6.9375 Mbits/sec ±25ppm
360 bits as 45 bytes of 8 bits each
Lines 6 to 22 and 318 to 335
All TV Lines
×/0 to ×/25, ×/26, ×/27, ×/28, ×/29, ×/30 (all formats), ×/31
000 to 7FF
0000 to 3F7F</td></tr>
<tr><td>Display Logic
Characters per row
Teletext rows displayed

TV lines used

Character definition
Character Sets

Spacing control characters

Data boxing into picture

Displayable page stores

Display options</td><td>
40, occupying 43.24µs of the 52µs display time
0 to 23 with 24 and 25 software programmable

<table><tr><th rowspan="2">Rows Displayed</th><th colspan="2">TV Lines</th></tr><tr><th>Start</th><th>Finish</th></tr><tr><td>24</td><td>48</td><td>287</td></tr><tr><td>25 or 26</td><td>38</td><td>297</td></tr></table>
15 × 10 dot matrix
English, German, Swedish, Italian, French, Spanish,Czechoslovakian, Polish, Romanian, Hungarian, Turkish, Danish, Serbo–Croat, ASCII
Standard Level One Range

Page Number – Row 0 characters 1 to 8
Page Header – Row 0 characters 9 to 32
Clock Time – Row 0 characters 33 to 40
Rows 24 and 25
Up to 254 pages, each of 1k bytes, depending on the size of the DRAM being used

Mix of text foreground and picture background
Three part magnify – display rows 0 to 11 double height
display rows 6 to 17 double height
display rows 12 to 23 double height
Boxing of Newsflash and Subtitles into picture
Boxing of picture into text</td></tr>
<tr><td>Dynamic RAM Control Logic
Memory Configuration

Maximum access time (t_{RAC})
Refresh period for complete memory</td><td>
All sizes: Page or nibble mode types
254 pages – 2 off 1M × 1 or 1 off 1M × 4
62 pages – 2 off 256k × 1 or 1 off 256k × 4
14 pages – 2 off 64k × 1 or 1 off 64k × 4
150ns
2.048ms
Refresh occurs during the line flyback period. Contents of any memory location may be accessed by the microprocessor via the I²C Bus Interface</td></tr>
<tr><td>I²C Bus Interface</td><td>
Standard implementation of a slave transmitter/receiver Control of the MV1815 is via the I²C Bus Interface</td></tr>
<tr><td>I²C Bus Address</td><td>
0010 001 R/$\overline{W}$</td></tr>
</table>

Table 1. MV1815 System specification

PIN DESCRIPTION		
Symbol	Pin No (DP 40)	Pin name and Description
GND	1, 20	Ground, both pins must be connected
XTO	2	Crystal out 27.75MHz fundamental crystal with an on–chip 1MΩ bias resistor to $\overline{\text{XTI}}$
$\overline{\text{XTI}}$	3	Crystal input
A9, A7, A5, A4, A3, A6, A8, A0, A2, A1	4 – 9 12, 34, 35, 36	DRAM address outputs
D1, D0	10, 11	DRAM data lines. Internal 100kΩ pull – up resistors are included.
$\overline{\text{RESET}}$	13	Active low reset input. Includes 100kΩ pull – up resistor.
SYNC I/O	14	Sliced sync input / output.
DATA I/O	15	Teletext data input / output
EXT/$\overline{\text{INT}}$	16	Control pin for SYNC and DATA I/O. Includes 100kΩ pull–down resistor. When low or not connected internal SYNC and DATA are used, pins 14 & 15 are outputs. When high supply SYNC and DATA from an external source, pins 14 & 15 are inputs.
BLC	17	Black level capacitor.
WLC	18	White level capacitor
VIDEO IN	19	Input for composite video signal with negative going SYNCS.
VDD	21, 40	+5V Supply. Both pins must be connected.
TCR	22	Time constant resistor controlling discharge rate of black and white level capacitor voltages.
BLANK	23	Blanking output, high power push–pull driver.
RED	24	Red output, high power push–pull tri–state driver.
GREEN	25	Green output, high power push–pull tri–state driver.
BLUE	26	Blue output, high power push–pull tri–state driver.
ONH	27	On hours indicator. When high CSO is locked to Video In. When low CSO is not locked.
CSO	28	Generated composite sync output during text, video input is switched through to CSO during modes that contain picture content. See Fig. 6.
VSI	29	Video switch input.
TEST	30	Used for factory testing. Even output is enabled by bits IOE and EOE in SYNCSW register. If EVEN output is not used, the pin should be left open–circuit. A 100kΩ pull–down resistor is included.
$\overline{\text{CAS}}$	31	DRAM column address strobe.
$\overline{\text{WR}}$	32	DRAM read/not write signal.
$\overline{\text{RAS}}$	33	DRAM row address strobe.
I^2C SCL	37	I^2C bus serial clock.
I^2C SDA	38	I^2C bus bi–directional data port.
$\overline{\text{EVENT}}$	39	Active low open drain output interrupt signal to microprocessor.

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 27.750000MHz. AT cut

Tolerance overall ±100ppm.
Nominal load capacitance 20pF
Equivalent series resistance <20Ω

A variable capacitor is provided internally on pin $\overline{XTI}$ and controlled by a phase locked loop to provide exact trimming of the frequency. This will provide compensation for temperature variation and crystal ageing.

BIT POSITION												
ADDRESS		REGISTER	7	6	5	4	3	2	1	0	R/W	RESET STATE
DEC	HEX											HEX
		RADD	A17	A16	IAI	RA4	RA3	RA2	RA1	RA0	W	00
0	0	ACONA	ACQ	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
1	1	STORA	STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	W	02
2	2	PGS1A	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
3	3	PGS2A	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	20
4	4	PGS3A	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	00
5	5	ACONB	$\overline{HLD}$	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
6	6	STORB	STB7	STB6	STB5	STB4	STB3	STB2	STB1	STB0	W	03
7	7	PGS1B	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
8	8	PGS2B	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBA0	W	00
9	9	PGS3B	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	88
10	A	RECON	WI0	WI24	WI25	PIN B	PIN A	FF	CDB	CDA	W	00
11	B	DISCON1	INV	RLH	DSB	CLS	CUR	BLC	LS3	UDI	W	00
12	C	DISCON2	LSO	LS1	LS2	MGS	IHD	SPH	BX1	BX0	W	00
13	D	DISCON3	TXT	MIX	INT	REV	UDK	SPOS	ST2	ST1	W	00
14	E	DISCON4	BXP	BXH	BXT	BXS	DHT	DHB	SG2	SG1	W	00
15	F	HADD	A15	A14	A13	A12	A11	A10	A9	A8	W	00
16	10	LADD	A7	A6	A5	A4	A3	A2	A1	A0	W	00
17	11	WDATA	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	W	00
19	13	SCROLL	WI29	MV	CRL	SRA4	SRA3	SRA2	SRA1	SRA0	W	00
20	14	SYNCSW	ESS	–	–	–	IOE	EOE	SEN	SVS	W	00
0	0	EVENTA	NPR	VHR	830A	X/29	X/28	X/27	X/26	C8	R	–
1	1	EVENTB	NPR	VHR	830B	X/29	X/28	X/27	X/26	C8	R	–
2	2	CBITSA	C14	C13	C12	C11	C10	C7	C6	C5	R	–
3	3	PGR1A	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
4	4	PGR2A	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
5	5	PGR3A	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
6	6	CBITB	C14	C13	C12	C11	C10	C7	C6	C5	R	–
7	7	PGR1B	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
8	8	PGR2B	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
9	9	PGR3B	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
10	A	HAMMC	HC7	HC6	HC5	HC4	HC3	HC2	HC1	HC0	R	FF
17	11	RDATA	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	–

Table 2 MV1815 Register details

Note. Write register addresses 18, and 21–31 (12, and15–1F HEX) are reserved for future development and should not be used.

WRITE REGISTERS

RADD (W)

A16 / A17	Memory quadrant select
IAI	Inhibit auto increment
RA$	Register address ($=0 to 4)

ACON A/B (W 0 & 5)

ACQ	Aquisition on
MGC	Magazine compare
PAC	Page units compare
PBC	Page tens compare
SAC	Page subcode compare digit A
SBC	Page subcode compare digit B
SCC	Page subcode compare digit C
SDC	Page subcode compare digit D
HLD	Not hold display acquisition circuit

STOR A/B (W 1 & 6)

STA$	Store number for aquisition A ($=0 to 7)
STB$	Store number for aquisition B ($=0 to 7)

PGS /1/2/3 A/B (W 2,3 4 & 7,8,9)

SAS$	Sub–Code digit A ($=0 to 3) select
SBS$	Sub–Code digit B ($=0 to 2) select
SCS$	Sub–Code digit C ($=0 to 3) select
SDS$	Sub–Code digit D ($=0 or 1) select
PAS$	Page number (units) ($=0 to 3) select
PBS$	Page number (tens) ($=0 to 3) select
MS$	Magazine number ($=0 to 2) select

RECON (W 10)

WI0	Write inhibit of packet 0
WI24	Write inhibit of packet 24
WI25	Write inhibit of packet 25
PIN B	Parity check inhibit acquisition circuit B
PIN A	Parity check inhibit acquisition circuit A
FF	Full field Teletext
CDB	Clear store disable acquisition circuit B
CDA	Clear store disable acquisition circuit A

DISCON1 (W 11)

INV	Invert display
RLH	Roll headers
DSB	Display acquisition circuit B (A if zero)
CLS	Clear current display store
CUR	Cursor enable
BLC	Block cursor
LS3	Language group select
UDI	Dispaly update indicator

DISCON2 (W 12)

LS$	Language select ($=0 to 2)
MGS	Magazine serial
IHD	Inhibit display, rows 2 to 26 disabled
SPH	Suppress header
BX$	Box control bits ($=0 or 1)

DISCON3 (W 13)

TXT	Text / not picture
MIX	Mix text and picture
INT	Display text in interlace mode (see Figure 6)
REV	Reveal hidden text
UDK	Update key, rows 1 to 26 disabled.
SPOS	Status line position
ST2	Display Status line 2 (row 26)
ST1	Display Status line 1 (row 25)

WRITE REGISTERS

DISCON4 (W 14)

BXP	Box page number
BXH	Box header
BXT	Box time
BXS	Box status rows
DHT	Double height top half
DHB	Double height bottom half
SG$	Seperate graphics control bits ($=0 or 1)

HADD and **LADD** (W 15 & 14)

A$	Memory address ($=0 to 15)

WDATA (W 17)

WD$	Data to be written to memory ($=0 to 7)

SCROLL (W 19)

WI29	Write inhibit of packet 29
MV	Majority vote on framing code
CRL	Cursor lock at last HADD. LADD setting
SRA$	Scroll display row up ($=0 to 4)

SYNCSW (W 20)

ESS	External sync source
IOE	Internal output enable
EOE	Even output enable
SEN	Select enable – SVS bit
SVS	Select VSI as sync source

READ REGISTER

EVENT A/B (R 0 & 1)

NPR	New page received
VHR	Valid header received
830$	Packet 30 received aquisition $ ($=A or B)
X/29	Packet 29 received
X/28	Packet 28 received
X/27	Packet 27 received
X/26	Packet 26 received
C8	Update Indicator

CBITS A/B (R 2 & 6)

C14	Language select bit
C13	Language select bit
C12	Language select bit
C11	Magazine serial
C10	Inhibit display
C7	Supress header
C6	Sub–title
C5	Newsflash

PGR/1/2/3/A/B (R 3,4,5 & 7,8,9)

SAR$	Sub–code digit A ($=0 to 3) received
SBR$	Sub–code digit B ($=0 to 2) received
SCR$	Sub–code digit C ($=0 to 3) received
SDR$	Sub–code digit D ($=0 or 1) received
PAR$	Page number (units) ($=0 to 3) received
PBR$	Page number (tens) ($=0 to 3) received
MR$	Magazine number ($=0 to 2) received

HAMMC (R 10)

HC$	Hamming counter ($=0 to 7)

RDATA (R 17)

RD$	Data read from memory ($=0 to 7)

I²C BUS

Device Address **0010 001 R/$\overline{W}$**

The circuit works as a slave transmitter with bit eight set high or as a slave receiver with bit eight low. In receive mode, the first data byte is written to the RADD register, where the least significant five bits from the sub–address for the next register to be written. The most significant three bits of RADD are data bits, see Table 2.

Automatic incrementing of registers allows successive data bytes to be written to or read from the registers. The automatic incrementing can be disabled by setting bit 5 of the sub–address register (RADD) to one.

If the sub–address is set to write or read from DRAM, the auto incrementing allows access to successive bytes of data. All DRAM addresses may be accessed via the I²C bus register. A stop condition resets the sub–address to zero.

Example of I²C Bus Messages

Write operation – MV1815 as a slave receiver

S	MV1815 ADD	W	A*	RADD (n)	A*	DATA (reg n)	A*	DATA (reg n + 1)	A*	P

Read operation – MV1815 as a slave transmitter

S	MV1815 ADD	R	A*	DATA * (reg 0)	A	DATA * (reg 1)	A	DATA * (reg 2)	A	P

S Start Conditions
P Stop Condition
A Acknowledge
W Write (=0)
R Read (=1)
* MV1815 output

Write/read operation – MV1815 as a slave transmitter sending data from register n etc.

S	MV1815 ADD	W	A*	RADD (reg n)	A*	S	MV1815 ADD	R	A*	DATA* (reg n)	A	DATA (reg n + 1)	A	P

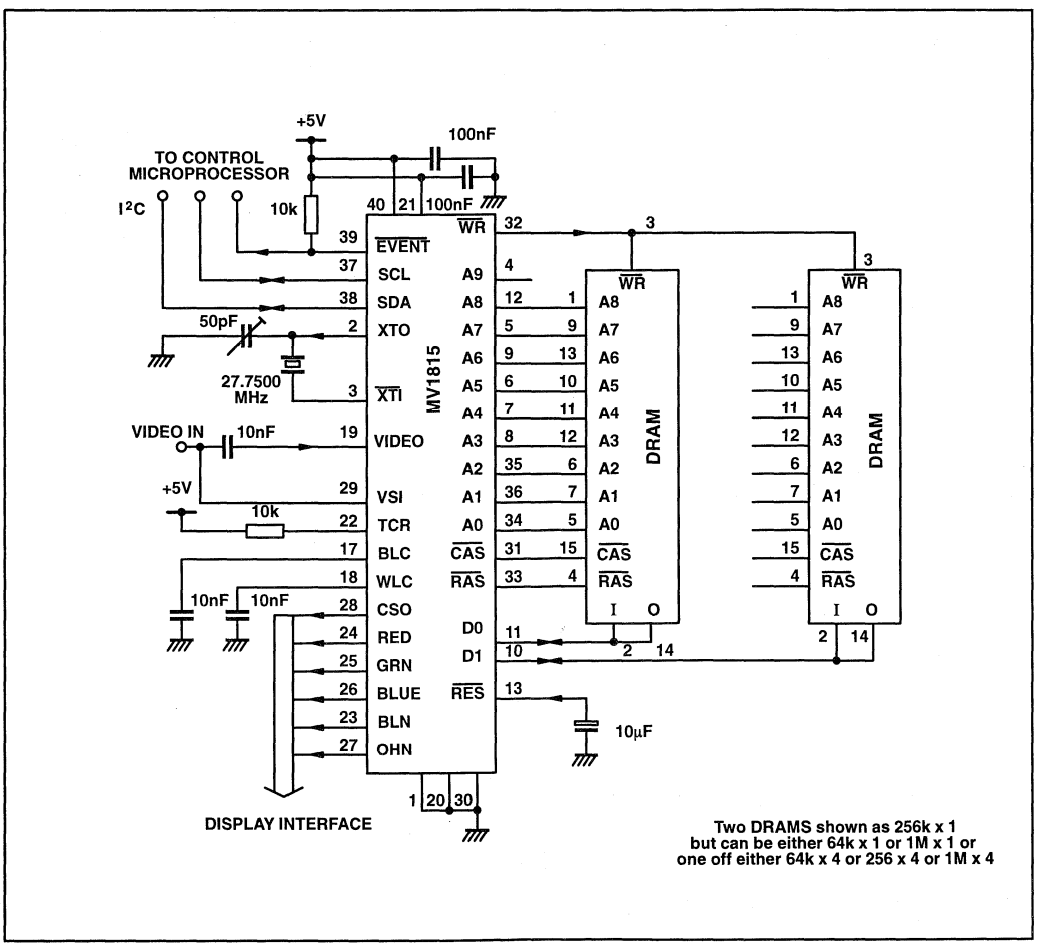


Fig. 3. MV1815 Typical application

DRAM Memory Organisation

The DRAM as viewed from the I²C Bus is organised in 1024 byte blocks. Each 1024 bytes (400 HEX) block is referred to as a store. Stores 0 and 1 are reserved for the non–display packets from acquisition A and B respectively. Stores 2 and above are used for display pages, one page per store

The display page number, first 8 bytes on row 0, are held in Store 0 bytes 0 to 7. The Time display, last 8 bytes on row 0 are also held in store 0 bytes 8 to F (HEX). See Figs. 4 and Figs. 5

To calculate the values of the start address in RADD, HADD and LADD for any store simply multiply the store number (HEX) by 400 (HEX)

e.g. Decimal store 160 = A0

A0 x 400 = 2 80 00 (HEX)

RADD HADD LADD

To find the address of any particular location in the store add the value of the relative address from Fig. 4 or 5.

Table 3 gives examples of the start addresses of stores expressed as values of A17, A16 from RADD, A15–A8 from HADD and A7–A0 from LADD.

STORE NUMBER HEX	START ADDRESS IN HEX		
	RADD	HADD	LADD
00	0	00	00
01	0	04	00
02	0	08	00
03	0	0C	00
04	0	10	00
05	0	14	00
06	0	18	00
07	0	1C	00
08	0	20	00
:		:	
0F	0	3C	00
10	0	40	00
:		:	
40	1	00	00
41	1	04	00
:		:	
7F	1	FC	00
80	2	00	00
:		:	
F0	3	C0	00
:		:	
FF	3	FC	00

Table 3

Display Row	First byte Relative Address HEX		Last byte Relative Address HEX
0	000	NOTE 1 / PACKET 0 24 byte / NOTE 2	017
1	018	PACKET 1 40 bytes	03F
2	040		
3	068		
4	090		
5	0B8		
6	0E0		
7	108		
8	130		
9	158		
10	180		
11	1A8		
12	1D0	PACKETS 2 – 23	
13	1F8		
14	220		
15	248		
16	270		
17	298		
18	2C0		
19	2E8		
20	310		
21	338		
22	360		
23	388		
24	3B0	PACKET 24	
25	3D8	PACKET 25	3FF

Fig. 4 Organisation of Display Memory. Stores 2 to 256

NOTE 1. Display of page number here, 8 bytes which are located in store 0 with absolute addresses 000 to 007.
NOTE 2. Display of time here, 8 bytes which are located in store 0 with absolute addresses 008 to 00F

First byte Absolute Address HEX	Page Number Add 0 – 7	Time Add 8 – F	Packet X/31 Add 10 – 17	Last byte Absolute Address HEX
00018				0003F
00040				
00068				
00090				
000B8				
000E0				
00108				
00130				
00158				
00180				
001A8				
001D0	ACQUISITION A PACKET X/26, X/27 OR X/28 IN ANY ORDER UP TO 23 PACKETS			
001F8				
00220				
00248				
00270				
00298				
002C0				
002E8				
00310				
00338				
00360				
00388				
003B0	PACKET X/29			
003D8	PACKET 8/30			003FF

Fig. 5. Store 0 memory organisation

Packet 8/30 designation codes 0,1,4,5,8,9, C and D are written to store 0.

NOTE: Store 1 is organised similarly except that it accepts aquisition circuit B packets X/26, etc. The starting address is 00400 (HEX) and bytes 00400 to 00417 (HEX) are not used by the MV1815. All addresses shown in Fig. 5 add 00400 (HEX).
Packet 8/30 designation codes 2,3,6,7, A,B,E and F are written to store 1.

	0	1
0	Alpha Black	Graphic Black
1	Alpha Red	Graphic Red
2	Alpha Green	Graphic Green
3	Alpha Yellow	Graphic Yelow
4	Alpha Blue	Graphic Blue
5	Alpha Magenta	Graphic Magenta
6	Alpha Cyan	Graphic Cyan
7	Alpha White[1]	Graphic White
8	Flash	Conceal Display [2]
9	Steady [1 2]	Contiguous Graphics [1 2]
A	End Box [1 2]	Separated Graphics [2]
B	Start Box [3]	No action
C	Normal Height [1 2]	Black Background [1 2]
D	Double Height	New Background [2]
E	No action	Hold Graphics
F	No action	Release Graphics [1]

Table 4 Control codes

Notes: 1. Presumed set at the start of each display row.

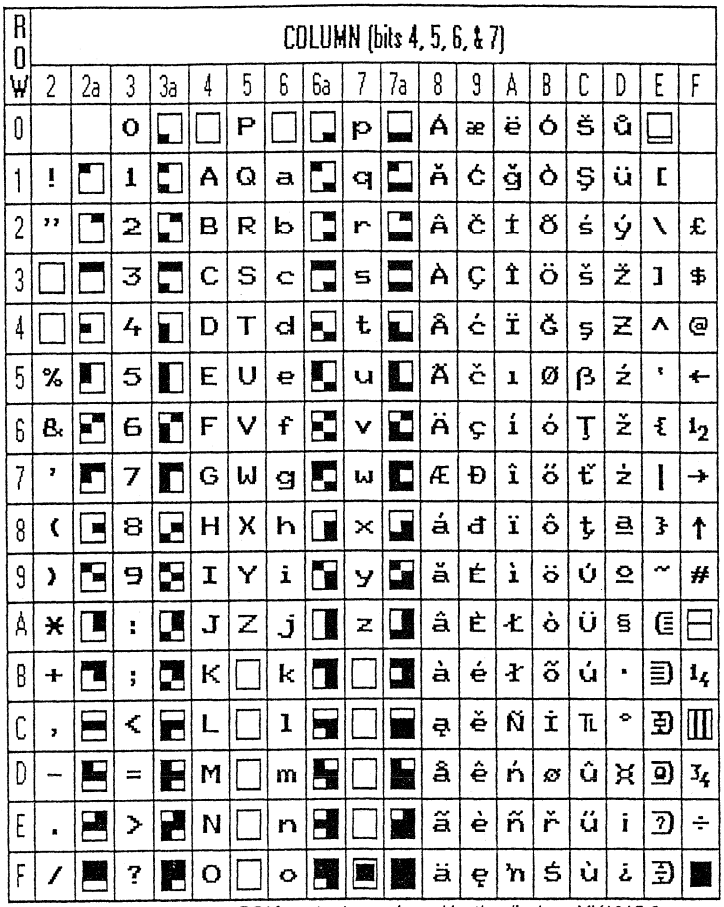
2 Action "set at the curent space", others are "set after the current space".

3. Two consecutive codes are transmitted, action takes place between them.

LS(3210)	0000	0001	0010	0011	0100	0101	0110	0111
TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH	ENGLISH
2/3	£	#	#	£	é	ç	#	£
2/4	$	$	¤	$	ï	$	ů	$
4/0	@	§	É	é	à	¡	č	@
5/B	←	Ä	Ä	°	ë	á	ť	←
5/C	½	Ö	Ö	ç	ê	é	ž	½
5/D	→	Ü	Å	→	ù	í	ý	→
5/E	↑	^	Ü	↑	î	ó	í	↑
5/F	#	_	_	#	#	ú	ř	#
6/0	■	°	é	ù	è	¿	é	■
7/B	¼	ä	ä	à	â	ü	á	¼
7/C	▮	ö	ö	ò	ô	ñ	ě	▮
7/D	¾	ü	å	è	û	è	ú	¾
7/E	÷	ß	ü	ì	ç	à	š	÷

LS(3210)	1000	1001	1010	1011	1100	1101	1110	1111
TABLE POSITION	POLISH	ROMANIAN	HUNGARIAN	TURKISH	DANISH	SERBO CROAT	ASCII	SOUTH AFRICAN
2/3	#	#	#	₺	£	#	#	£
2/4	ń	¤	ú	ğ	$	$	$	$
4/0	ą	Ţ	É	İ	@	Č	@	ħ
5/B	Ź	Â	í	Ş	Æ	Ć	[	ë
5/C	ś	Ş	Ö	Ö	Ø	Ž	\	ê
5/D	Ł	ă	Á	Ç	Å	Đ	]	ü
5/E	ć	î	ű	Ü	↑	Š	^	é
5/F	ó	ı	ő	ğ	#	ë	_	ï
6/0	ę	ţ	é	ı	■	č	`	š
7/B	ż	â	ó	ş	æ	ć	{	ä
7/C	ś	ş	ö	ö	ø	ž	▯	ô
7/D	ł	ă	á	ç	å	đ	}	û
7/E	ź	î	ü	ü	÷	š	~	ö

Table 5. Western European national optional variations - MV1815-2.



ROW	COLUMN (bits 4, 5, 6, & 7)																	
	2	2a	3	3a	4	5	6	6a	7	7a	8	9	A	B	C	D	E	F
0			0	□	□	P	□	□	p	□	Á	æ	ë	ó	š	ů	□	
1	!	□	1	□	A	Q	a	□	q	□	Ă	ć	ğ	ò	Ş	ü	[	
2	"	□	2	□	B	R	b	□	r	□	Â	č	ł	ő	ś	ý	\	£
3	□	□	3	□	C	S	c	□	s	□	À	Ç	î	ö	š	ž	]	$
4	□	□	4	□	D	T	d	□	t	□	Â	ć	Ï	Ğ	ş	Ź	^	@
5	%	□	5	□	E	U	e	□	u	□	Ä	č	ı	Ø	ß	ź	'	←
6	&	□	6	□	F	V	f	□	v	□	Ä	ç	í	ó	Ţ	ž	ł	½
7	'	□	7	□	G	W	g	□	w	□	Æ	Đ	î	ő	ť	ż	|	→
8	(	□	8	□	H	X	h	□	x	□	á	đ	ï	ô	ţ	ą	}	↑
9	)	□	9	□	I	Y	i	□	y	□	ă	É	ì	ö	Ú	°	~	#
A	*	□	:	□	J	Z	j	□	z	□	â	È	Ł	ò	Ü	ß	□	□
B	+	□	;	□	K	□	k	□	□	□	à	é	ł	ő	ú	·	□	¼
C	,	□	<	□	L	□	l	□	□	□	ą	ě	Ń	İ	Ţ	°	□	□
D	–	□	=	□	M	□	m	□	□	□	â	ê	ń	ø	û	□	□	¾
E	.	□	>	□	N	□	n	□	□	□	ã	è	ń	ř	ű	i	□	÷
F	/	□	?	□	O	□	o	□	□	□	ä	ę	ń	ś	ù	¿	□	□

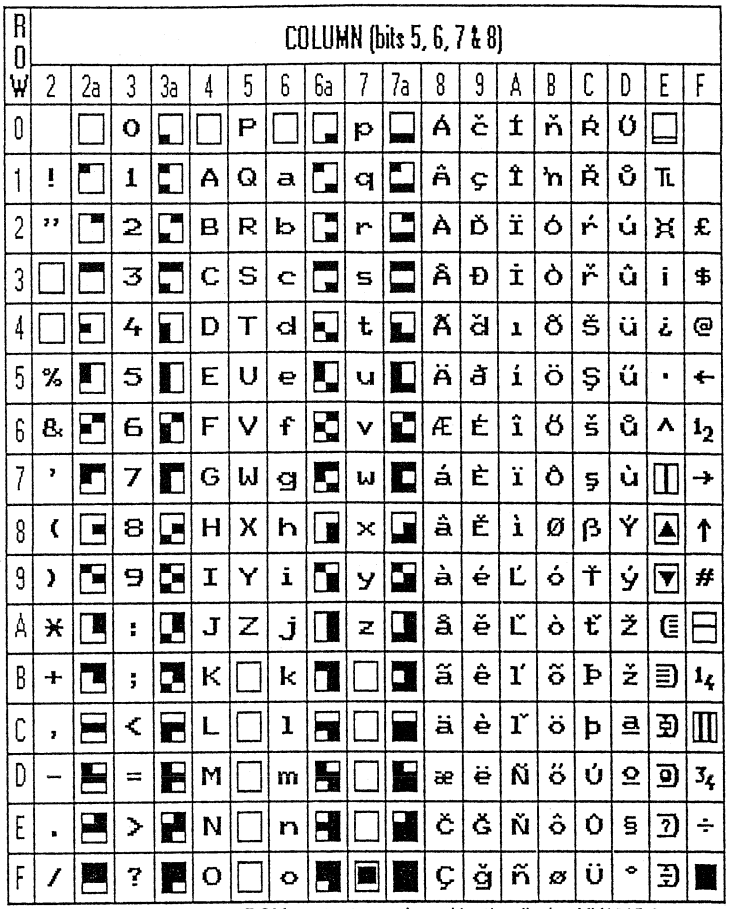
Table 6. Character ROM contents as viewed by the display - MV1815-2.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes. like the control columns 0 and 1 listed in table 4.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
□ Characters in these positions are displayed according to the setting of LS(0-3) bits, see table 5. When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

LS(3210)	0000	0001	0010	0011	0100	0101	0110	0111
TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH	ENGLISH
2/3	£	#	#	£	é	ç	#	£
2/4	$	$	¤	$	ï	$	û	$
4/0	@	§	É	é	à	¡	č	@
5/B	←	Ä	Ä	°	ë	á	ť	←
5/C	½	Ö	Ö	ç	ê	é	ž	½
5/D	→	Ü	Å	→	ù	í	ý	→
5/E	↑	^	Ü	↑	î	ó	í	↑
5/F	#	_	_	#	#	ú	ř	#
6/0	■	°	é	ù	è	¿	é	■
7/B	¼	ä	ä	à	â	ü	á	¼
7/C	▮	ö	ö	ò	ô	ñ	ě	▮
7/D	¾	ü	å	è	û	è	ú	¾
7/E	÷	ß	ü	ì	ç	à	š	÷

LS(3210)	1000	1001	1010	1011	1100	1101	1110	1111
TABLE POSITION	ENGLISH	GERMAN	HUNGARIAN	TURKISH	DANISH	SPANISH	CZECH	SOUTH AFRICAN
2/3	£	#	#	₺	£	ç	#	£
2/4	$	$	ú	ğ	$	$	û	$
4/0	@	§	É	İ	@	¡	č	ŉ
5/B	←	Ä	í	Ş	Æ	á	ť	ë
5/C	½	Ö	Ö	Ö	Ø	é	ž	ê
5/D	→	Ü	Á	Ç	Å	í	ý	ü
5/E	↑	^	ű	Ü	↑	ó	í	é
5/F	#	_	ő	Ğ	#	ú	ř	ï
6/0	■	°	é	ı	■	¿	é	š
7/B	¼	ä	ó	ş	æ	ü	á	ä
7/C	▮	ö	ö	ö	ø	ñ	ě	ô
7/D	¾	ü	á	ç	å	è	ú	û
7/E	÷	ß	ü	ü	÷	à	š	ö

Table 7. West and East European national optional variations MV1815-3.



ROW	COLUMN (bits 5, 6, 7 & 8)																	
	2	2a	3	3a	4	5	6	6a	7	7a	8	9	A	B	C	D	E	F
0			0			P			p		Á	č	ť	ň	Ŕ	Ú		
1	!		1		A	Q	a		q		Â	ç	ţ	ň	ř	Ű	Ţ	
2	"		2		B	R	b		r		Ä	Ď	Ï	ó	ŕ	ú	¤	£
3			3		C	S	c		s		Ă	Đ	ł	ô	ř	ű	¡	$
4			4		D	T	d		t		Ĺ	đ	ı	ő	š	ü	¿	@
5	%		5		E	U	e		u		Ä	đ	í	ö	Ş	ű	·	←
6	&		6		F	V	f		v		Æ	É	î	ő	š	ů	^	½
7	'		7		G	W	g		w		á	È	ï	ô	ş	ù		→
8	(		8		H	X	h		x		â	Ě	ì	Ø	ß	Ý		↑
9	)		9		I	Y	i		y		à	é	Ľ	ó	Ť	ý		#
A	*		:		J	Z	j		z		å	ě	ľ	ò	ť	Ž		
B	+		;		K		k				ã	ê	ĺ	õ	Þ	ž		¼
C	,		<		L		l				ä	è	Ĺ	ö	þ	ą		
D	-		=		M		m				æ	ë	Ń	ő	Ú	Ą		¾
E	.		>		N		n				č	Ğ	ń	ô	Ů	ş		÷
F	/		?		O		o				Ç	ğ	ń	ø	Ü	°		

Table 8. Character ROM contents as viewed by the display MV1815-3.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes. like the control columns 0 and 1 listed in table 4.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
☐ Characters in these positions are displayed according to the setting of LS(0-3) bits, see table 7. When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

ELECTRICAL CHARACTERISTICS

T_{amb}= 0°C to +70°C, V_{CC}=+5V to ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Voltage	21 & 40	4.5	5.0	5.5	V	XTI=27.75MHz All outputs open
Supply Current	21 & 40		25		mA	circuit
	21 & 40		15		mA	XTI=0Hz All outputs open circuit
Video Input, VSI	19 & 29					
Voltage Amplitude		0.8		3.0	Vpp	Bottom of Sync to White (pk–pk)
Source Impedance				250	Ω	
TCR Input	22					
External Resistance		5	10	200	kΩ	Connected to V_{DD}
BLC and WLC	17 & 18					
Capacitor Value			10		nF	Connected to GND
Capacitor Tolerance		–10		+10		
Effective Series Resistance				5	Ω	1MHz
Sync I/O	14					100K (nom) pull up resistor
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input Current Low		–22	–50	–220	µA	V_{IN}=V_{SS}
Input Current High		–30		+30	µA	V_{IN}=V_{DD}
Data I/O	15					No pull–up resistor
Output voltage High		2.4	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input Voltage High		V_{DD}–1.0		V_{DD}	V	
Input current	–30		+30		µA	V_{IN}=V_{DD} or V_{SS}
EXT/$\overline{INT}$ (Note 1)	16					100kΩ (nom) pull–down resistor
Input current Low		–10		+10	µA	V_{IN}=V_{SS}
Input current High		22	50	220	µA	V_{IN}=V_{DD}
$\overline{XTI}$ (Note 1)	3					1M (nom) resistor to XTO
Input current Low		–5.0	–5.0	–20	µA	–0.3 <V_{IN} <V_{IL} max
Input current High		0.5	5.0	20	µA	V_{IH} min <V_{IN} <(V_{DD}+0.3)
XTO output	2					See note 2
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Frequency			27.750		MHz	±100ppm

Notes.

1. Input voltage low and input voltage high for these are as specified for Data I/O
2. When $\overline{RESET}$ is held low, A9 (pin 4) will output $F_{OSC}/2$. If required, adjust capacitor on XTO for a frequency of 13.875MHz.

ELECTRICAL CHARACTERISTICS (continued)

T_{amb}= 0°C to +70°C, V_{CC}=+5V to ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
ON HOUR INDICATOR ONH	27					
Output voltage V_{OH}		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage V_{OL}			0.2	0.4	V	I_{OL}=2.4mA
I²C bus SCL, SDA I/Ps	37, 38					100kΩ (nom) pull–up resistor
Input voltage Low		0		1.5	V	
Input voltage High		3.5		V_{DD}	V	
Output voltage Low		0	0.1	0.40	V	I_{OL}=3mA
SCL clock frequency	37		100	1000	kHz	
RED, GREEN, BLUE	24, 25, 26					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–12.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=24.0mA
Tri–state output leakage current		–60		60	µA	V_{OH}=V_{SS} or V_{DD}
EVENT	39					100kΩ (nom) pull–up resistor
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
BLANK	23					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–12.0mA
Output Voltage Low			0.2	0.4	V	I_{OL}=24.0mA
CSO	28					With typical load of 360Ω
Output voltage swing			0.5		Vpp	Text mode only, see note 3
Output voltage High		V_{DD}–0.5			V	Load of 4.3kΩ to V_{DD}
Output voltage Low				V_{DD}+0.5	V	
TEST/EVEN	30					100kΩ (nom) pull–down resistor
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input current Low		–30		+30	µA	V_{IN}=V_{SS}
Input current High		22	50	220	µA	V_{IN}=V_{DD}

Note 3.

CSO output voltage when in picture or mix mode will depend on size of Video signal applied to VSI pin 29, together with attenuation due to internal transmission switch (60Ω nom) and external load on pin 28. In these states the video signal at pin 29 is switched straight through to pin 28.

ELECTRICAL CHARACTERISTICS

T_{amb}= 0°C to +70°C, V_{CC}= +5V to ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
MEMORY INTERFACE						100kΩ (nom) pull–up resistor
DATA D0,D1	11,10					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input current Low		–22	–50	–220	µA	V_{IN}=V_{SS}
Input current High		–30		+30	µA	V_{IN}=V_{DD}
ADDRESS A0–A9 **$\overline{RAS}$, $\overline{CAS}$, $\overline{WR}$**	See Fig. 1					
Output voltage High		V_{DD}–1.0	4.5		V	I_{OH}=–1.2mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.4mA
$\overline{RESET}$ (Schmitt input)	13					100kΩ (nom) pull–up resistor
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}–1.0		V_{DD}	V	
Input current Low		–22	–50	–220	µA	V_{IN}=V_{SS}
Input current High		–10		+10	µA	V_{IN}=V_{DD}
Hysteresis voltage			0.8		V	(Rising threshold) – (falling threshold) voltages

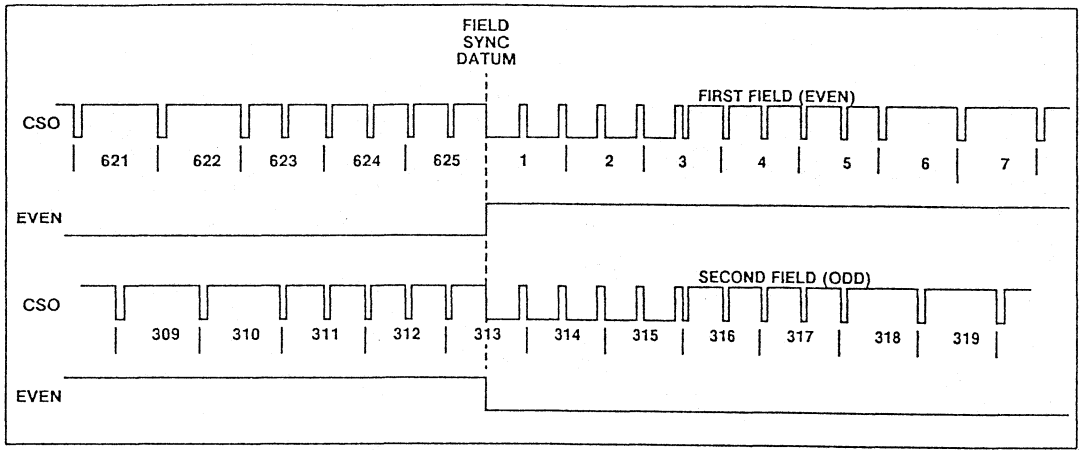


Fig.6a. Composite sync (output interlaced) and EVEN output

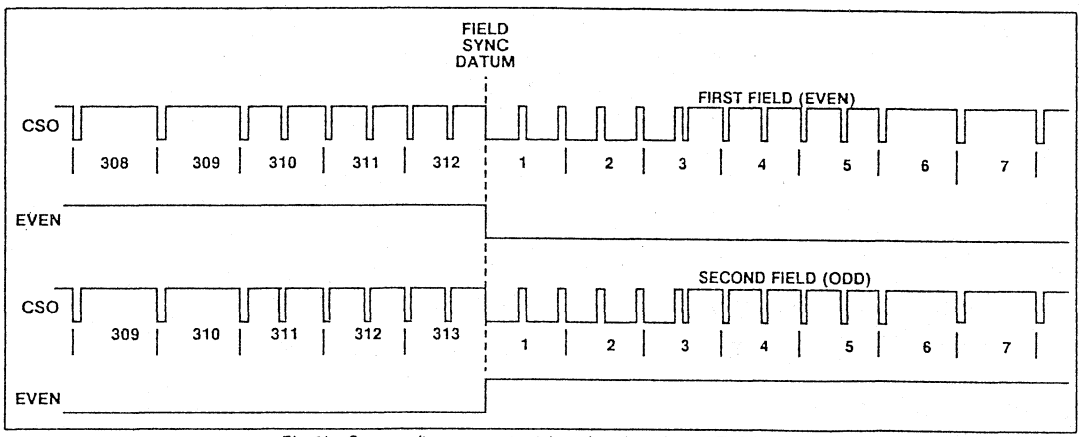


Fig.6b. Composite sync output (non-interlaced) and EVEN output

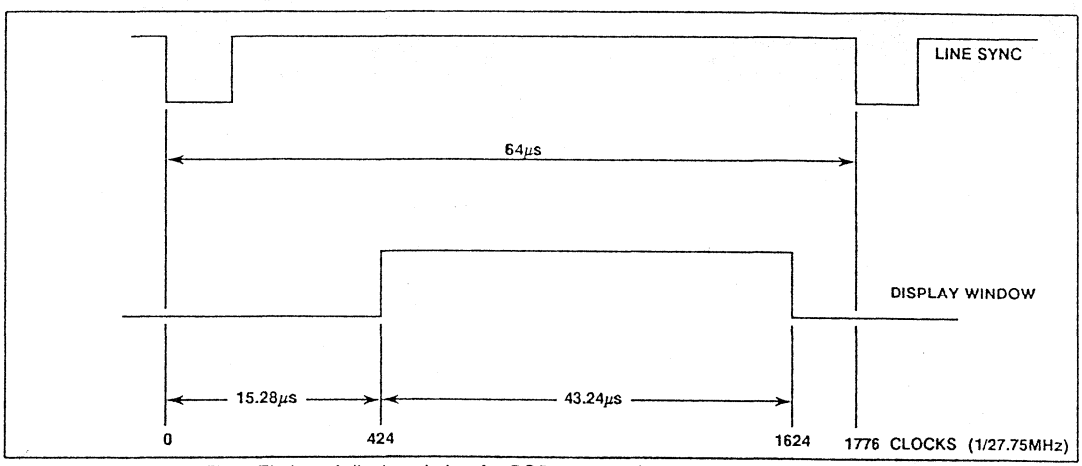


Fig.7. Timing of display window for RGB outputs related to composite sync output

MV1817

SINGLE CHIP TELETEXT DECODER FOR 625 LINE OPERATION

The MV1817 Television Data Service, TDS, IC incorporates all the features of the MV1815 with identical registers, so that MV1815 register control is software compatible. Additional TDS features are controlled by registers with addresses above those of the MV1815. A 2K/page system is included to enable extension packets to be stored with the display page data and page header data.

FEATURES

Acquisition

- Two page related data acquisition circuits
- On chip adaptive slicers for data and sync
- Accepts all data packets
- Advanced Header and Instant Page Clear working

Display

- High resolution 15x10 pixel characters
- Multi–lingual capability
- 26 display rows

Memory

- Up to 510 pages in one 4 bit organised DRAM
- 2K or 1K bytes per page

Synchronisation

- Three vertical time base modes:–
  - 312½–312½ interlaced
  - 312 – 312 non–interlaced – default
  - 312 – 313 non–interlaced
- Line (H) and field (V) sync inputs
- Full field operation
- On chip video switch

I²C bus etc.

- I²C bus interface bus to microcontroller
- I²C bus is released during power down
- Software compatible with MV1815
- Software maskable EVENT interrupts
- Register to indicate language variant

ORDERING INFORMATION

MV1817–1 CG DPAS –	West Europe version equivalent to MV1815–1 & MV1815–2
MV1817–2 CG DPAS	West + East Europe version equivalent to MV1815–3
MV1817–3 CG DPAS –	All Europe version

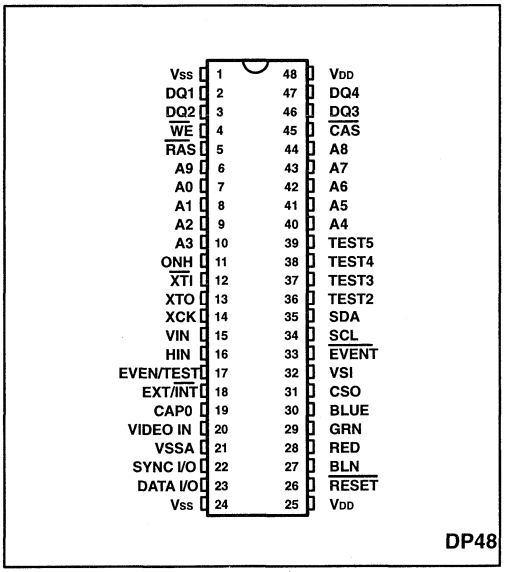


Fig. 1 Pin connections – top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	–0.3V to +7.0V
All inputs	–0.3V to V_{DD}+0.3V
Operating temperature	0°C to +70°C
Storage temperature	–65°C to 150°C

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency (preferred)	6.93750MHz. AT cut
Tolerance over operating temperature range	±50ppm
Tolerance overall	±100ppm
Nominal load capacitance	30pF
Equivalent series resistance	<20Ω

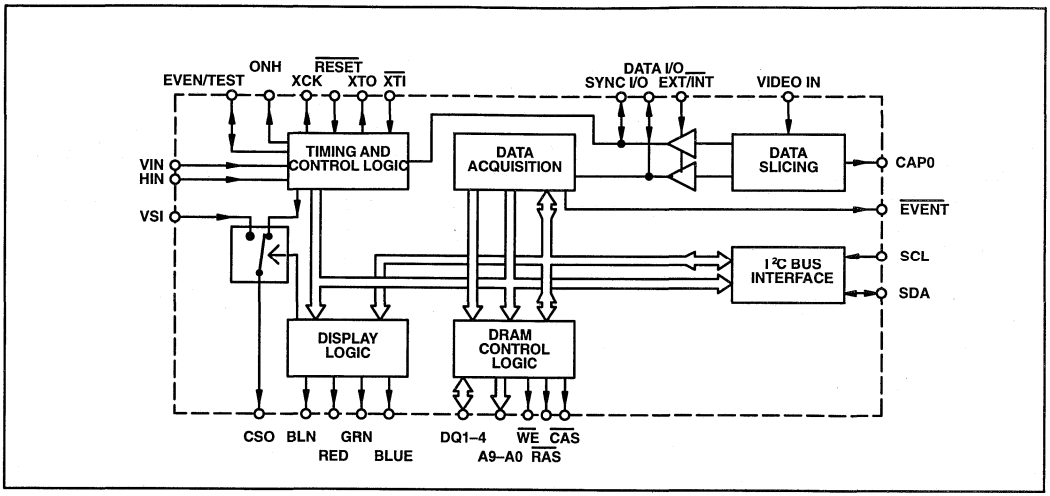


Fig. 2 Functional block diagram

ELECTRICAL CHARACTERISTICS

T_{amb}= 0°C to +70°C, V_{DD}=+5V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	25, 48	4.5	5.0	5.5	V	
Supply current	25, 48		80	140	mA	V_{DD}=5.5V White test screen
Video input, VSI	20, 32					Acquisition from TV lines 6–22 and 318–335
Voltage amplitude		0.7	1.0	2.0	V_{pp}	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	220nF input capacitor
CAP0	19					
Capacitor value			220		nF	Connected to GND
Capacitor tolerance		–10%		+10%		
Effective series resistance				5	Ω	1MHz
Sync I/O & Data I/O	22, 23					Acquisition from TV lines 2–22 and 314–335, see note 1.
Output voltage High (Data I/O only)		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA Sync I/O is an open drain output.
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Input voltage Low		0		$0.2V_{DD}$	V	
Input voltage High		$0.8V_{DD}$		V_{DD}	V	
Input current Low		–10		+10	µA	V_{IN}=V_{SS} or V_{DD}
EXT/INT	18					75k (nom) pull–down resistor
Input voltage Low		0		$0.2V_{DD}$	V	
Input voltage High		$0.8V_{DD}$		V_{DD}	V	
Input current Low		–10		+10	µA	V_{IN}=V_{SS}
Input current High		18	67	275	µA	V_{IN}=V_{DD}

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= 0°C to +70°C, V_{DD}=+5V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
XTI input	12					1M (nom) resistor to XTO
Input voltage Low		0		$0.2V_{DD}$	V	
Input voltage High		$0.8V_{DD}$		V_{DD}	V	
Input current Low		–0.5	–5.0	–20	µA	$-0.3 < V_{IN} < V_{IL}$ max
Input current High		0.5	1.5	20	µA	V_{IH} min$< V_{IN} <(V_{DD}+0.3)$
XTO output	13					
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–0.1mA
Output voltage Low			0.2	0.4	V	I_{OL}=0.1mA
Frequency			6.9375		MHz	±100ppm
I²C bus SCL, SDA Schmitt inputs	34, 35					
Input voltage Low		0		1.5	V	
Input voltage High		3.0		V_{DD}	V	
Output voltage Low			0.1	0.6	V	I_{OL}=6.0mA
SCL Clock Frequency			750	775	kHz	
Hysteresis voltage		0.2	0.4		V	
EVENT	33					75k (nom) pull–up resistor
Output voltage Low			0.2	0.4	V	I_{OL}=6.0mA open drain
RESET, VIN, HIN Schmitt inputs	26, 15 16					75k (nom) pull–up resistor
Threshold voltage falling		1.4	1.9			
Threshold voltage rising			3.1	3.8	V	
Hysteresis voltage		0.6	1.2		V	
Input current Low		–18	–67	–275	µA	$V_{IN}=V_{SS}$
Input current High		–10		+10	µA	$V_{IN}=V_{DD}$
VIN pulse width		32			µs	
HIN pulse width		1			µs	at 90% level
VIN rise time				18	µs	10% to 90% level
HIN rise time				6	µs	10% to 90% level
ONH, XCK	11, 14					See note 2
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Red, Green, Blue	28, 29					
Output voltage High	30	$0.9V_{DD}$	$0.95V_{DD}$		V	I_{OH}=–8mA
Output voltage Low			0.2	0.4	V	I_{OL}=8mA
Tri–state leakage current		–10		10	µA	
Blank	27					
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–12mA
Output voltage Low			0.2	0.4	V	I_{OL}=12mA

ELECTRICAL CHARACTERISTICS (cont.)

T_{amb}= 0°C to +70°C, V_{DD}=+5V ±10%. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
CSO	31					With typical ac load of 360Ω
Output voltage swing		0.1		1.5	V_{PP}	Text mode only. See note 3
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–0.2mA with CSOT bit =1
Output voltage Low			0.2	0.4	V	I_{OL}=1.6mA with CSOT bit =1
Even output/Test input (Schmitt)	17					75k (nom) pull–down resistor
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Threshold voltage falling		1.4	1.9			
Threshold voltage rising			3.1	3.8	V	
Hysteresis voltage		0.6	1.2		V	
Input current Low		–10		–10	µA	V_{IN}=V_{SS}
Input current High		18	67	275	µA	V_{IN}=V_{DD}
Data DQ1 – DQ4	2, 3					75k (nom) pull–up resistor
Output voltage High	46, 47	$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}=–2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA
Input voltage Low		0		0.8	V	
Input voltage High		2.0		V_{DD}	V	
Input current Low		–18	–67	–275	µA	V_{IN}=V_{SS}
Input current High		–10		+10	µA	V_{IN}=V_{DD}
Address A0 – A9	4 – 10					See note 4
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	40 – 45					
Output voltage High		$0.8V_{DD}$	$0.9V_{DD}$		V	I_{OH}= –2.0mA
Output voltage Low			0.2	0.4	V	I_{OL}=2.0mA

NOTE1. Acquisition window is wider when sliced data is supplied to DATA I/O to accommodate satellite transmissions.
NOTE 2 XCK output will be 6.9375MHz with XCKH=0 in register TADD, or 13.875Mhz with XCKH=1.
NOTE 3. CSO output voltage when in Picture or Mix modes will depend on the size of the video signal applied to VSI pin 32, together with the attenuation due to the internal video switch (30Ω nom) and the external load on pin 31. In these modes the video signal at pin 32 is switched straight through to pin 31. The maximum current allowed through the video switch is 24 mA.
NOTE 4. Capacitive loading on $\overline{RAS}$ and $\overline{CAS}$ should not exceed 20pF per pin.

Output voltage high specification ensures the output will also drive TTL levels of V_{DD}–2.1V at the specified current.

Pin N0	Name	Pin Description
1, 24	V_{SS}	Power ground 0V, both pins must be connected.
2, 3, 46, 47	DQ1–4	DRAM data lines, with internal 75k pull–up resistors.
4	$\overline{WE}$	DRAM write enable.
5	$\overline{RAS}$	DRAM row address strobe.
6–10, 40–44	A9, A0–8	DRAM address outputs.
11	ONH	On hours output.
12	$\overline{XTI}$	Crystal input or external clock input.
13	XTO	Crystal output.
14	XCK	Divided output of VCO clock, default 6.9375MHz. If XCKH bit in TADD register is set high, the output is 13.875MHz.
15	VIN	Vertical sync input positive pulse, with internal 75k pull–up. If bit VINV in MODE register is set high, the signal may be a negative pulse.
16	HIN	Horizontal sync input positive pulse, with internal 75k pull–up. If bit HINV in MODE register is set high, the signal may be a negative pulse.
17	EVEN/TEST	Even output is enabled by bits IOE and EOE in SYNCSW register. If EVEN output is not used it should be left open circuit. TEST input is used for factory testing. An internal 75k pull–down resistor is included.
18	EXT/$\overline{INT}$	Control pin for SYNC I/O and DATA I/O, with internal 75k pull–down. When high, supply sliced sync and data.
19	CAP0	Black level reference capacitor.
20	VIDEO IN	PAL composite signal with negative syncs.
21	VSSA	Analog ground.
22	SYNC I/O	Sliced sync input/output, (open drain output).
23	DATA I/O	Sliced data input/output, (push–pull output).
25, 48	V_{DD}	Power, +4.5V to +5.5V, both pins must be connected.
26	$\overline{RESET}$	Active low reset input, with 75k pull up–resistor.
27	BLN	Blanking output, high power push–pull driver.
28	RED	Red output, high power push–pull tri–state driver.
29	GRN	Green output, high power push–pull tri–state driver.
30	BLUE	Blue output, high power push–pull tri–state driver.
31	CSO	Composite sync output generated in text modes. In picture modes, connected to VSI through <30Ω video switch, see Fig. 6.
32	VSI	Composite video switch input.
33	$\overline{EVENT}$	Active low open drain output interrupt to microcontroller, with internal 75k pull–up.
34	SCL	Standard I^2C bus serial clock input.
35	SDA	Standard I^2C bus serial data input/output. Address is 0010 001R/$\overline{W}$ (22hex).
36	TEST2	For factory test only, do not connect.
37	TEST3	For factory test only, do not connect.
38	TEST4	For factory test only, do not connect.
39	TEST5	for factory test only, do not connect.
45	$\overline{CAS}$	DRAM column address strobe.

PINS	TEST	TEST LEVELS	NOTES
SDA &SCL	Human body model	1kV on 100pK through 1k5Ω	<15% LTPD
SDA & SCL	Machine model	100V on 200pF through 0Ω & <500nH	
All others	Human body model	2kV on 100pF through 1k5Ω	Meets Mil Std. 883D class 2 requirements
All others	Machine model	200V on 200pF through 0Ω & <500nH	

LTPD=Lot Tolerant Percent Defective

ESD data

ADDRESS dec/hex	REGISTER NAME	7	6	5	4	3	2	1	0	R/W	DEFAULT hex
	RADD	A17	A16	IAI	RA4	RA3	RA2	RA1	RA0	W	00
0/0	ACONA	ACQ	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
1/1	STORA	STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	W	02
2/2	PGS1A	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
3/3	PGS2A	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	20
4/4	PGS3A	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	00
5/5	ACONB	$\overline{\text{HLD}}$	MGC	PBC	PAC	SDC	SCC	SBC	SAC	W	F0
6/6	STORB	STB7	STB6	STB5	STB4	STB3	STB2	STB1	STB0	W	03
7/7	PGS1B	SCS3	SCS2	SCS1	SCS0	SAS3	SAS2	SAS1	SAS0	W	00
8/8	PGS2B	MS2	MS1	MS0	SDS1	SDS0	SBS2	SBS1	SBS0	W	00
9/9	PGS3B	PBS3	PBS2	PBS1	PBS0	PAS3	PAS2	PAS1	PAS0	W	88
10/A	RECON	WI0	WI24	WI25	PINB	PINA	FF	CDB	CDA	W	00
11/B	DISCON1	INV	RLH	DSB	CLS	CUR	BLC	LS3	UDI	W	00
12/C	DISCON2	LS0	LS1	LS2	MGS	IHD	SPH	BX1	BX0	W	00
13/D	DISCON3	TXT	MIX	INT	REV	UDK	SPOS	ST2	ST1	W	00
14/E	DISCON4	BXP	BXH	BXT	BXS	DHT	DHB	SG2	SG1	W	00
15/F	HADD	A15	A14	A13	A12	A11	A10	A9	A8	W	00
16/10	LADD	A7	A6	A5	A4	A3	A2	A1	A0	W	00
17/11	WDATA	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	W	00
19/13	SCROLL	WI29	MV	CRL	SRA4	SRA3	SRA2	SRA1	SRA0	W	00
20/14	SYNCSW	ESS	–	BXSDEL	CSOT	IOE	EOE	SEN	SVS	W	00
21/15	MODE	MD3	MD2	MD1	312:313	VHLD	HVEN	HINV	VINV	W	24
22/16	TADD	–	A18	RESET	XCKH	2K/ST	DISC	ADEC	DST8	W	00
23/17	DISPST	DSTI7	DST6	DST5	DST4	DST3	DST2	DST1	DST0	W	00
24/18	DPOS	V3	V2	V1	V0	H3	H2	H1	H0	W	7B
25/19	ENABLE	NPR	VHR	830	X/24A	X/28	X/27	X/26	X/24B	W	EE
26/1A	ACCENT	APA	APB	C8APIA	C8APIB	SCAPIA	SCAPIB	–	AHEN	W	00
0/0	EVENTA	NPR	VHR	830A	X/24	X/28	X/27	X/26	C8	R	–
1/1	EVENTB	NPR	VHR	830B	X/24	X/28	X/27	X/26	C8	R	–
2/2	CBITSA	C14	C13	C12	C11	C10	C7	C6	C5	R	–
3/3	PGR1A	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
4/4	PGR2A	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
5/5	PGR3A	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
6/6	CBITSB	C14	C13	C12	C11	C10	C7	C6	C5	R	–
7/7	PGR1B	SCR3	SCR2	SCR1	SCR0	SAR3	SAR2	SAR1	SAR0	R	–
8/8	PGR2B	MR2	MR1	MR0	SDR1	SDR0	SBR2	SBR1	SBR0	R	–
9/9	PGR3B	PBR3	PBR2	PBR1	PBR0	PAR3	PAR2	PAR1	PAR0	R	–
10/A	HAMMC	HC7	HC6	HC5	HC4	HC3	HC2	HC1	HC0	R	FF
17/11	RDATA	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	R	–
18/12	EXTEND	APIIA	APIIB	RSIND	–	CLSI	ONH	C9B	C9A	R	–
31/1F	STATUS	SL2	SL1	SL0	SR4	SR3	SR2	SR1	SR0	R	–

Table 1. Register details

WRITE REGISTERS

RADD

A17–16	Memory address
IAI	Inhibit auto increment
RA5–0	Register address

ACON A/B

ACQ	Acquisition on
MGC	Magazine compare
PBC	Page tens compare
PAC	Page units compare
SDC	Sub–code compare digit D
SCC	Sub–code compare digit C
SBC	Sub–code compare digit B
SAC	Sub–code compare digit A
$\overline{\text{HLD}}$	Hold display

PGS 1,2,3 A/B

SAS3–0	Sub–code digit A (LSD) select
SBS2–0	Sub–code digit B select
SCS3–0	Sub–code digit C select
SDS1–0	Sub–code digit D (MSD) select
PAS3–0	Page (units) select
PBS3–0	Page (tens) select
MS2–0	Magazine select

RECON

WI0	Write inhibit packet 0
WI24	Write inhibit packet 24
WI25	Write inhibit packet 25
PINB	Parity check inhibit Acquisition B
PINA	Parity check inhibit Acquisition A
FF	Full Field mode
CDB	Clear store disable Acquisition B
CDA	Clear store disable Acquisition A

DISCON1

INV	Invert display colours
RLH	Roll headers
DSB	Display acquisition circuit B (A if zero)
CLS	Clear current display store
CUR	Cursor enable
BLC	Block cursor
LS3	Language group select
UDI	Display update indicator

DISCON2

LS2–0	Language select
MGS	Magazine serial
IHD	Inhibit display rows 1–25
SPH	Suppress header
BX1–0	Boxing control bits

DISCON3

TXT	Text/ not picture
MIX	Mix text and picture
INT	Text interlace sync mode
REV	Reveal hidden text
UDK	Update key – inhibit rows 0–25
SPOS	Status line 2 position, top if set high
ST2	Display status line 2
ST1	Display status line 1

DISCON4

BXP	Box page number
BXH	Box header
BXT	Box time
BXS	Box status rows
DHT	Double height top
DHB	Double height bottom
SG2–1	Separated graphics control bits

HADD & LADD

A15–0	Memory address

WDATA

WD7–0	Write data byte to memory

SCROLL

WI29	Write inhibit packet 29
MV	Majority vote on framing code
CRL	Cursor lock
SRA4–0	Scroll value 0–23 only

SYNCSW

ESS	External sync source
BXSDEL	Box status delay by one character
CSOT	CSO TTL signal
IOE	Interlace output enable
EOE	Even output enable
SEN	Select enable SVS
SVS	Select VSI input as sync source

MODE

MD3	H sync mode 3
MD2	H sync mode 2
MD1	H sync mode 1
312:313	Non–interlace 312:313 mode
VHLD	Vertical sync half line delay (Fig. 8)
HVEN	H and V inputs enable
HINV	H invert
VINV	V invert

TADD

A18	Memory address
RESET	Reset to default state
XCKH	XCK output 13.875MHz or 6.9375MHz when low
2K/ST	2K/store mode
DISC	Disconnect display from acquisition
ADEC	Automatic memory decrement
DST8	Store number for display bit 8

DISPST

DST7–0	Store number for display bits 7–0

DPOS

V3–0	Vertical position in 2 line steps
H3–0	Horizontal position in 4 pixel steps

ENABLE

NPR	Enable NPR flag in read regs
VHR	Enable VHR flag in read regs
830	Enable 830 flag in read regs
X/24A	Enable X/24A flag in read regs
X/28	Enable X/28 flag in read regs
X/27	Enable X/27 flag in read regs
X/26	Enable X/26 flag in read regs
X/24B	Enable X/24B flag in read regs

ACCENT

APA–B	Accent protection A/B
C8APIA–B	C8 accent protection inhibit A/B
SCAPIA–B	Sub–code accent protection inhibit A/B
AHEN	Advanced headers enable

READ REGISTER

EVENT A/B

NPR	New page received flag
VHR	Valid header received flag
830A	Packet 8/30 format 1 received flag
830B	Packet 8/30 format 2 received flag
X/24	Packet X/24 received flag
X/28	Packet X/28 received flag
X/27	Packet X/27 received flag
X/26	Packet X/26 received flag
C8	Update indicator

PGR 1,2,3 A/B

SAR3–0	Sub–code digit A (LSD) received
SBR2–0	Sub–code digit B received
SCR3–0	Sub–code digit C received
SDR1–0	Sub–code digit D (MSD) received
PAR3–0	Page (units) received
PBR3–0	Page (tens) received
MR2–0	Magazine received

RDATA

RD7–0	Read data byte from memory

CBITS A/B

C14–12	Language select bits (C14 is LSB)
C11	Magazine serial
C10	Inhibit display
C7	Suppress header
C6	Sub–title
C5	News flash

HAMMC

HC7–0	Hamming counter

EXTEND

APII A/B	Accent protection inhibit indication A/B
RSIND	Reset indication
CLSI	Clear screen indicator
ONH	On hours flag
C9 A/B	Interrupted sequence bit Acq A/B

STATUS

SL2–0	Status language indication
SR4–0	Status revision indication
SL2–0=001	West Europe version=MV1815–1 & –2
SL2–0=002	West + East Europe version=MV1815–3
SL2–0=003	All Europe version

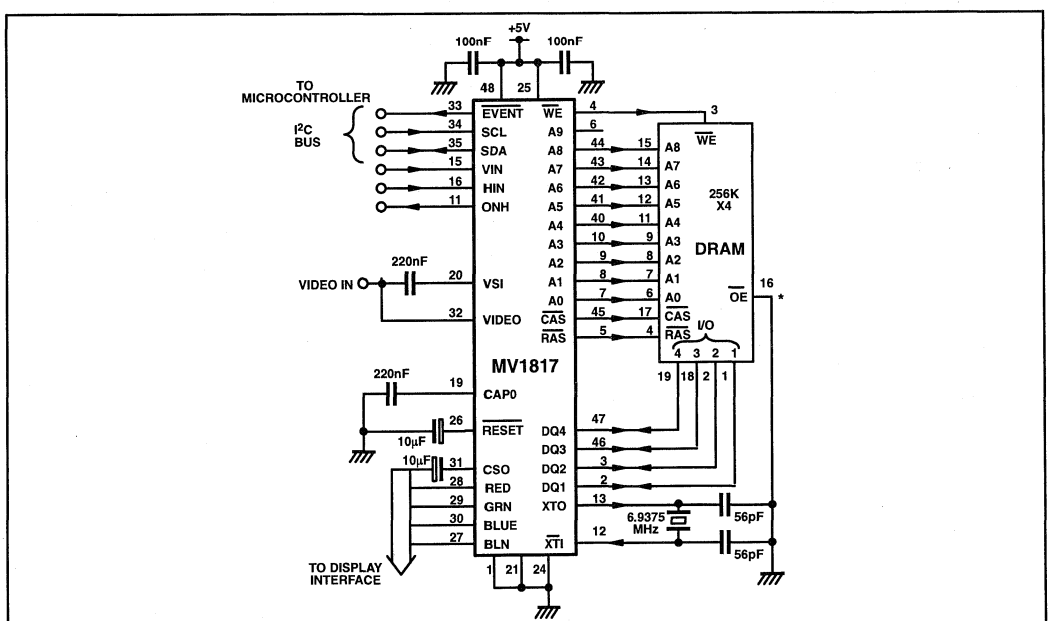


Fig. 3 Typical application diagram

* Note, on some DRAM devices $\overline{OE}$ should not be low during a write cycle. An inverted $\overline{WE}$ can be connected to $\overline{OE}$ in such cases.

I²C bus Interface – SCL and SDA.
Control of the MV1817 registers is through this interface. The I²C bus address is 0010 001 R/$\overline{W}$

The circuit works as a slave transmitter with bit eight set high or as a slave receiver with bit eight set low. In receive mode, the first data byte is written to RADD register, where the least significant five bits form the sub–address. The most significant three bits of RADD are data bits, see Table 1.

Automatic incrementing of the registers allows successive data bytes to be written to, or read from the registers. The automatic incrementing can be disabled by setting IAI bit five of RADD to one. Automatic increment can be changed to automatic decrement (for DRAM address NOT registers) by setting ADEC bit high in TADD register. All DRAM addresses may be accessed via the I²C bus interface.

When WDATA or RDATA registers are reached, the automatic incrementing accesses successive bytes of data in the DRAM starting from the current value of HADD and LADD. Automatic incrementing of registers will operate above WDATA from SCROLL register onwards.

MEMORY MAPS

The DRAM memory as viewed from the I^2C bus is organised in 1024 (400hex) byte blocks, referred to as a store. Stores 0 and 1 in 1K/store mode are reserved for the non–display packets from acquisition A and B respectively. Stores A0 and B0 in 2K/store mode are reserved for the packets X/29 and 8/30 from acquisition A and B respectively.

The table below shows the start addresses for each store. The store numbers relate to the values in the STORA, STORB and DISPST registers.

1K/store	Start addresses hex TADD, RADD, HADD, LADD	2K/store
STORE 0	0 0 00 00	STORE A0
STORE 1	0 0 04 00	STORE B0
STORE 2	0 0 08 00	STORE 1 DISPLAY
STORE 3	0 0 0C 00	STORE 1 EXT PKTS
STORE 4	0 0 10 00	STORE 2 DISPLAY
STORE 5	0 0 14 00	STORE 2 EXT PKTS
STORE 6	0 0 18 00	STORE 3 DISPLAY
STORE 7	0 0 1C 00	STORE 3 EXT PKTS
	etc. until	
STORE 508	1 3 F0 00	STORE 254 DISPLAY
STORE 509	1 3 F4 00	STORE 254 EXT PKTS
STORE 510	1 3 F8 00	STORE 255 DISPLAY
STORE 511	1 3 FC 00	STORE 255 EXT PKTS

Table 2 Memory organisation

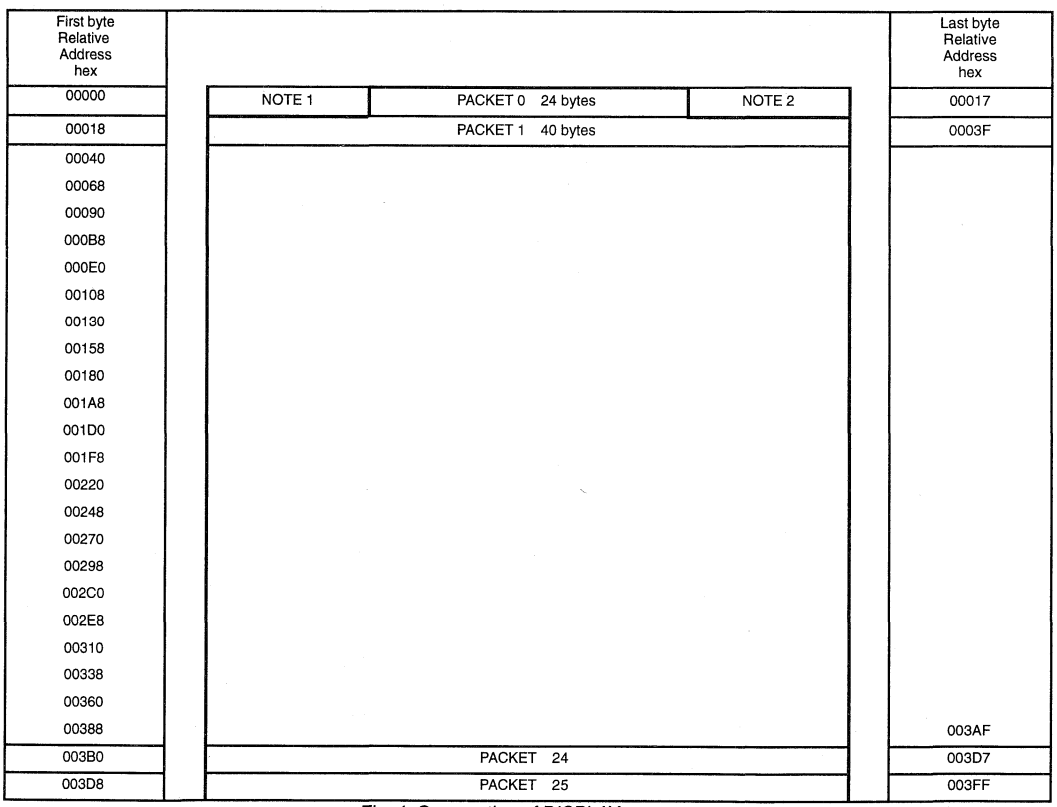


Fig. 4. Organsation of DISPLAY memory

Note 1. Page number, 8 bytes from store 0 (A0) with absolute addresses 000 to 007

Note 2. Time display, 8 bytes from store 0 (A0) with absolute addresses 008 to 00F

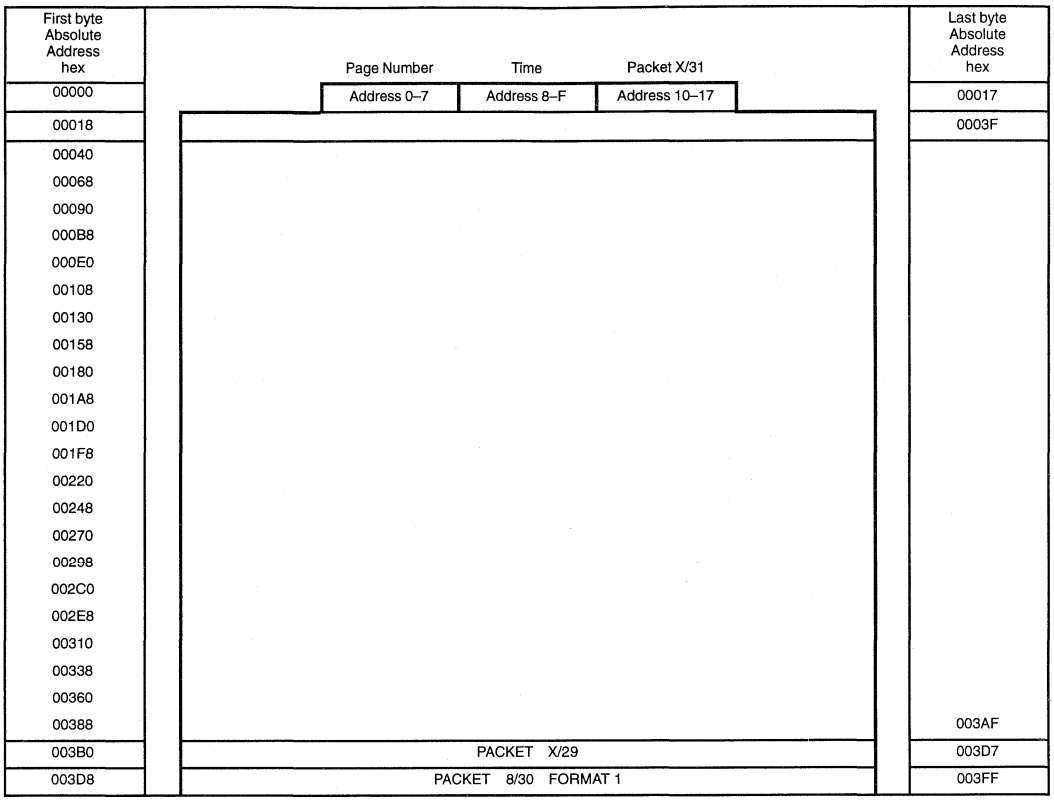


Fig. 5. Store 0 (A0) Memory organisation.

NOTE: Store 1 (B0) is organised similarly except that, in 1K/store mode it accepts acquisition circuit B packets X/26 etc. and packet 8/30 format 2 in the last row. To obtain addresses for store 1 (B0) add 400hex. Bytes 400 to 417hex are not used in store 1 (B0).

In 2K/store mode, all page related extension packets, X/26, X/27 and X/28, are directed to the store adjacent to the display store, see Table 2. Up to 23 of these packets are stored in the order received with no fixed location in the memory. The first four bytes with relative address 000 to 003 contain a copy of the related acquisition circuit data in CBITS and PGR1–3 registers in the same order. Bytes 004 to 017_{hex} are not used by the MV1817. The last two rows will not be used by the MV1817 since X/29 and 8/30 packets only go to stores A0 and B0 (or to stores 0 and 1 in 1K/store mode).

Synchronisation

In the usual configuration where a video signal is applied to the data and sync slicer, a composite sync output (CSO) is generated from the sliced video input. CSO can be modified by register bits to provide 312:312, 312:313 or 312.5:312.5 text syncs, or switch through the video switch input signal direct. If video syncs are selected with SEN=1 and SVS=1 (in SYNCSW register), the action of the 312:313 bit (in MODE register) is inhibited.

When the vertical synchronisation circuit finds a field sync datum, (see Fig. 6) it is disabled for 64 lines so that double field synchronisation is avoided.

If the display is to be synchronised to horizontal and vertical signals via the HIN and VIN pins, the HVEN enable bit in the MODE register must be set high. This will disable the action of interlace (INT) bit in DISCON3 register and also 312:313 bit in MODE register. HIN and VIN signals are normally positive pulses, but inverted signals may be applied provided that the appropriate HINV and VINV bits are set high in the MODE register. The leading edge of VIN pulse is sampled at –4.7µs and +27.3µs with respect to HIN pulse to establish which is the EVEN or ODD field, see Fig. 7. The VIN pulse should be at least 32µs minimum and the HIN pulse 1µs minimum.

If required, the vertical pulse may be delayed by half a line period by setting VHLD bit high in MODE register, see Fig. 8.

LS(3210)	0000	0001	0010	0011	0100	0101	0110	0111
TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH	ENGLISH
2/3	£	#	#	£	é	ç	#	£
2/4	$	$	¤	$	ï	$	ů	$
4/0	@	§	É	é	à	¡	č	@
5/B	←	Ä	Ä	°	ë	á	ť	←
5/C	½	Ö	Ö	ç	ê	é	ž	½
5/D	→	Ü	Å	→	ù	í	ý	→
5/E	↑	^	Ü	↑	î	ó	í	↑
5/F	#	_	_	#	#	ú	ř	#
6/0	±	°	é	ù	è	¿	é	±
7/B	¼	ä	ä	à	â	ü	á	¼
7/C	‖	ö	ö	ò	ô	ñ	ě	‖
7/D	¾	ü	å	è	û	è	ú	¾
7/E	÷	ß	ü	ì	ç	à	š	÷

LS(3210)	1000	1001	1010	1011	1100	1101	1110	1111
TABLE POSITION	POLISH	ROMANIAN	HUNGARIAN	TURKISH	DANISH	SERBO CROAT	ASCII	SOUTH AFRICAN
2/3	#	#	#	₺	£	#	#	£
2/4	ń	¤	ú	ğ	$	$	$	$
4/0	ą	Ţ	É	İ	@	Č	@	ŉ
5/B	Ź	Â	í	Ş	Æ	Ć	[	ë
5/C	ś	Ş	Ö	Ö	ø	Ž	\	ê
5/D	Ł	Ă	Á	Ç	Å	Đ	]	ü
5/E	ć	Î	ü	Ü	↑	Š	^	é
5/F	ó	ı	ő	ğ	#	ë	_	ï
6/0	ę	ţ	é	ı	±	č	'	š
7/B	ż	â	ó	ş	æ	ć	{	ä
7/C	ś	ş	ö	ö	ø	ž	‖	ô
7/D	ł	ă	á	ç	å	đ	}	û
7/E	ź	î	ü	ü	÷	š	~	ö

Table 3. Western European national optional variations - equivalent to MV1815-2. Language version 001.

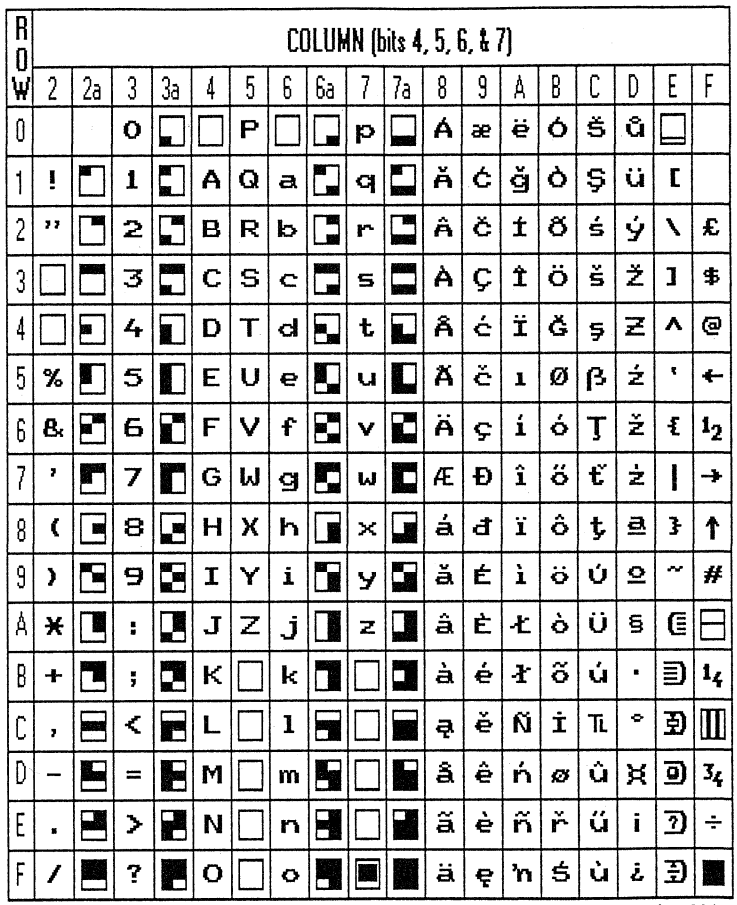


Table 4. Character ROM contents as viewed by the display. Language version 001.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes, like the control columns 0 and 1 listed in table 10.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
☐ Characters in these positions are displayed according to the setting of LS(0-3) bits, see table 3.
When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

Some language options require accented characters which are not present in the above ROM table, which is identical to that in the MV1815-2 for software compatibility.

Page closure.

In serial mode, any header will close a page being received.
In parallel mode, only a header from the selected magazine will close a page being received.

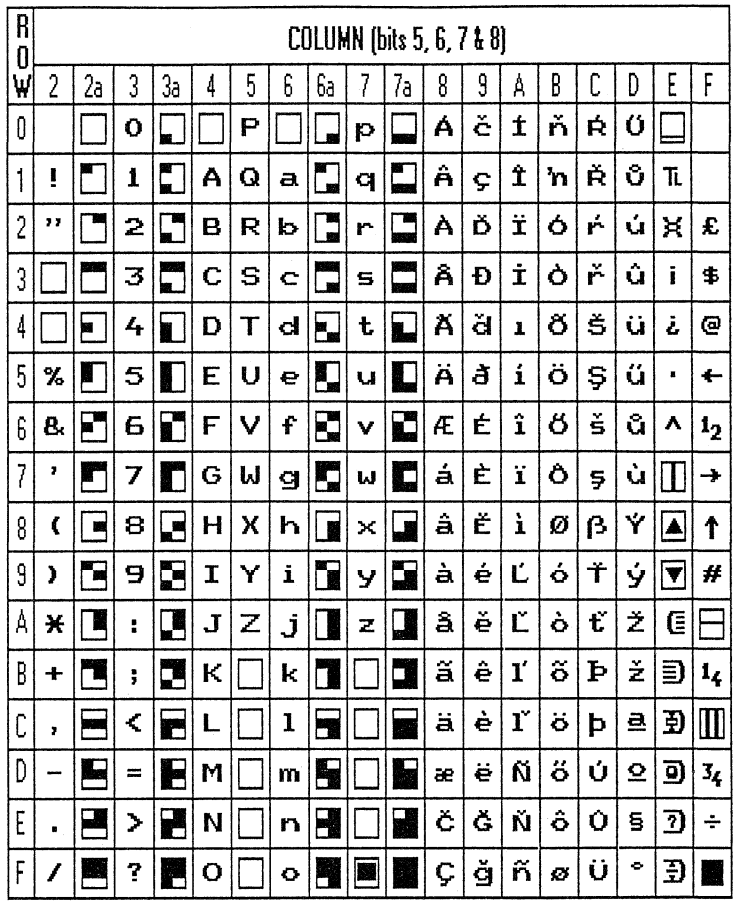
Advanced Header and Instant Page Clear transmission systems.

With these systems, the main page header packet is transmitted in the same VBI, before the associated data packets, without the standard 20ms page clearing interval. The MV1817 can be programmed to protect those associated data packets, in the same VBI, from erasure when the page is cleared. This feature is enabled for both systems by setting AHEN bit high in ACCENT register.

LS(3210)	0000	0001	0010	0011	0100	0101	0110	0111
TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH	ENGLISH
2/3	£	#	#	£	é	ç	#	£
2/4	$	$	¤	$	ï	$	ů	$
4/0	@	§	É	é	à	¡	č	@
5/B	←	Ä	Ä	°	ë	á	ť	←
5/C	½	Ö	Ö	ç	ê	é	ž	½
5/D	→	Ü	Å	→	ù	í	ý	→
5/E	↑	^	Ü	↑	î	ó	ˇ	↑
5/F	#	_	_	#	#	ú	ř	#
6/0	■	°	é	ù	è	¿	é	■
7/B	¼	ä	ä	à	â	ü	á	¼
7/C	▮	ö	ö	ò	ô	ñ	ě	▮
7/D	¾	ü	å	è	û	è	ú	¾
7/E	÷	ß	ü	ì	ç	à	š	÷

LS(3210)	1000	1001	1010	1011	1100	1101	1110	1111
TABLE POSITION	ENGLISH	GERMAN	HUNGARY	TURKISH	DANISH	SPANISH	CZECH	SOUTH AFRICAN
2/3	£	#	#	₺	£	ç	#	£
2/4	$	$	ú	ğ	$	$	ů	$
4/0	@	§	É	İ	@	¡	č	ŉ
5/B	←	Ä	í	Ş	Æ	á	ť	ë
5/C	½	Ö	Ö	Ö	Ø	é	ž	ê
5/D	→	Ü	Á	Ç	Å	í	ý	ü
5/E	↑	^	ű	Ü	↑	ó	ˇ	é
5/F	#	_	ő	ğ	#	ú	ř	ï
6/0	■	°	é	ı	■	¿	é	š
7/B	¼	ä	ó	ş	æ	ü	á	ä
7/C	▮	ö	ö	ö	ø	ñ	ě	ô
7/D	¾	ü	á	ç	å	è	ú	û
7/E	÷	ß	ü	ü	÷	à	š	ö

Table 5. National Optional Characters equivalent to MV1815-3. Language version 002.



ROW	COLUMN (bits 5, 6, 7 & 8)																	
	2	2a	3	3a	4	5	6	6a	7	7a	8	9	A	B	C	D	E	F
0			0			P			p		Á	č	ŧ	ň	Ŕ	Ú		
1	!		1		A	Q	a		q		Â	ç	Ţ	ń	ŕ	Ô	₸	
2	"		2		B	R	b		r		À	Ď	ï	ó	ŕ	ú	¤	£
3			3		C	S	c		s		Ã	Đ	ţ	ò	ř	û	¡	$
4			4		D	T	d		t		Ä	đ	ı	ő	š	ü	¿	@
5	%		5		E	U	e		u		Ä	ð	í	ö	Ş	ű	·	←
6	&		6		F	V	f		v		Æ	É	î	ő	š	ů	^	½
7	'		7		G	W	g		w		á	È	ï	Ô	ş	ù		→
8	(		8		H	X	h		x		â	Ě	ì	Ø	β	Ý		↑
9	)		9		I	Y	i		y		à	é	Ľ	ó	Ť	ý		#
A	*		:		J	Z	j		z		å	ë	Ľ	ò	ť	ž		
B	+		;		K		k				ã	ê	Ĺ	ő	Þ	ž		¼
C	,		<		L		l				ä	è	Ĺ	ö	þ	ą		
D	-		=		M		m				æ	ë	Ń	ő	Ú	ǫ		¾
E	.		>		N		n				č	ğ	Ń	ô	Ó	ş		÷
F	/		?		O		o				Ç	ğ	ń	ø	Ü	°		

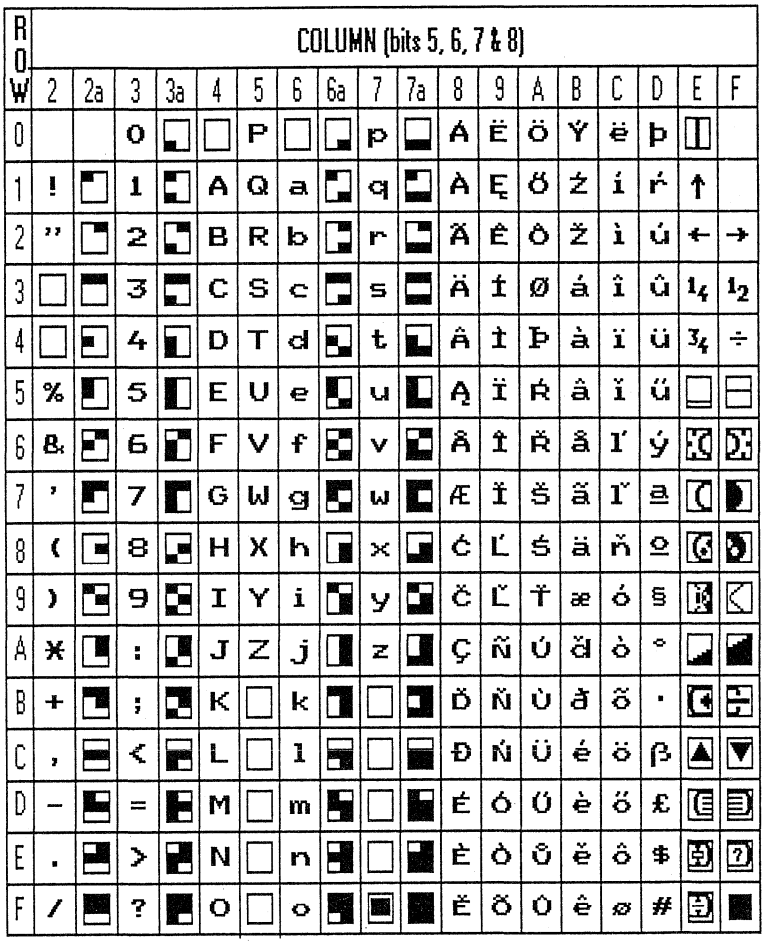
Table 6. Character ROM contents as viewed by the display. Language version 002.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes, like the control columns 0 and 1 listed in table 10.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
☐ Characters in these positions are displayed according to the setting of LS(0-3) bits, see table 5.
When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

LS(3210)	0000	0001	0010	0011	0100	0101	0110	0111
TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH	ROMANIAN
2/3	£	#	#	£	é	ç	#	#
2/4	$	$	¤	$	ï	$	ů	$
4/0	@	§	É	é	à	¡	č	Ţ
5/B	←	Ä	Ä	°	ë	á	ť	Â
5/C	½	Ö	Ö	ç	ê	é	ž	Ş
5/D	→	Ü	Å	→	ù	í	ý	Ă
5/E	↑	^	Ü	↑	î	ó	í	Î
5/F	#	_	_	#	#	ú	ř	ı
6/0	■	°	é	ù	è	¿	é	ţ
7/B	¼	ä	ä	à	â	ü	á	â
7/C	‖	ö	ö	ò	ô	ń	ě	ş
7/D	¾	ü	å	è	û	è	ú	ă
7/E	÷	ß	ü	ì	ç	à	š	î

LS(3210)	1000	1001	1010	1011	1100	1101	1110	1111
TABLE POSITION	POLISH	GERMAN	HUNGARIAN	TURKISH	DANISH	SERBO CROAT	CZECH	SOUTH AFRICAN
2/3	#	#	#	₺	£	#	#	£
2/4	ń	$	ú	ğ	$	$	ů	$
4/0	ą	§	É	İ	@	Č	č	ŉ
5/B	Ƶ	Ä	í	Ş	Æ	Ć	ť	ë
5/C	ś	Ö	Ö	ö	Ø	Ž	ž	ê
5/D	Ł	Ü	Á	Ç	Å	Đ	ý	ü
5/E	ć	^	ű	Ü	↑	Š	í	é
5/F	ó	_	ő	ğ	#	ë	ř	ï
6/0	ę	°	é	ı	■	č	é	š
7/B	ż	ä	ó	ş	æ	ć	á	ä
7/C	ś	ö	ö	ö	ø	ž	ě	ô
7/D	ł	ü	á	ç	å	đ	ú	û
7/E	ź	ß	ü	ü	÷	š	š	ö

Table 7.National Optional Characters. Language version 003 .



ROW	COLUMN (bits 5, 6, 7 & 8)																	
	2	2a	3	3a	4	5	6	6a	7	7a	8	9	A	B	C	D	E	F
0			0			P			p		Á	Ë	ö	Ý	ë	þ		
1	!		1		A	Q	a		q		À	Ę	ő	ź	í	ŕ	↑	
2	"		2		B	R	b		r		Ă	Ê	ô	ž	ì	ú	←	→
3			3		C	S	c		s		Ä	ĺ	ø	á	î	û	¼	½
4			4		D	T	d		t		Â	ł	Þ	à	ï	ü	¾	÷
5	%		5		E	U	e		u		Ą	Ï	Ŕ	â	ǐ	ű		
6	&		6		F	V	f		v		Å	ţ	Ř	å	ľ	ý		
7	'		7		G	W	g		w		Æ	ť	š	ă	ľ	ą		
8	(		8		H	X	h		x		ć	Ľ	ś	ä	ń	°		
9	)		9		I	Y	i		y		č	Ľ	ŧ	æ	ó	§		
A	*		:		J	Z	j		z		Ç	Ń	Ú	ď	ò	°		
B	+		;		K		k				Ď	Ń	Ù	đ	ő	·		
C	,		<		L		l				Đ	Ń	Ü	é	ö	ß		
D	-		=		M		m				É	Ó	Ű	è	ő	£		
E	.		>		N		n				È	Ò	Ů	ě	ô	$		
F	/		?		O		o				Ë	Ő	Ó	ê	ø	#		

Table 8. Character ROM as viewed by the display. Language version 003.

Notes: Character positions F0 and F1 will be displayed as spaces, but are actually spacing control codes, like the control columns 0 and 1 listed in table 10.
F0 is UNDERLINE start / stop code.
F1 is INVERT display colours start / stop code.
FF is displayed as all foreground.
☐ Characters in these positions are displayed according to the setting of LS(0-3) bits, see table 7.
When graphics mode is set, columns 2a, 3a, 6a & 7a are displayed as the graphic symbols shown. All other columns are displayed normally. The graphic symbols are shown above with a border which is not present when the symbol is displayed on the screen.

Graphic symbols to scale.

	INCLUDED IN MV1817- 3	NOT INCLUDED
CZECH	Ä Á Č Ď É Ě Í Ĺ Ľ Ń Ň Ö Ó Ô Ŕ Ř Š Ś Ť Ü Ú Ů Ý Ź Ž ß § ° ä ď ĺ ľ ň ö ó ô ŕ ü	
DENMARK	Æ æ Ø ø	
FRANCE	À Â Ç È É Ê Ë Ï Î Ô Û	Œ œ
HOLLAND	Ë ë	Ĳ ĳ
HUNGARY	Á Í Ó Ő Ú Ű á í ó ő ú ű	
ICELAND	Á Đ Í Ó Ö Þ Ú Ý Æ Ø ð ö þ ý æ ø	
ITALY	À È É Ì Í Ò Ù Ú í ú	
POLAND	Ą Ć Ę Ń Ó Ź $ § _	
ROMANIA	É Ě Ê Ĭ Ó é ě ê ĭ ó	
SPAIN	Á À Ã Ç É È Ï Í Ñ Ó Ò Õ Ŕ Ú Ü # · ª º → ↑ ã ä â ë ê ï î ô ò ö õ ŕ û	
TURKEY	Â Î Û â î û	

Table 5. Additional characters for the languages shown. Language version 003.

Accented characters added via X/26.

These can be automatically locked in place on the screen by the MV1817 hardware, so that further reception of the page will not change accented characters to the level one fall-back characters. Whenever a page is cleared to spaces, the locked characters will be unlocked and also become spaces. Control of this feature is by setting APA/B bits in ACCENT register. The header should be cleared by software the first time a store is used to prevent random characters in the DRAM at power up from being locked.

For pages where data is updated with C8 set, but clear page C4 is not set, the accent locking feature may be inhibited during current page reception by setting C8APIA/B bits. For rolling sub-coded pages where clear page C4 is not set, the accent locking feature may be inhibited during current page reception by setting SCAPIA/B bits. When these inhibit mechanisms are active, an indication is provided in EXTEND register by bits APIIA/B set high. They are set low when the current page is closed.

	0	1
0	Alpha Black	Graphic Black
1	Alpha Red	Graphic Red
2	Alpha Green	Graphic Green
3	Alpha Yellow	Graphic Yellow
4	Alpha Blue	Graphic Blue
5	Alpha Magenta	Graphic Magenta
6	Alpha Cyan	Graphic Cyan
7	Alpha White [1]	Graphic White
8	Flash	Conceal Display [2]
9	Steady [1] [2]	Contiguous Graphics [1] [2]
A	End Box [1] [2]	Separated Graphics [2]
B	Start Box [3]	No action
C	Normal Height [1] [2]	Black Background [1] [2]
D	Double Height	New Background [2]
E	No action	Hold Graphics
F	No action	Release Graphics [1]

Table 6. Control codes.

Notes: [1] Presumed set at the start of each display row.
[2] Action "set at the current space", others are "set after the current space".
[3] Two consecutive codes are transmitted, action takes place between them.

Sync switch register truth table

ESS	SEN	SVS	CSO output
0	0	X	VSI or digital sync selected by algorithm
0	1	0	Digital syncs
0	1	1	VSI switched through
1	X	X	Digital syncs from SYNC I/O

X=don't care.

Sync switch algorithm

The video signal will be switched through from VSI to CSO when:
TXT = 0 or MIX = 1 or TXT = 1 and BX1 = 1 and BX0 = 1.

EVEN output on TEST pin, truth table

IOE	EOE	CSO	Function
X	0	X	TEST configured as an input with an internal pull down resistor
0	1	INTERLACE	Enables EVEN output, which is held high.
1	1	INTERLACE	Enables EVEN output going high during the first field (lines 1–312½)
X	1	312:313	Enables EVEN output going high during the short field (312 lines)

X = don't care.

Note: CSO is not only dependent upon the state of the INT bit in DISCON4 register, but also on MIX and any other register bits which cause picture to be displayed, for example, UDK, BXP, BXH, BXT, BXS, or BX0–1 if start box codes are present on screen.

BOXING options and MIX mode, truth table

The bits BXP, BXH, BXT and BXS in DISCON4 register will BOX text into the picture when TXT and MIX mode are set, the BOXED text will retain its background colours. However, BOXED text using Box codes 0B in text together with BX0 or BX1 bits in DISCON2 will not override MIX and can be displayed as BOXED text by setting TXT & MIX bits low, or MIXED by setting MIX high. The BOXED STATUS ROWS can start at character position one by setting BXSDEL bit in SYNCSW register.

TXT	BX – 1.0		BX – n (n=P, H, T, S)	MIX	Status Area n	Boxed Text Areas		BASIC MODE
						Outside	Inside	
0	0.0		0	X	Picture	Picture	Picture	PICTURE
0	0.0		1	0	Boxed	Picture	Picture	
0	0.0		1	1	Mixed	Picture	Picture	
0	X.1	1.X	0	0	Picture	Picture	Text	NEWSFLASH
0	X.1	1.X	0	1	Picture	Picture	Mixed	
0	X.1	1.X	1	0	Boxed	Picture	Text	
0	X.1	1.X	1	1	Boxed	Picture	Mixed	
1	0.X	X.0	X	0	Text	Text	Text	TEXT
1	0.X	X.0	0	1	Mixed	Mixed	Mixed	
1	0.X	X.0	1	1	Boxed	Mixed	Mixed	
1	1.1		X	0	Text	Text	Picture	WINDOW
1	1.1		0	1	Mixed	Mixed	Picture	
1	1.1		1	1	Boxed	Mixed	Picture	

X = don't care.

BOX STATUS DELAY

When status rows 1 and/or 2 are enabled to be boxed into a picture or MIX text display, the first character in the row may be omitted and replaced by picture by setting the BXSDEL bit 5 in SYNCSW register high

SCROLL

A value in the range 0–23 can be used to move the text rows 1–23 up the screen, the rows 0, 24 and 25 remain fixed.

A scroll value of 3 will cause text row 4 to be displayed in row 1. Text rows 1–3, in this example will appear in rows 21, 22 and 23 respectively. If half page expand is also used, by setting DHT in DISCON3 register, the text screen can be made to scroll through the expanded top half window. The position of the text in memory, is not affected by scroll, only the row addressing is changed to effect the display.

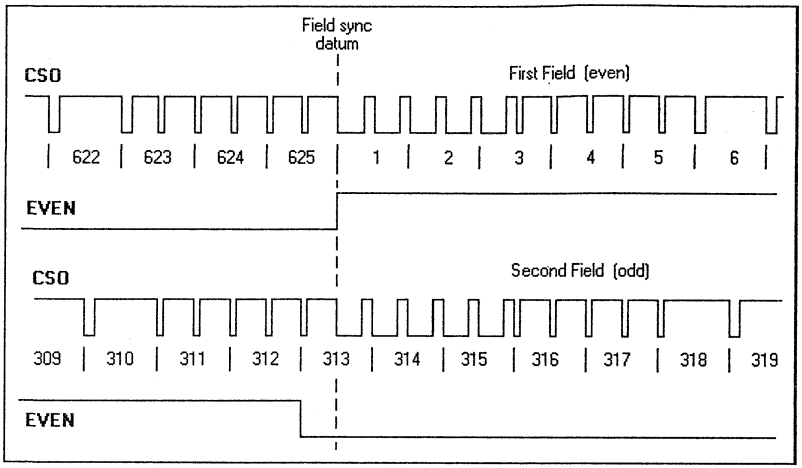


Fig. 6a. Composite sync output (interlaced) and EVEN output.

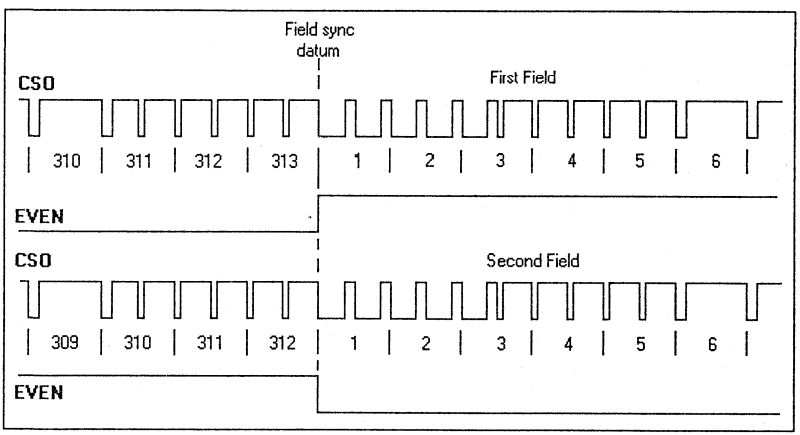


Fig. 6b. Composite sync output (non-interlaced 312:313) and EVEN output.

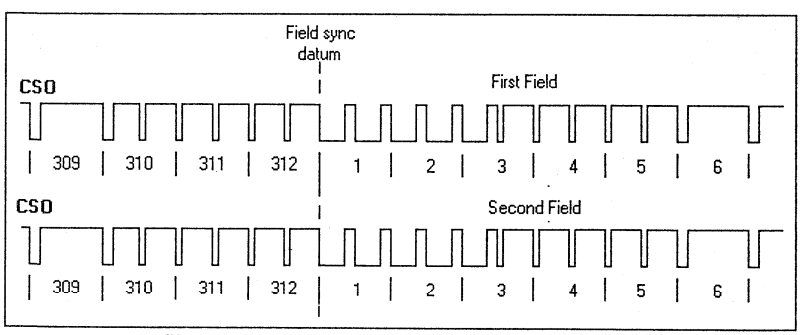


Fig. 6c. Composite sync output (non-interlaced 312:312).

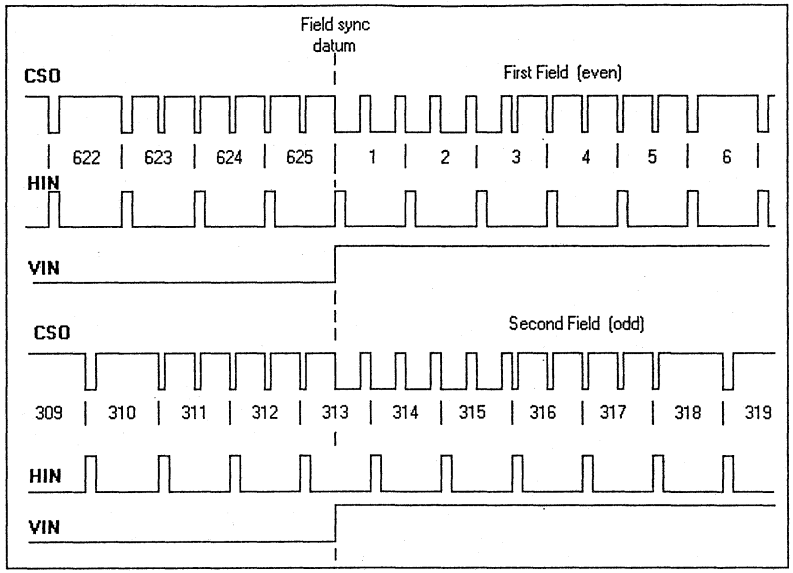


Fig. 7. Horizontal and Vertical input waveforms

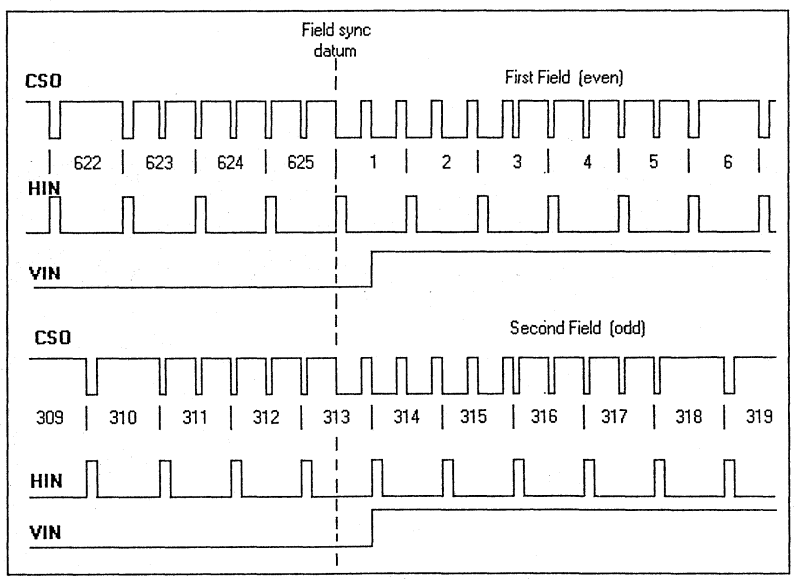


Fig. 8. Horizontal and Vertical input waveforms with Vertical Half Line Delay bit set.

Symbol	Parameter Description	Value for DRAM		Units
		Min	Max	
t_{RAC}	Access time from $\overline{RAS}$		<106	ns
t_{CAC}	Access time from $\overline{CAS}$		<43	ns
t_{CAA}	Access time from column address		<61	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge		<72	ns
t_{ASR}	Row address set-up time before $\overline{RAS}$	<27		ns
t_{RAH}	Row address hold time after $\overline{RAS}$	<45		ns
t_{RSH}	$\overline{RAS}$ hold time	<36		ns
t_{ASC}	Column address set-up time before $\overline{CAS}$	<18		ns
t_{CAH}	Column address hold time after $\overline{CAS}$	<54		ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	<72		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay	<63		ns
t_{RP}	$\overline{RAS}$ precharge time	<81		ns
t_{CP}	$\overline{CAS}$ precharge time	<27		ns
t_{CAS}	$\overline{CAS}$ low pulse width	<45		ns
t_{RAS}	$\overline{RAS}$ low pulse width	<171		ns
t_{DS}	Data set-up before $\overline{CAS}$	<18		ns
t_{DH}	Data hold time after $\overline{CAS}$	<54		ns
t_{WCS}	Write set-up before $\overline{CAS}$	<72		ns
t_{WCH}	Write hold time after $\overline{CAS}$	<72		ns
t_{PC}	Page mode cycle time	<72		ns
t_{REF} - 64K x 4	Refresh cycle time per $\overline{RAS}$ address		>1·033	ms
t_{REF} - 256K x 4	Refresh cycle time per $\overline{RAS}$ address		>2·066	ms
t_{REF} - 1M x 4	Refresh cycle time per $\overline{RAS}$ address		>4·133	ms

Table 7. Timing parameter requirements for DRAM.

NOTE: Timings are for nominal centre points on edges, so care should be taken not to load the pins.

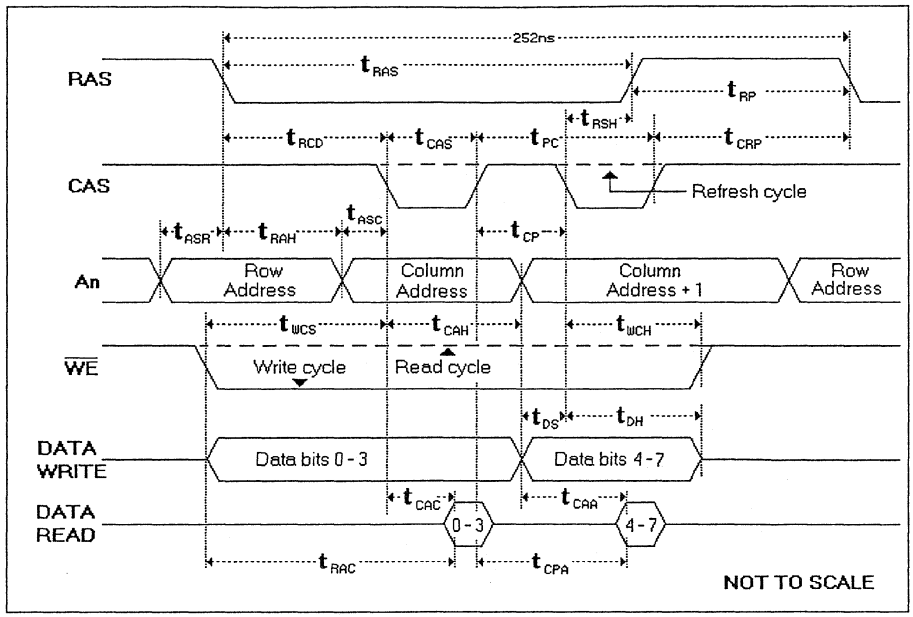


Fig. 9. DRAM interface.

DISPLAY STORE.

The MV1817 has two modes of operation defined by the setting of DISC bit in TADD register.

1. With DISC set low, the display store is tied to acquisition circuit A, if DSB bit in DISCON1 register is low, or to acquisition circuit B if DSB bit is set high. STORA or STORB defines the working store for both acquisition and display.

2. With DISC set high, the display store is disconnected from the acquisition circuits and controlled independently by the DISPST register, together with DST8 in TADD register.

The store number programmed into STORA, STORB or DISPST registers is internally adjusted to take account of 2K/STORE working, see table 2. However, the I²C bus addresses for the DRAM data are NOT internally adjusted in 2K/STORE mode, see again table 2.

DISPLAY POSITION.

This may be adjusted by changing the value in the DPOS register. The lower 4 bits control the horizontal position. The default state is Bhex and the step size is four pixels (0·288 µs). Incrementing by one moves the display right by four pixels. This means the display can be moved 16 pixels (1·153 µs) right and 44 pixels (3·171 µs) left from the default position 15·28µs from the leading negative edge of the Composite Sync Output horizontal sync pulse, see figure 10.

The upper 4 bits control the vertical position and the line numbers are referred to the Field Sync Datum on the Composite Sync Output, see Fig 6. The default state is 7hex and the step size is 2 TV lines. Incrementing by one moves the display up two TV lines. The default start position is TV line 46 for a 24 row display and TV line 36 for a 25 or 26 row display. The range of movement is 16 TV lines up and 14 TV lines down from the default starting position, see figure 11.

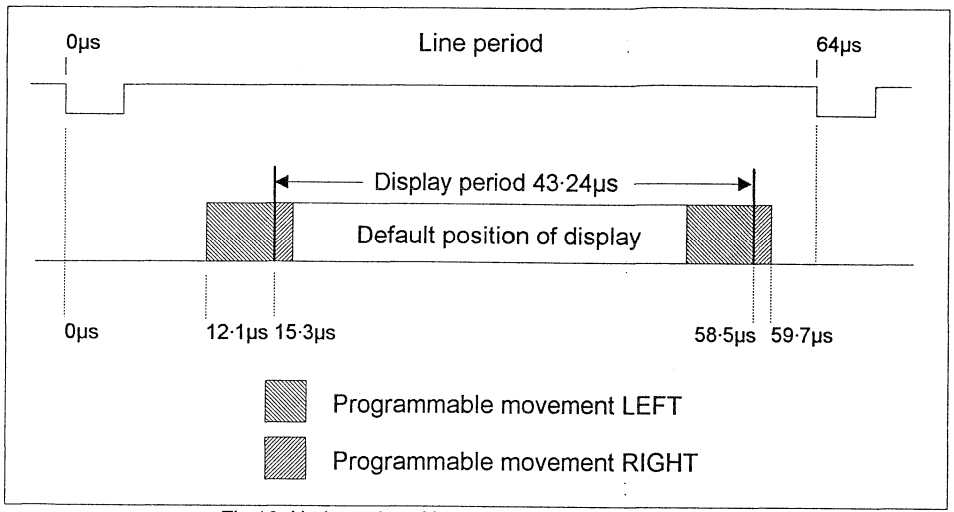


Fig.10. Horizontal position and movement of text display.

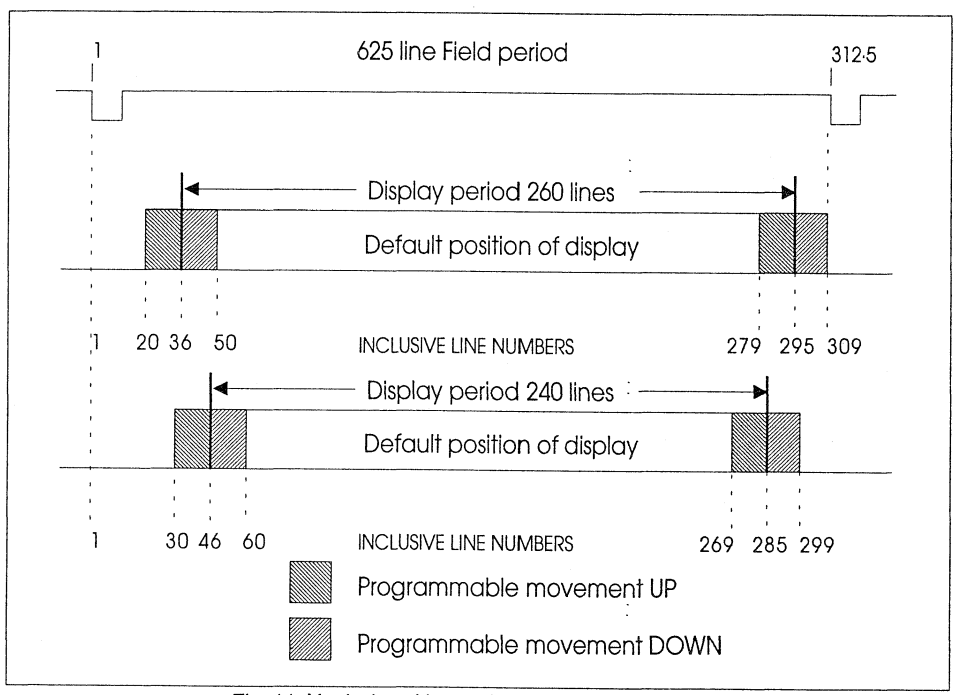


Fig. 11. Vertical position and movement of text display.

DS3106 2.4

MV1820

VIDEO PROGRAMME DELIVERY CONTROL INTERFACE CIRCUIT

The MV1820 is a high speed CMOS receiver for Programme Delivery Control (PDC) messages broadcast in World System Teletext (WST) Format Two Broadcast Service Data Packets (BSDP). The PDC message can be read on an I²C bus with a data format similar to standard Video Programming Service (VPS) decoders. Additional data is appended to include new PDC features.

It is intended for use in Video Cassette Recorders to provide automatic recording of suitably labelled Television programmes requested by the user.

FEATURES

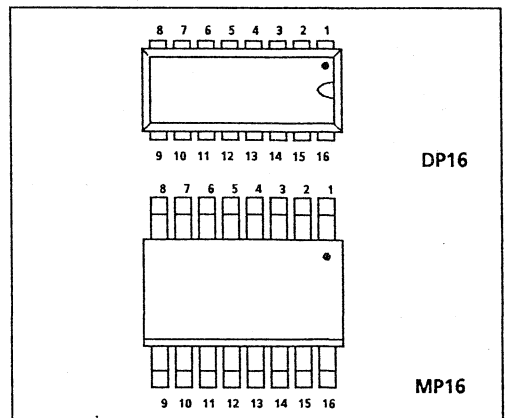
- On chip data slicing
- Low external component count
- I²C bus for low cost interfacing
- Advanced CMOS technology gives low power dissipation and high reliability

ABSOLUTE MAXIMUM RATINGS

Supply voltage	0.3V to 7V
All inputs	-0.3 to V_{DD} + 0.3V
Operating temperature	0 to +70°C
Storage temperature	-55 to 125°C

ORDERING INFORMATION

MV1820E/CG/DPAS
MV1820E/CG/MPES



PIN	DESCRIPTION	PIN	DESCRIPTION
1	RESET (bar)	16	XTI (bar)
2	EXT/INT (bar)	15	XTO
3	BLC	14	DAV (bar)
4	WLC	13	SDA
5	VIDEO	12	VDD
6	GND	11	SCL
7	TCR	10	SYNC I/O
8	AS	9	DATA I/O

Fig.1 Pin connections - top view

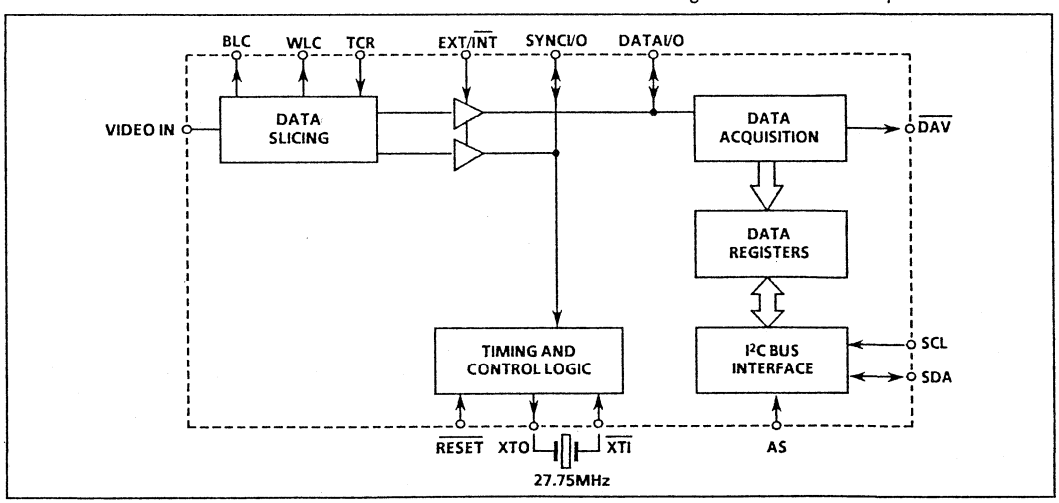


Fig.2 MV1820 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0 to 70°C, V_{DD} = 5V ± 10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply voltage	12	4.5	5.0	5.5	V	
Supply current	12		20	25	mA	
Video input	5					
Video amplitude		0.8		3.0	Vpp	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	
TCR input	7					
External resistance		4.7	4.7	200	kΩ	Connected to V_{DD}
BLC and WLC	3 & 4					
Capacitor value			10		nF	Connected to GND
Capacitor tolerance		-10%		+10%		
Effective series resistance				5	Ω	1MHz
DATA I/O and SYNC I/O	9 & 10					
Output voltage High		V_{DD}-1.0	4.5		V	I_{OH} = -1.2mA
Output voltage Low			0.2	0.4	V	I_{OL} = 2.4mA
Input voltage Low		0		0.8	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current		-30		+30	µA	V_{IN} = V_{SS} or V_{DD}
EXT/INT (bar)	2					100k (nom) pull-down resistor
Input voltage Low		0		0.8	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current Low		-10		+10	µA	V_{IN} = V_{SS}
Input current High		22	50	220	µA	V_{IN} = V_{DD}
AS	8					100k (nom) pull-down resistor
Input voltage Low		0		1.0	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current Low		-10		+10	µA	V_{IN} = V_{SS}
Input current High		22	50	220	µA	V_{IN} = V_{DD}
XTI (bar) Input	16					
Input current Low		-0.5	-5.0	-20	µA	-0.3 < V_{IN} < V_{IL} max
Input current High		0.5	5.0	20	µA	V_{IH}min < V_{IN} < (V_{DD} + 0.3)
XTO output	15					
Output voltage High		V_{DD}-1.0	4.5		V	I_{OH} = -1.0mA
Output voltage Low			0.2	0.4	V	I_{OL} = 2.0mA
Frequency			27.750		MHz	± 100ppm

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise stated)
T_{amb} = 0 to 70°C, V_{DD} = 5V ± 10%

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
I²C bus						
SCL, SDA Schmitt inputs	11, 13					Not clamped when V_{DD} = 0V
Input voltage Low		0		1.5	V	
Input voltage High		3.5		V_{DD}	V	
Output voltage Low			0.1	0.4	V	I_{OL} = 3.0mA
SCL clock frequency	11		100	1000	kHz	
DAV (bar) data available						100k (nom) pull-up resistor
Output voltage Low			0.2	0.4	V	I_{OH} = 2.4mA
RESET (bar) Schmitt input	1					100k (nom) pull-up resistor
Input voltage Low		0		0.8	V	
Input voltage High		V_{DD}-1.0		V_{DD}	V	
Input current Low		-22	-50	-220	µA	V_{IN} = V_{SS}
Input current High		-10		+10	µA	V_{IN} = V_{DD}

NOTE
Input voltage low and input voltage high for EXT/INT (bar), AS and XTI (bar) are as specified for DATA I/O

PIN DESCRIPTION Symbol	Pin No	Pin Name and Description
RESET (bar)	1	**Active Low Reset.** Includes a 100kΩ pull - up resistor.
EXT/INT (bar)	2	**Control Pin for SYNC I/O and DATA I/O.** Includes a 100kΩ pull - down resistor. When low or not connected, internal SYNC and DATA are used, pins 9 and 10 are outputs. When high, supply SYNC and DATA from an external source, pins 9 and 10 are inputs.
BLC	3	**Black level capacitor.**
WLC	4	**White level capacitor.**
VIDEO	5	**Input for composite video signal with negative going syncs**
GND	6	**Ground 0 volts.**
TCR	7	**Time constant resistor**. Controlling discharge rate of black and white level capacitor voltages.
AS	8	**Address select for I²C bus.** [0010 0001] with AS set high, or [0010 0011] with AS set low. Includes 100kΩ pull - down resistor.
DATA I/O	9	**Data input/output.**
SYNC I/O	10	**Sync input/output.**
SCL	11	**I²C bus serial clock.**
VDD	12	**Positive supply voltage +5V ±10%**
SDA	13	**I²C bus bi-directional data port.**
DAV (bar)	14	**Active low open drain output data available signal to microprocessor.** Includes 100kΩ pull - up resistor
XTO	15	**Crystal out**, 27.75MHz fundamental crystal with on-chip 1MΩ resistor to XTI (bar).
XTI (bar)	16	**Crystal input.**

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 27.750000MHz. AT cut.
Tolerance at -10°C to 60°C ± 50ppm.
Tolerance overall ±100ppm.
Nominal load capacitance 20pF.
Equivalent series resistance <20Ω.

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1820 to lock onto the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6 - 22 and 318 - 335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext data.

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and valid Broadcast Service Data Packets (BSDP) format two type only are accepted. These are known as packet 8/30. Format two is signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8,4) and stored in seven registers each of eight bits. If the complete message is correctly received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by the DAV (bar) pin going low. At the same time the data is transferred to a second bank of registers, reorganised with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to be read out on the I²C bus when so requested. Subsequent valid messages will continue to be transferred to the output registers overwriting any existing data. In this way the output registers always contain the latest PDC message.

The MV1820 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20 + 1 hex) with the address select (AS) pin set high, or 0010 0011 (22 + 1 hex) with the AS pin set low. The read bit (LSB) must always be set, it is not possible to write to the MV1820.

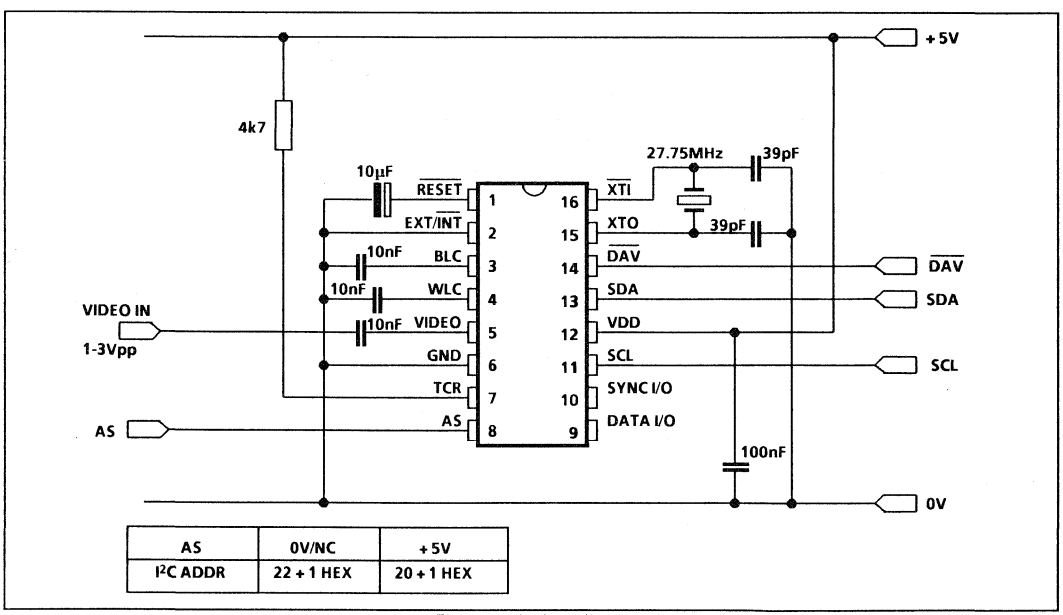
On recognising its address, the MV1820 will send an acknowledge and then transmit on the SDA line the first byte from the output registers (decoded byte 16 and 17) most significant bit (MSB) first. It will then monitor the SDA line for an acknowledge from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1820 will release the data line to allow the microprocessor to send a stop condition. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged. The final data will be byte 13 followed by the four '1's.

When readout is complete, the DAV (bar) pin is reset high and the output registers are all set high. If the microprocessor continues to send clocks on the SCL line, the MV1820 will output FF bytes on the SDA line. Also, if the MV1820 is re-addressed before another PDC message is received, the MV1820 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an Acknowledge followed by a STOP condition after any byte has been sent by the MV1820. The registers will then be reset to FF bytes and the DAV (bar) pin will be reset high.

To prevent any corruption of the data in the output registers during I²C bus activity, valid PDC messages are held in the incoming registers until I²C bus activity ceases. Here they may be overwritten by new PDC messages until the I²C bus activity ceases and they can then be transferred to the output registers.

System clock is provided by an on - chip 27.75MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset, RESET (bar) pulled low, the output I²C bus registers will contain FF bytes and the DAV (bar) pin will be set high. When the power supply is removed, the I²C bus will not be clamped to ground, leaving it free for other I²C bus traffic.



AS	0V/NC	+5V
I²C ADDR	22 + 1 HEX	20 + 1 HEX

Fig. 3 typical application diagram

ORDER OF DATA OUTPUT ON THE I²C BUS

Bit Order		EBU Numbering		Bit Value	VPS Equivalence
byte 1	bit 7	byte 16	bit 0 - CNI b9	reserved	[byte 11
	bit 6		bit 1 - CNI b10	64 network (or programme provider)	I
	bit 5		bit 2 - PIL b1	16	I
	bit 4		bit 3 - PIL b2	8	I
	bit 3	byte 17	bit 0 - PIL b3	4 day	I
	bit 2		bit 1 - PIL b4	2	I
	bit 1		bit 2 - PIL b5	1	I
	bit 0		bit 3 - PIL b6	8	[
byte 2	bit 7	byte 18	bit 0 - PIL b7	4	[byte 12
	bit 6		bit 1 - PIL b8	2 month	I
	bit 5		bit 2 - PIL b9	1	I
	bit 4		bit 3 - PIL b10	16	I
	bit 3	byte 19	bit 0 - PIL b11	8	I
	bit 2		bit 1 - PIL b12	4 hour	I
	bit 1		bit 2 - PIL b13	2	I
	bit 0		bit 3 - PIL b14	1	[
byte 3	bit 7	byte 20	bit 0 - PIL b15	32	[byte 13
	bit 6		bit 1 - PIL b16	16	I
	bit 5		bit 2 - PIL b17	8	I
	bit 4		bit 3 - PIL b18	4 minute	I
	bit 3	byte 21	bit 0 - PIL b19	2	I
	bit 2		bit 1 - PIL b20	1	I
	bit 1		bit 2 - CNI b5	8	I
	bit 0		bit 3 - CNI b6	4	[
byte 4	bit 7	byte 22	bit 0 - CNI b7	2 country	[byte 14
	bit 6		bit 1 - CNI b8	1	I
	bit 5		bit 2 - CNI b11	32	I
	bit 4		bit 3 - CNI b12	16	I
	bit 3	byte 23	bit 0 - CNI b13	8 network (or programme provider)	I
	bit 2		bit 1 - CNI b14	4	I
	bit 1		bit 2 - CNI b15	2	I
	bit 0		bit 3 - CNI b16	1	[
byte 5	bit 7	byte 14	bit 0 - PCS b1	2 status (define the analog sound	[byte 5
	bit 6		bit 1 - PCS b2	1 transmission system)	I
	bit 5		bit 2 - unallocated		I
	bit 4		bit 3 - unallocated		I
	bit 3	byte 15	bit 0 - CNI b1	128	I
	bit 2		bit 1 - CNI b2	64	I
	bit 1		bit 2 - CNI b3	32 country	I
	bit 0		bit 3 - CNI b4	16	[
byte 6	bit 7	byte 24	bit 0 - PTY b1	128	[byte 15
	bit 6		bit 1 - PTY b2	64	I
	bit 5		bit 2 - PTY b3	32	I
	bit 4		bit 3 - PTY b4	16 programme type	I
	bit 3	byte 25	bit 0 - PTY b5	8	I
	bit 2		bit 1 - PTY b6	4	I
	bit 1		bit 2 - PTY b7	2	I
	bit 0		bit 3 - PTY b8	1	[
byte 7	bit 7	byte 13	bit 0 - LCI b1	2 Label Channel Identifier	
	bit 6		bit 1 - LCI b2	1 Interleave up to four PIL messages	
	bit 5		bit 2 - LUF	1 Label Update Flag (LUF)	
	bit 4		bit 3 - unallocated		
	bit 3		-set to 1		
	bit 2		-set to 1	NOTE: Data is output on the	
	bit 1		-set to 1	I²C bus MSB first	
	bit 0		-set to 1		

MV1821

VIDEO CASSETTE RECORDER PDC AND VPS INTERFACE CIRCUIT

The MV1821 is a member of the Enhanced Video Automation (EVA) family for receiving Programme Delivery Control (PDC) messages broadcast in World System Teletext (WST) format two Broadcast Service Data Packets (BSDP). It will also receive Video Programme System (VPS) data from TV line 16 in Manchester bi–phase format. The data from either service can be read via the I²C bus connections in a standard format (see page 7). Additional data is appended to include new PDC features and differentiate between data sources.

It is intended for use in Video Cassette Recorders to provide automatic recording of suitably labelled Television programmes requested by the user.

FEATURES

- Fully automatic PDC/VPS switching
- Full error checking of both data formats
- Low external component count
- I²C Bus for low cost Interfacing
- I²C Bus and $\overline{DAV}$ released during power down
- Low frequency 6·9375MHz oscillator
- Full decoding of Hamming data (PDC)
- Supports 'fast mode' I²C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	–0·3V to +7·0V
All inputs	–0·3 to V_{DD}+0·3V
Operating temperature	–10°C to +75°C
Storage temperature	–65°C to +150°C

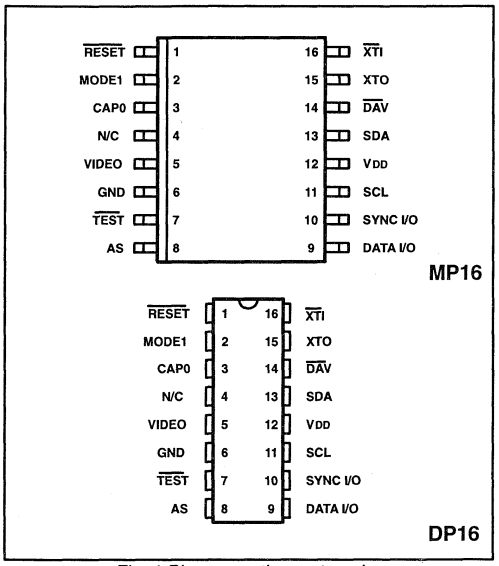


Fig. 1 Pin connections – top view

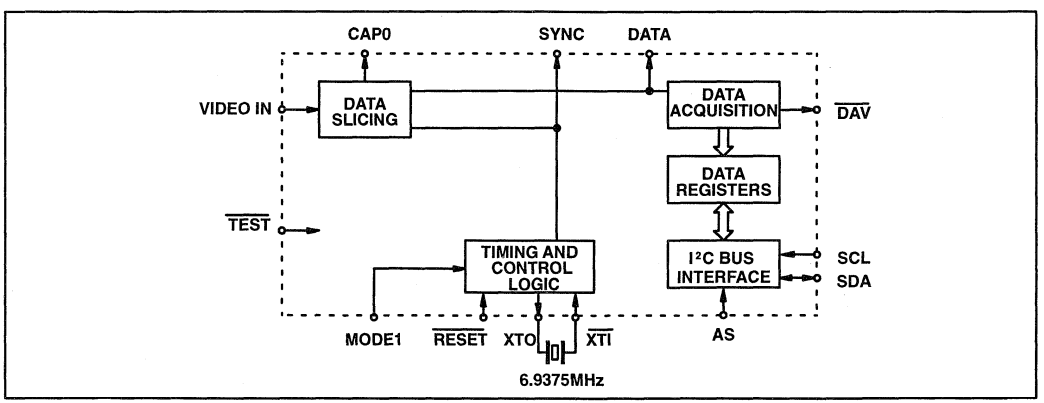


Fig. 2 MV1821 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = –10 to +75°C, V_{DD} = 5V ±10%

Characteristics	Pin	Min	Typ	Max	Units	Conditions
Supply voltage	12	4·5	5·0	5·5	V	
Supply Current	12		20		mA	
Video input	5					
Voltage amplitude		0·7	1·0	2·0	Vpp	Bottom of sync to white (pk to pk)
Source impedance				250	Ω	220nF input capacitor
CAP0	3					
Capacitor value			220		nF	Connected to GND
Capacitor tolerance		–10%		+10%		
Effective series resistance				5	Ω	1MHz
DATA & SYNC OUTPUTS	9 & 10					
Output voltage High		0·8V_{DD}	0·95V_{DD}		V	I_{OH} = –2·0mA
Output voltage Low			0·1	0·4	V	I_{OL} = 2·0mA
MODE1 & AS	2 & 8					75k (nom) pull–down resistor
Input voltage Low		0		0·2V_{DD}	V	
Input voltage High		0·8V_{DD}		V_{DD}	V	
Input current Low		–10		+10	µA	V_{IN} = V_{SS}
Input current High		18	67	275	µA	V_{IN} = V_{DD}
$\overline{\text{XTI}}$ input	16					1M (nom) resistor to XTO
Input voltage Low		0		0·2V_{DD}	V	
Input voltage High		0·8V_{DD}		V_{DD}	V	
Input current Low		–0·5	–5·0	–20	µA	–0·3 <V_{IN} <V_{IL} max
Input current High		0·5	1.5	20	µA	V_{IH} min <V_{IN} <(V_{DD} +0·3)
XTO output	15					
Output voltage High		0·8V_{DD}	0·9V_{DD}		V	I_{OH} = –0·1mA
Output voltage Low			0·1	0·4	V	I_{OL} = 0·1mA
Frequency			6·9375		MHz	±100ppm
I²C bus						
SCL, SDA Schmitt inputs	11, 13					
Input voltage Low		0		1·5	V	
Input voltage High		3·0		V_{DD}	V	
Output voltage Low (SDA only)			0·1	0·6	V	I_{OL} = 6·0mA
SCL Clock Frequency	11		400	775	kHz	
Hysteresis voltage		0·2	0·4		V	
$\overline{\text{DAV}}$ Data available	14					
Output voltage Low			0·1	0·4	V	I_{OL} = 2·0mA

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = –10 to +75°C, V_{DD} = 5V ±10%

Characteristics	Pin	Min	Typ	Max	Units	Conditions
$\overline{\text{RESET}}$ Schmitt input	1					75k (nom) pull–up resistor
Threshold voltage falling		1·4	2·0		V	
Threshold voltage rising			3·0	3·8	V	
Hysteresis Voltage		0·6	1·0		V	
Input current Low		–18	–67	–275	µA	$V_{IN} = V_{SS}$
Input current High		–10		+10	µA	$V_{IN} = V_{DD}$

Table 1

Pins	Test	Test Levels	Notes
SDA & SCL	Human body model	1kV on 100pF through 1k5Ω	< 15% LTPD
SDA & SCL	Machine model	100V on 200pF through 0Ω & <500nH	
All others	Human body model	4kV on 100pF through 1k5Ω	Meets Mil. Std. 883D class 3 requirements
All others	Machine model	400V on 200pF through 0Ω & <500nH	

LTPD=Lot Tolerant Percent Defective

Table 2 ESD data

PIN DESCRIPTION

Symbol	Pin No	Pin Name and Description
$\overline{\text{RESET}}$	1	Active low reset. Includes a 75kΩ pull–up resistor
MODE1	2	When low or not connected, both PDC and VPS data are received automatically. When high during reset positive going edge VPS ONLY mode is forced. The pin must be returned low after reset for proper operation. Includes a 75kΩ pull–down resistor. (See †)
CAP0	3	Capacitor zero. Storage for reference voltage.
N/C	4	No connection.
VIDEO	5	Input for composite video signal with negative going syncs.
GND	6	Ground 0 volts.
$\overline{\text{TEST}}$	7	Test pin, for factory use only, leave open circuit or connected to V_{DD}.
AS	8	Address select for I^2C bus, 0010 0001 if set high, or 0010 0011 if set low.
DATA	9	Data output
SYNC	10	Sync output
SCL	11	I^2C bus serial clock input
V_{DD}	12	Positive supply voltage +5V
SDA	13	I^2C bus bi–directional data port
$\overline{\text{DAV}}$	14	Active low open drain output data available signal to microprocessor
XTO	15	Crystal out, 6·9375MHz fundamental crystal with on–chip 1MΩ resistor to $\overline{\text{XTI}}$
$\overline{\text{XTI}}$	16	Crystal input

CRYSTAL SPECIFICATION

Parallel resonant fundamental frequency 6·9375000MHz. AT cut.

Tolerance at –10°C to 60°C	±50ppm
Tolerance overall	±100ppm
Nominal load capacitance	30pF
Equivalent series resistance	<20Ω

FUNCTIONAL DESCRIPTION

The video signal is sliced to produce data and synchronising signals. Timing circuits monitor the sync signal to enable the MV1821 to lock to the broadcast signal. A timing window, for the Vertical Blanking Interval (VBI) lines 6–22 and 318–335, is established to enable the acquisition circuit to monitor the sliced data signal for valid teletext or VPS line 16 data.

PDC reception

The framing code is checked for valid World System Teletext (WST) data. Magazine, packet and designation code bytes are checked and valid Broadcast Service Data Packets (BSDP) format two type only are accepted. These are also known as packet 8/30. Format two is signalled by byte six, data bit two being set high and bits 3 and 4 set low. Bytes 13 to 25 inclusive are Hamming decoded (8, 4) and stored in seven registers each of eight bits. If the complete message is received with no uncorrectable Hamming errors, an interrupt to the microprocessor is signalled by setting the $\overline{DAV}$ pin low. At the same time the data is transferred to a second bank of registers, provided there is no I²C bus activity at the time, reorganised with original numbered bytes 14, 15, 24, 25 and 13 placed after byte 23, to read out on the I²C bus when so requested. See page 7.

VPS reception

The VPS data consists of 15 eight bit words encoded in Manchester bi–phase format with a data rate of 2.5Mbits/sec. It is only transmitted in TV line 16, so similar data on other TV lines is excluded. A data low to high transition indicates a binary zero and a high to low transition indicates a binary one. Word 1 acts as a clock run (10/10/10/10/10/10/10/10) to synchronise the decoder. Word 2 is a start code (10/00/10/10/10/01/10/01) to verify the required data. Note, the second element 00 contains a deliberate violation of the Manchester bi–phase format which is only permitted in word 2. Words 5, 11, 12, 13, 14 and 15 are Manchester bi–phase decoded and if verified are stored in the input registers. When all the message is correctly received, an interrupt to the microprocessor is signalled by the $\overline{DAV}$ pin going low. At the same time the data is transferred to a second bank of registers, provided there is no I²C bus activity at the time, reorganised into the word sequence11, 12, 13, 14, 5, 15, followed by 11111110, to be read out on the I²C bus when requested, see page 7.

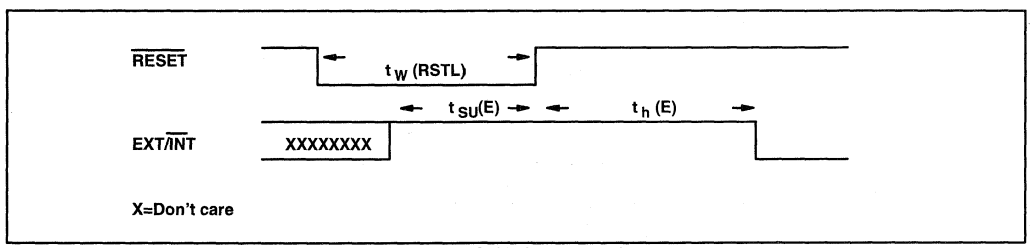


Fig. 3 VPS ONLY mode timing

PARAMETER		FROM POWER UP			FROM RESET		
		MIN	NOM	MAX	MIN	NOM	MAX
t_w(RSTL)	Pulse duration $\overline{RESET}$ low	300ms			150ns		
t_{su}(E)	EXT/$\overline{INT}$ set–up time before $\overline{RESET}$ high	150ns			150ns		
t_h(E)	EXT/$\overline{INT}$ hold time after $\overline{RESET}$ high	150ns			150ns		

† VPS ONLY mode

In an area where VPS is the only form of Programme Delivery Control then because of the algorithm employed by MV1821 when searching for the presence of either packet 8/30 format 2 or VPS in the broadcast signal, a delay of approximately 2·5 seconds would occur at power–up, reset and whenever a channel change occurred. This mode alleviates this problem in VPS only areas.

To force the MV1821 into VPS ONLY mode the following events must occur:

At power–up/reset the $\overline{RESET}$ pin must be low and the EXT/$\overline{INT}$ pin must be high, the reset pin is then taken high after which the EXT/$\overline{INT}$ pin is taken low. (see Fig. 3).

The ideal way of generating the timing shown in Fig.3 is under microcontroller or microprocessor control using output pins or some from of decoder e.g. 74HCT138.

In order to return to AUTO PDC/VPS mode it is only necessary to perform a reset with EXT/$\overline{INT}$ held low.

I²C bus interface

The MV1821 is configured as an I²C bus slave transmitter with a selectable address. The I²C bus address is 0010 0001 (20+1 hex) with the address select (AS) pin set high, or 0010 0011(22+1 hex) with the AS pin set low. The read bit (LSB) must be set, it is not possible to write to the MV1821.

On recognising its address, the MV1821 will send an acknowledge, and then transmit on the SDA line the first byte from the output registers most significant bit (MSB) first. It will then monitor the SDA line for an acknowledge from the microprocessor. If the microprocessor does NOT send an acknowledge, the MV1821 will release the data line to allow the microprocessor to send a stop condition and the output registers are all set high. If the microprocessor does send an acknowledge, the following bytes of the message will be output provided each byte is acknowledged. The final data will be either, PDC byte 13 followed by1111, or 1111110 for VPS messages, see page 7. The last bit of the message serves to indicate the source of data: 1=PDC, 0=VPS.

When readout is complete, the $\overline{DAV}$ pin is reset high and the output registers are all set high. If the microprocessor continues to send clocks on the SCL line, the MV1821 will output FF bytes on the SDA line. Also, if the MV1821 is re–addressed before another PDC message is received, the MV1821 will output FF bytes on the SDA line. The microprocessor can prematurely stop the message by NOT sending an acknowledge followed optionally by a STOP condition after any byte has been sent by the MV1821. The registers will then be reset to FF and the $\overline{DAV}$ pin will be reset high. Also, if after a partial readout, the microprocessor sends a repeat START condition followed by the MV1821 I^2C bus address, the registers will be reset to FF, $\overline{DAV}$ pin will be reset high and the MV1821 will output FF bytes on the SDA line.

To prevent any corruption of the data in the output registers during I^2C bus activity, valid PDC or VPS messages are held in the incoming registers until I^2C bus activity ceases. Here they may be over written by new PDC or VPS messages until the I^2C bus activity ceases and they can be transferred to the output registers. In the absence of I^2C bus reads, subsequent valid messages will continue to be transferred to the output registers over–writing any existing data. In this way the output registers always contain the latest PDC or VPS message.

General information

PDC data transmitted via Teletext packets 8–30 Format 2, will take precedence over VPS data. A 64 state frame counter is reset by every valid PDC packet, which will inhibit VPS reception until the counter reaches maximum. This will ensure that if receiving both signals on a given transmission, the PDC data will dominate, but if it does at any time cease to be received, the VPS data will be enabled within 2.56 seconds of the last PDC packet. This allows for one pkt. 8–30 to be missed without changing to VPS operation. See Fig. 6.

The system clock is provided by an on chip 6·9375MHz oscillator together with an external parallel resonant fundamental frequency AT cut crystal.

Following a reset ($\overline{RESET}$ pulled low), the output I^2C bus registers will contain FF bytes and the $\overline{DAV}$ pin will be set high. When the MV1821 is powered down, the I^2C bus will be released so that it can be used by other devices.

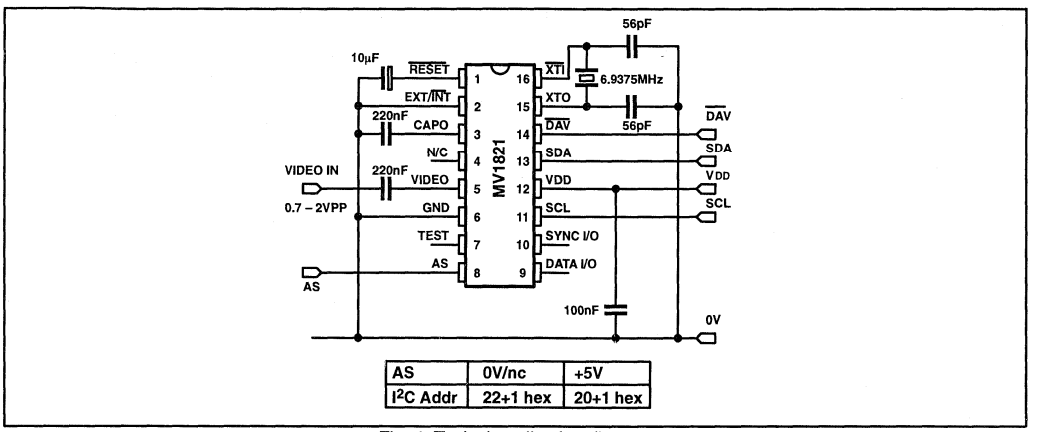


Fig. 4. Typical application diagram

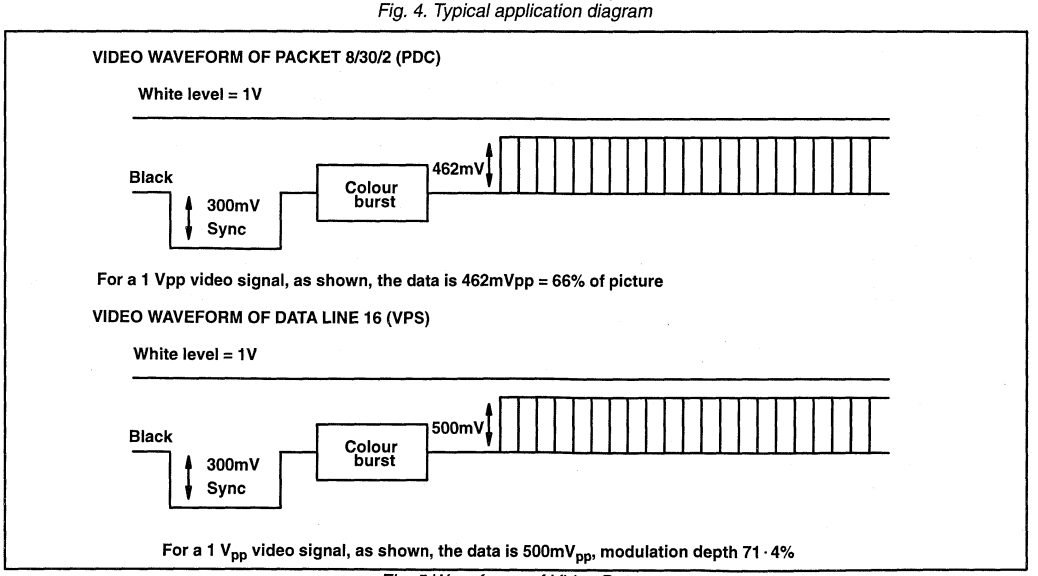


Fig. 5 Waveforms of Video Data

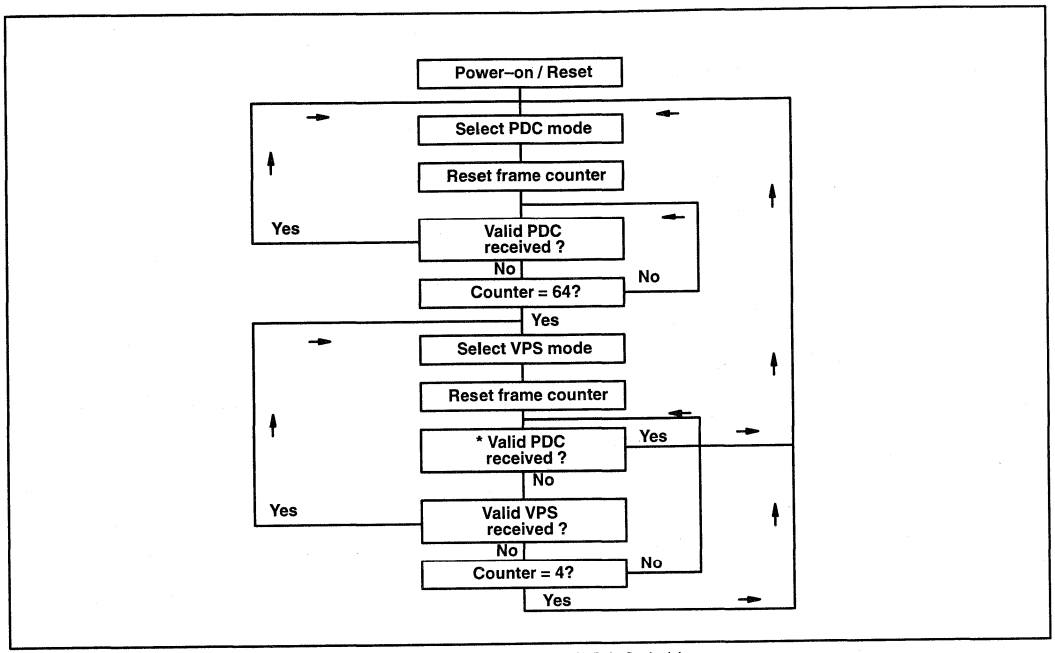


Fig. 6 Flow chart of VPS/PDC Switching

* The operation of the MV1821, in the presence of both Line 16 (VPS) and packet 8/30/2, follows the guidelines of the EBU Code of practice, SPB459 Revision2, February 1992, page 49:

"–When both Line 16 (VPS) and teletext delivered labels are available simultaneously, decoders should default to the teletext delivered service."

The counter is incremented once / frame

One line = 64µs One frame = 625 lines

PDC timeout count =	64 frames =	625 x 64µs x 64 =	2·56s
VPS timeout count =	4 frames =	625 x 64µs x 4 =	160ms

ORDERING INFORMATION

MV1821/KG/DPAS
MV1821/KG/MPES
MV1821/KG/MPEE (Tape and Reel)

ORDER OF DATA OUTPUT ON THE I²C BUS

BIT ORDER		PDC DATA		BIT VALUE		VPS data
byte 1	bit 7	byte 16	bit 0 – CNI b9	———	reserved	byte 11
	bit 6		bit 1 – CNI b10	64	Network (or programme provider)	
	bit 5		bit 2 – PIL b1	16		
	bit 4		bit 3 – PIL b2	8		
	bit 3	byte 17	bit 0 – PIL b3	4	Day	
	bit 2		bit 1 – PIL b4	2		
	bit 1		bit 2 – PIL b5	1		
	bit 0		bit 3 – PIL b6	8		
byte 2	bit 7	byte 18	bit 0 – PIL b7	4		byte 12
	bit 6		bit 1 – PIL b8	2	Month	
	bit 5		bit 2 – PIL b9	1		
	bit 4		bit 3 – PIL b10	16		
	bit 3	byte 19	bit 0 – PIL b11	8		
	bit 2		bit 1 – PIL b12	4	Hour	
	bit 1		bit 2 – PIL b13	2		
	bit 0		bit 3 – PIL b14	1		
byte 3	bit 7	byte 20	bit 0 – PIL b15	32		byte 13
	bit 6		bit 1 – PIL b16	16		
	bit 5		bit 2 – PIL b17	8		
	bit 4		bit 3 – PIL b18	4	Minute	
	bit 3	byte 21	bit 0 – PIL b19	2		
	bit 2		bit 1 – PIL b20	1		
	bit 1		bit 2 – CNI b5	8		
	bit 0		bit 3 – CNI b6	4		
byte 4	bit 7	byte 22	bit 0 – CNI b7	2	Country	byte 14
	bit 6		bit 1 – CNI b8	1		
	bit 5		bit 2 – CNI b11	32		
	bit 4		bit 3 – CNI b12	16		
	bit 3	byte 23	bit 0 – CNI b13	8	Network (or programme provider)	
	bit 2		bit 1 – CNI b14	4		
	bit 1		bit 2 – CNI b15	2		
	bit 0		bit 3 – CNI b16	1		
byte 5	bit 7	byte 14	bit 0 – PCS b1	2	Status (define the analog sound	byte 5
	bit 6		bit 1 – PCS b2	1	transmission system)	
	bit 5		bit 2 – MI	1	Mode Indicator	
	bit 4		bit 3 – unallocated			
	bit 3	byte 15	bit 0 – CNI b1	128		
	bit 2		bit 1 – CNI b2	64		
	bit 1		bit 2 – CNI b3	32	Country	
	bit 0		bit 3 – CNI b4	16		
byte 6	bit 7	byte 24	bit 0 – PTY b1	128		byte 15
	bit 6		bit 1 – PTY b2	64		
	bit 5		bit 2 – PTY b3	32		
	bit 4		bit 3 – PTY b4	16	Programme Type	
	bit 3	byte 25	bit 0 – PTY b5	8		
	bit 2		bit 1 – PTY b6	4		
	bit 1		bit 2 – PTY b7	2		
	bit 0		bit 3 – PTY b8	1		
byte 7	bit 7	byte 13	bit 0 – LC1 b1	2	Label Channel Identifier	– set to 1
	bit 6		bit 1 – LC1 b2	1	interleave up to four PIL messages	– set to 1
	bit 5		bit 2 – LUF	1	Label Update Flag	– set to 1
	bit 4		bit 3 – PRF	1	Prepare to Record Flag	– set to 1
	bit 3		– set to 1			– set to 1
	bit 2		– set to 1	NOTE: Data is output on the I²C bus MSB first		– set to 1
	bit 1		– set to 1			– set to 1
	bit 0		– set to 1			– set to 0

Section 6
Remote Control

GEC PLESSEY
SEMICONDUCTORS

SL486

INFRA RED REMOTE CONTROL PREAMPLIFIER

The SL486 is a high gain preamplifier designed to form an interface between an infra-red receiving diode and the digital input of remote control receiving circuits. The device contains two other circuit elements, one to provide a stretched output pulse facility and a voltage regulator to allow operation from a wide range of supplies.

FEATURES

- Fast Acting AGC Improves Operation In Noisy Environments
- Differential Inputs Reduce Noise Pick-up and Improve Stability
- Gyrator Circuit Allows Operation in Environments with High Brightness Background Light Levels
- Output Pulse Stretcher for use with Microprocessor Decoders
- On-chip Regulator allows Operation from Wide Range of Power Supplies
- Low Noise Output

ORDERING INFORMATION

SL486 NA DP
SL486 NA MP

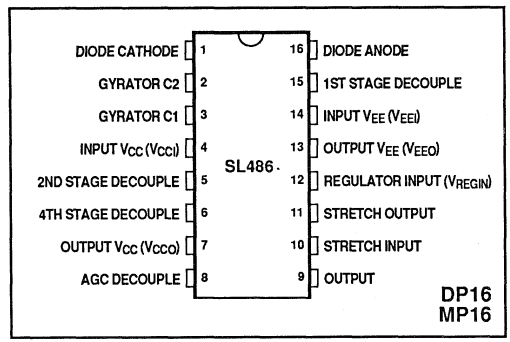


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CCI}	+10V wrt V_{EEI}
Supply voltage, V_{CCO}	+10V wrt V_{EEO}
Regulator input voltage, V_{REGIN}	−20V wrt V_{CCO}
Output current	5mA
Stretch output current	5mA
Operating temperature range	0°C to +70°C
Storage temperature	−55°C to+150°C

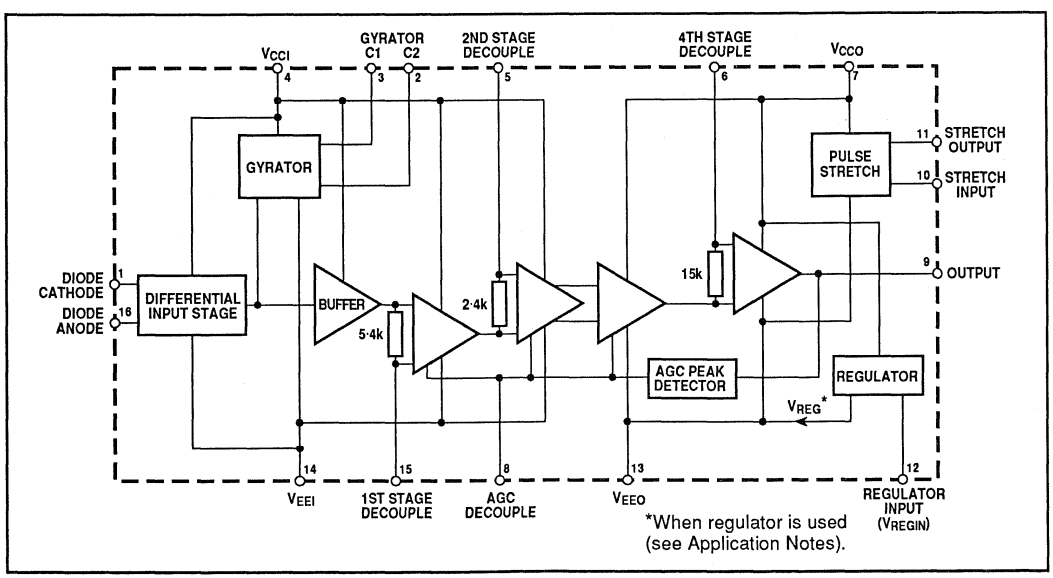


Fig. 2 SL486 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):
T_{AMB} = +25°C, $V_{CCI} = V_{CCO} = V_{CC}$ = +4·5V to +7·0V, $V_{EEI} = V_{EEO} = V_{EE}$ = 0V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current (see note 1)	4,7		6·5	9·0	mA	V_{CC} = 5·0V, I_D = 1·0μA
	4	3·5+3I_D	4·2+3I_D	5+3I_D	mA	V_{CC} = 4·5V, $I_D \leq$ 1·5mA
	4,7		8·5	10	mA	V_{CC} = 18V, I_D = 1·0μA, V_{REGIN} = 0V
Low voltage supply wrt V_{EEI} & V_{EEO}	4,7	4·5		9·5	V	
High voltage supply wrt V_{REGIN}	4,7	8·4		18	V	$V_{EEI} = V_{EEO} = V_{REG}$ (see Figs. 4 & 6)
Int. regulated voltage, V_{REG}, wrt V_{CCO}	13	5·9	6·2	6·5	V	$V_{CCO}+V_{REGIN}$ = +16V
$\lvert V_{CCI}-V_{CCO}\rvert$	4,7			1·5	V	
				1·1	V	T_{AMB} = +70°C
Minimum sensitivity of differential input	1,16	9·0		2·3	nA	I_D = 1·0μA
		74·0		18·5	nA	I_D = 100μA
		168·0		42·0	nA	I_D = 0·5mA
Common mode rejection	1,16		35		dB	
Maximum signal input	1,16	3·0	4·0		mA (pk)	
AGC range			68·0		dB	
Output and Stretch output internal pull-up resistance	9, 11		55·0		kΩ	
Stretch output pulse width, t_P	11		2·4		ms	Capacitance pin 9 to pin 10 (C8 on Figs. 4 and 8) = 10nF; $t_P \approx -R_X C_8 \log_e\left[\frac{1·5}{V_{CC}}\right]$ ms where R_X = 200kΩ ±25% and R_X = internal resistance)
Temperature coefficient of R_X			0·7		%/°C	
Output low voltage	9			V_{EEO}+0·35	V	I_{SINK} = 0·2mA max.
Output high voltage	9	V_{CCO}−0·5			V	I_{SOURCE} = 5μA
Stretch output low voltage	11			V_{EEO}+0·5	V	I_{SINK} = 1·6mA max.
Stretch output high voltage	11	V_{CCO}−0·1			V	I_{SOURCE} = 5μA, output open circuit
V_{CCI} supply rejection	4		1·5		V (pk)	Ripple amplitude at 100Hz, V_{REGIN} = 0V
			0·8		V (pk)	Ripple amplitude at 100Hz, V_{EEO} and V_{EEI} = 0V

NOTE 1. I_D = IR diode forward current

APPLICATION NOTES - REFER TO FIG. 4

Diode Anode and Cathode (Pins 1 and 16) The infra-red receiving diode is connected between pins 1 and 16. The input circuit is configured so as to reject signals common to both pins. This improves the stability of the device, and greatly reduces the sensitivity to radiated electrical noise, The diode is reverse biased by a nominal 0·65V

Gyrator C2 and C1 (Pins 2 and 3) The decoupling, provided by gyrator C2 and C1, rolls off the gain of the feedback loop which balances the DC component of the infra-red diode current. The values of C2 and C1 are chosen to produce a low frequency cut-off characteristic below a nominal 2kHz. Hence, the gyrator produces approximately 20dB rejection at 100Hz.

The gyrator consists of two feedback loops operating in tandem. Only one feedback path is functional when the DC component of the diode current is less than 200μA. This loop is decoupled by gyrator C2. For diode currents between 200μA and 1·5mA the second control loop is operative, and this is decoupled by gyrator C1.

The decoupling capacitors, gyrator C2 and C1, must be connected between pins 2 and 3, to pin 4. The series impedance of C2 and C1 should be kept to a minimum.

First Stage Decouple (Pin 15) The capacitor on pin 15 decouples the signal from the non-inverting input of the first difference amplifier (see also Fig. 2). The capacitance of 15nF is chosen to produce a 2kHz low frequency roll-off. .The capacitor must be connected between pins 15 and 14 (the input ground).

Second Stage Decouple (Pin 5) The capacitor on pin 5 decouples the signal from the non-inverting input of the second difference amplifier. The capacifance of 33nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 5 and 4 (the input V_{CC}).

Fourth Stage Decouple (Pin 6) The capacitor on pin 6 decouples the signal from the non-inverting input of the fourth difference amplifier. The capacitance of 4.7nF is chosen to produce a 2kHz low frequency roll-off. The capacitor must be connected between pins 6 and 7 (the output V_{CC}).

AGC Decouple/Delay Adjust (Pin 8) The output of the fourth difference amplifier is followed by a peak detector, which is used to provide an AGC control level. This produces a current source which is limited to 10mA at pin 8. The AGC decoupling capacitor (C5 normally 150nF) filters the pulsed input, and the resultant level controls the gain of the first three difference amplifiers.

The AGC control level exhibits a fast attack/slow decay characteristic. Immediately infra-red pulses are detected, the gain will be reduced, so that any weaker noise pulses that are also received will not be seen at the output. Thus, provided the infra-red pulses are the most intense, it is possible to receive data in noisy environments. The slow decay keeps the AGC level intact during data reception, and produces a delay before any received noise may become present at the output, when transmission ceases.

Output (Pin 9) The output will be low, pulsing high with a source impedance of a nominal 55kΩ , for a received infra-red pulse. It is a linear amplification of the input and swings between output ground and output V_{CC}.

Stretch Input and Stretch Output (Pins 10 and 11) A typical infra-red PPM system transmits very narrow pulses. The duration of these pulses is typically 15μs, so in order to use a microprocessor-based decoder system it is necessary to lengthen the received pulse. This stretched output can be obtained from pin 11 when a capacitor is connected between pins 9 and 10 (C8 in Fig. 4).

The width of the pulse is determined by the value of this coupling capacitor and is defined in the Electrical Characteristics. The stretch output is normally high, pulsing low for a received infra-red pulse and swings between V_{CCO} and V_{EEO}.

It must be noted that the stretch output logic sense is inverse to that of the output on pin 9 so must be re-inverted for microprocessor applications.

Regulator Input, V_{REGIN} (Pin 12) The device can be operated with supplies of between 4·5V and 9·0V connected between input/output ground (pins 14 and 13) and input and output V_{CC} (pins 4 and 7) as shown in Fig. 3. The device can also be operated with supplies in excess of 9·0V by using the on-chip regulator. In this case connections are made between V_{CCO} (pin 7) and the regulator input V_{REGIN}(pin 12) as shown in Fig. 4. A supply voltage of between 9·0V and 18V will then cause V_{EEO} (pin 13) to be regulated at a level nominally 6·4V below V_{CCO}(pin 7). The regulator will, however, lose control with a potential difference of less than 9·0V. Below this level the voltage on pin 13 will track nominally 1·5V above the level of pin 12. When the regulator is not used (low voltage operation), pin 12 must be connected to V_{EEO} (pin 13).

OPERATING NOTES - REFER TO FIGS. 3 AND 4

Gyrator C1 (Pin 3) If the environment in which the device is operating limits the background light such that the DC component of the diode current has a maximum of 200μA, it may be desirable to omit (as in Fig. 3) the more bulky and costly 68μF capacitor (gyrator C1 shown in Fig. 4). In this case pin 3 can be left open circuit. The resultant application will then have a characteristic of greatly reduced gain when the ambient light causes the DC current to rise above this threshold. Alternatively,the 68μF capacitor can be replaced by a resistor.

The outcome of this is to further reduce the gain in ambient light levels above the 200μA threshold. Below this threshold the overall gain is slightly enhanced as the light level approaches the threshold value. If chosen, this resistance should lie between 10kΩ and 200kΩ .

Noise Immunity The stretch output can also be used as a means of improving performance relating to a receiver system, over and above its main purpose of providing a microprocessor interface. Including C8 (Fig. 4) causes the output pulses (from pin 9) to be subjected to the stretch input threshold. Thus any noise pulses from pin 9 that are below this threshold will not be seen at the stretch output (pin 11). A further improvement can be made, using this stretch input threshold, by including some additional filtering of the output (C10 in Fig. 4). This can be adjusted in value (typically 100pF) to reduce some of the noise pulses that otherwise cross the threshold, to a level below the threshold.

Screening Use of screening for the device, and associated components, improves the performance and immunity to externally radiated noise. The screening method used must protect the sensitive front-end of the device; provided that the diode, pin 1-pin 16, C2 (pin 2) and the first stage decoupling (pin 15) are screened, it may be found that for the application considered, the remalning circuitry need not be so protected. In applications where externally radiated noise is minimal, it may be possible to reduce any screening to pins 1 and 16 and the diode connections only. Screening may not be necessary in some instances, but this largely depends on the level of radiated noise, the decoupling/filtering employed and the receiver's decoding technique.

Decoupling Typical decoupling arrangements for use with or without the regulator are given in Figs. 4 and 3, respectively. When using the regulator, further improvements in high frequency supply rejection are possible by the inclusion of R2. The value can be chosen so as to keep the pin 12 end of R2 within the −9·0 to −18V (wrt pin 7) specified voltage range. For example, if the SL486 is used in a system with a supply of 16V, a typical value tor R2 would be 200Ω. Note that the regulator is a low impedance point between pins 12 and 13. C7 thus maintains a low impedance path between pins 4 and 12 at high frequencies.

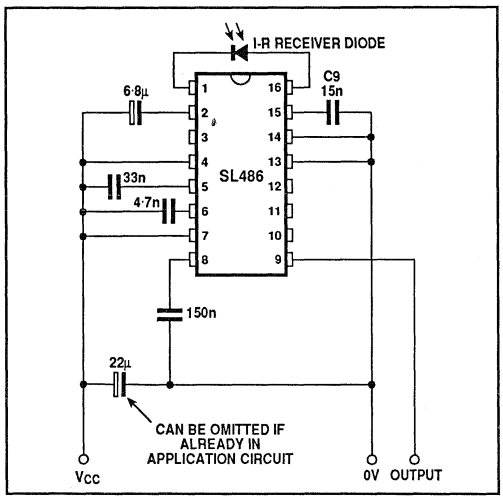


Fig. 3 Circuit diagram of minimum component application (low voltage operation)

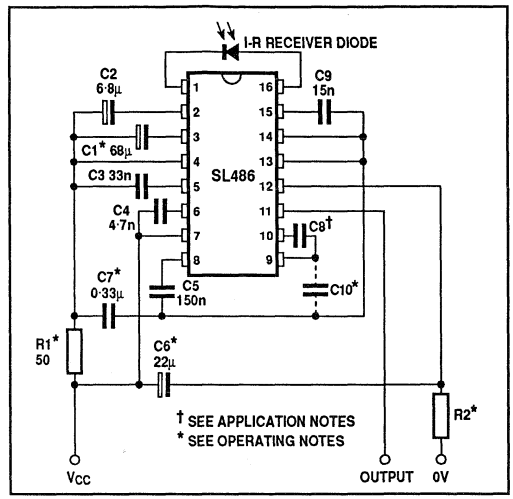


Fig. 4 SL486 application diagram showing all optional components (Note: supply decoupling and connections for use of voltage regulator, also pulse stretch output)

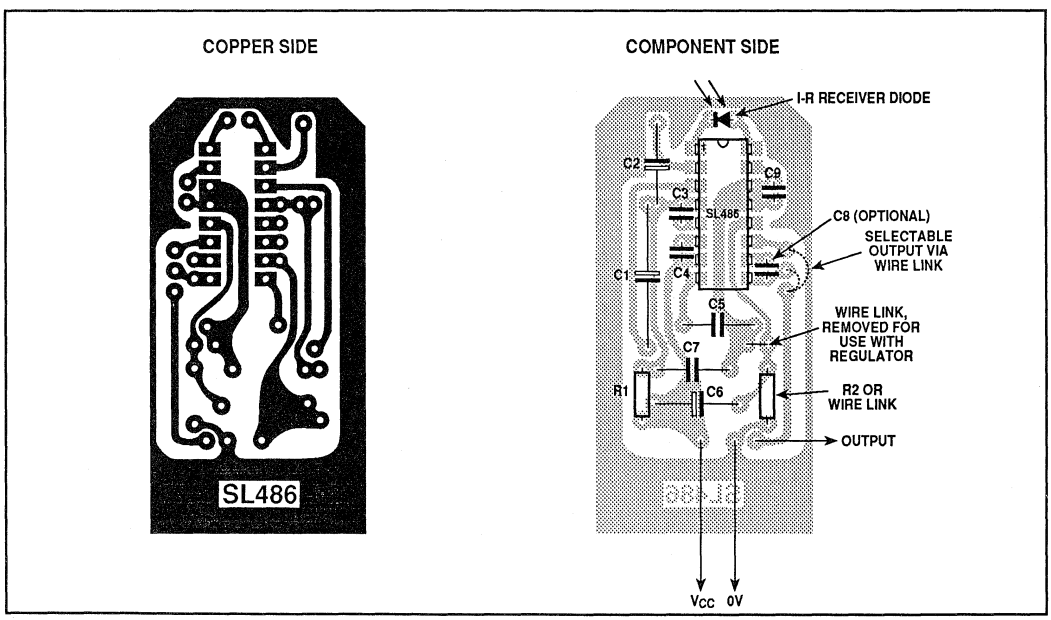


Fig. 5 PCB track (actual size)and component layout for the circuit of Fig. 4, using SL486 in DP16 package

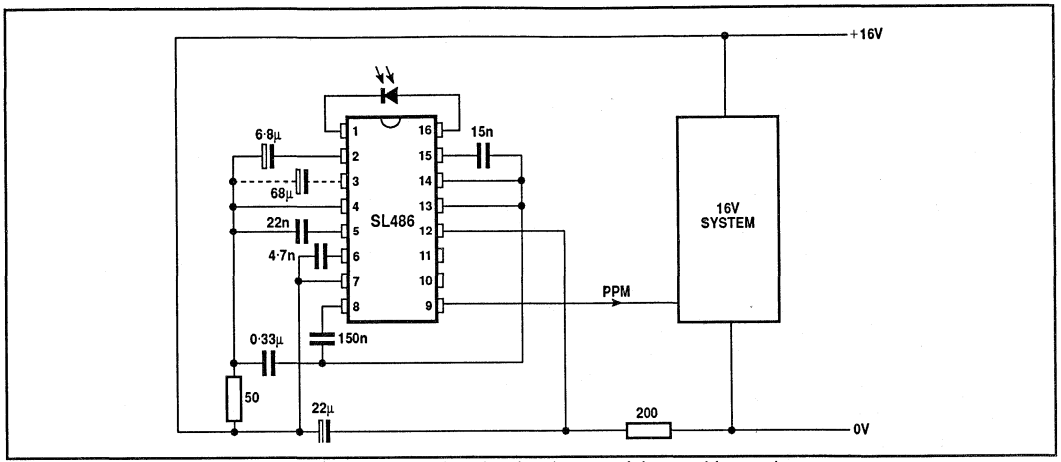


Fig. 6 SL486 application showing the use of the on-chip regulator

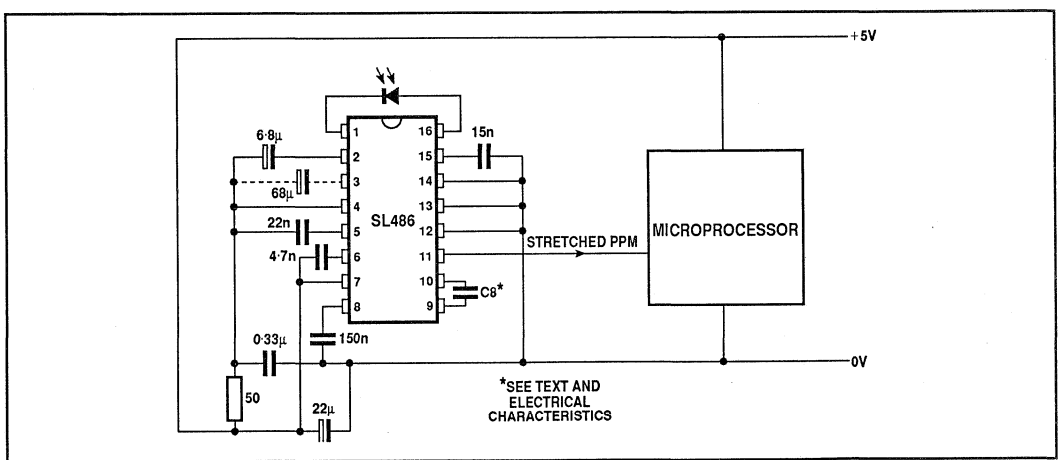


Fig. 7 Microprocessor interface, using the SL486 pulse stretching facility

SL490B

REMOTE CONTROL TRANSMITTER

GPS has developed and produced a range of monolithic integrated circuits which give a wide variety of remote control facilities. As well as ultrasonic or infra-red transmission, cable, radio or telephone links may also be used. Pulse Position Modulation (PPM) is used with or without carrier and automatic error detection is incorporated. Initially designed with TV remote control in mind, the device is also suitable for use in radios, tuners, tape and record decks, lamps and lighting, toys and models, industrial control and monitoring.

The SL490B is an easily extendable, 32-command PPM transmitter drawing negligible standby current.

FEATURES

- Ultrasonic or Infra-Red Transmission
- Direct Drive or Ultrasonic Transducer
- Direct Drive of Visible LED when using Infra-Red
- Very Low Power Requirements
- Pulse Position Modulation gives Excellent Immunity from Noise and Multipath Reflections
- Single Pole Key Matrix
- Switch Resistance up to 1kΩ Tolerated
- Low External Component Count
- On-Chip Anti-Bounce Circuitry

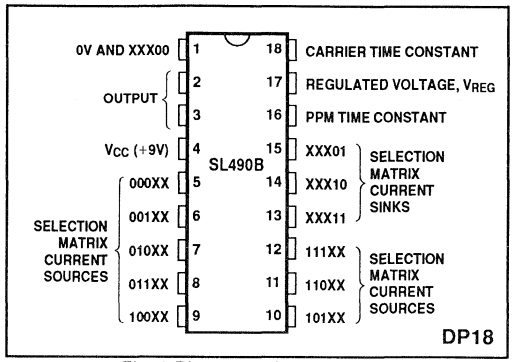


Fig. 1 Pin connections - top view

QUICK REFERENCE DATA

- Power Supply: 9V Standby 6μA, Operating 8mA
- Modulation: Pulse Position with or without Carrier
- Coding: 5-Bit Word giving a Primary Command Set of 32 Commands
- Key Entry: 8 × 4 Single Pole Key Matrix
- Data Rate: Selectable 1Bit/Sec to 10kBit/Sec.
- Carrier Frequency: Selectable 0Hz (No Carrier) to 200kHz

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+9·5V
Total power dissipation	600mW
Operating temperature range	−10°C to +60°C
Storage temperature range	−55°C to+150°C

ORDERING INFORMATION

SL490B NA DP

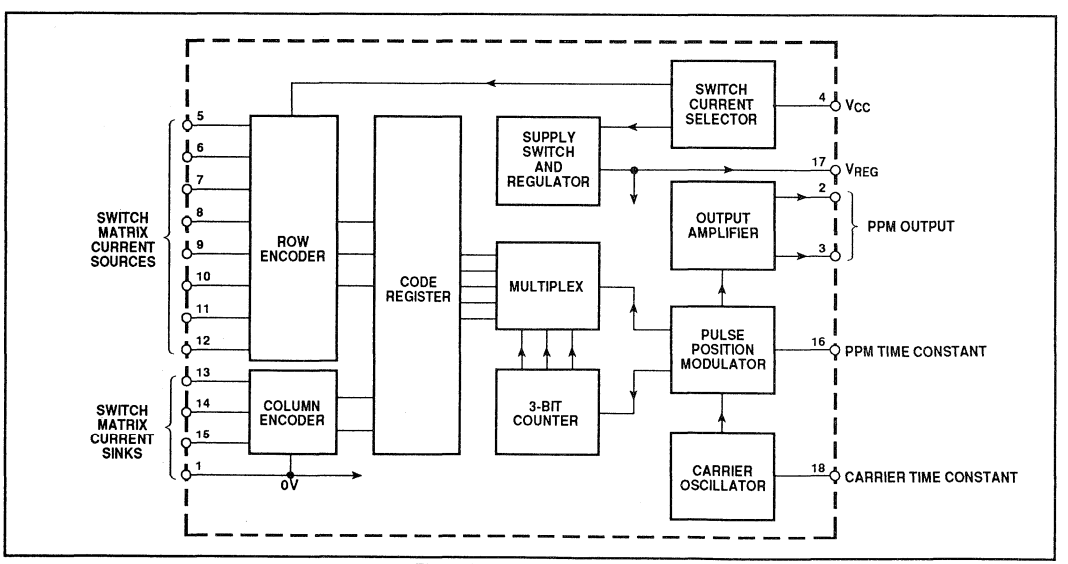


Fig. 2 SL486 block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{AMB} = +25°C, V_{CC} = +7V to +10·5V. Test circuit: Fig. 4. Timings are defined in Fig. 3.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating supply current	4		9·5	16	mA	V_{CC} = 9·5V
Standby supply current	4			10	µA	
Regulated voltage, V_{REG}	17	4·1		4·9	V	
Regulator output current, I_{REG}	17			1	mA	
Output voltage swing	2,3	$V_{CC}-1$			V	Unloaded
Output voltage	2			1	V	I_2 = 10mA } peak value <1ms
Output voltage	3			1	V	I_3 = 5mA } peak value <1ms
Keypad switch resistance	5-15			5	kΩ	
Carrier time constant resistor, R2	18	20	40	80	kΩ	C2 = 680pF, $f_C \approx$ 50kHz; see Fig. 4
PPM time constant resistor, R1	16	15	30	60	kΩ	
t_1 deviation from calculated value,	2,3			±10	%	R1 = 15kΩ } t_1 = 0·95C1R1, see
using fixed timing components				±10	%	R1 = 60kΩ } Fig. 4
Variation of t_1 and t_0 with V_{CC}						
Δt_1	2,3			±4	%	} ΔV_{CC} = 3·5V (7V to 10·5V)
Δt_0	2,3			±4	%	} ΔV_{CC} = 3·5V (7V to 10·5V)
Ratio t_0/t_1	2,3	1·4		1·6		
Pulse width, t_P	2,3	0·11t_1		0·22t_1		
Interword gap, t_g	2,3		3t_1			Derived by counting

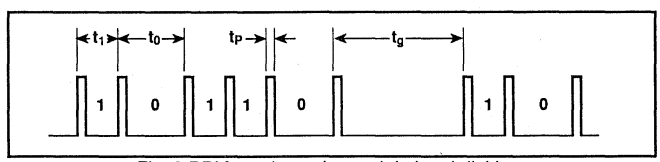


Fig. 3 PPM word notation and timing definitions

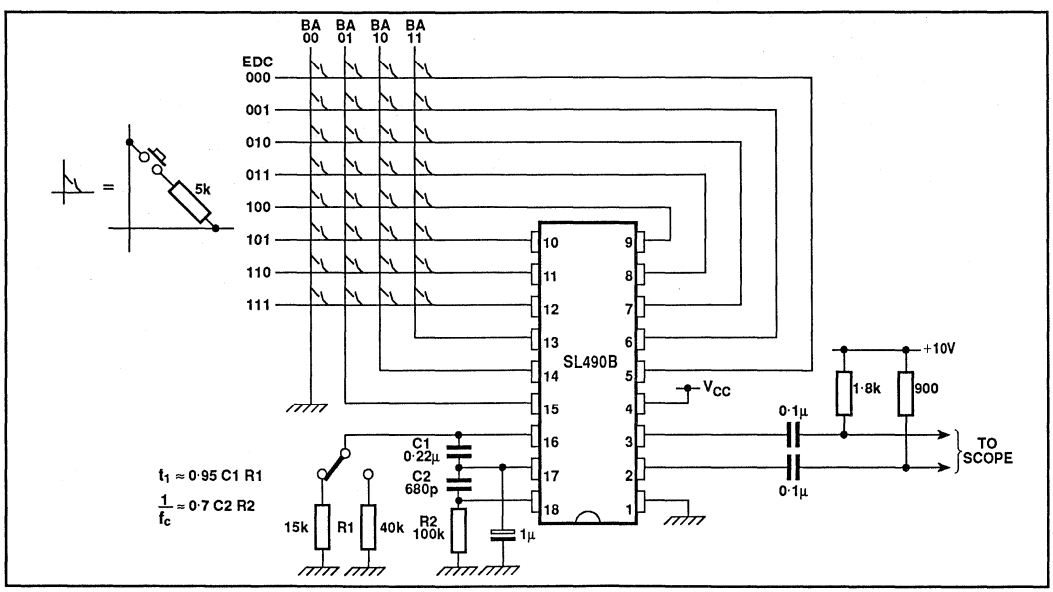


Fig. 4 Test circuit

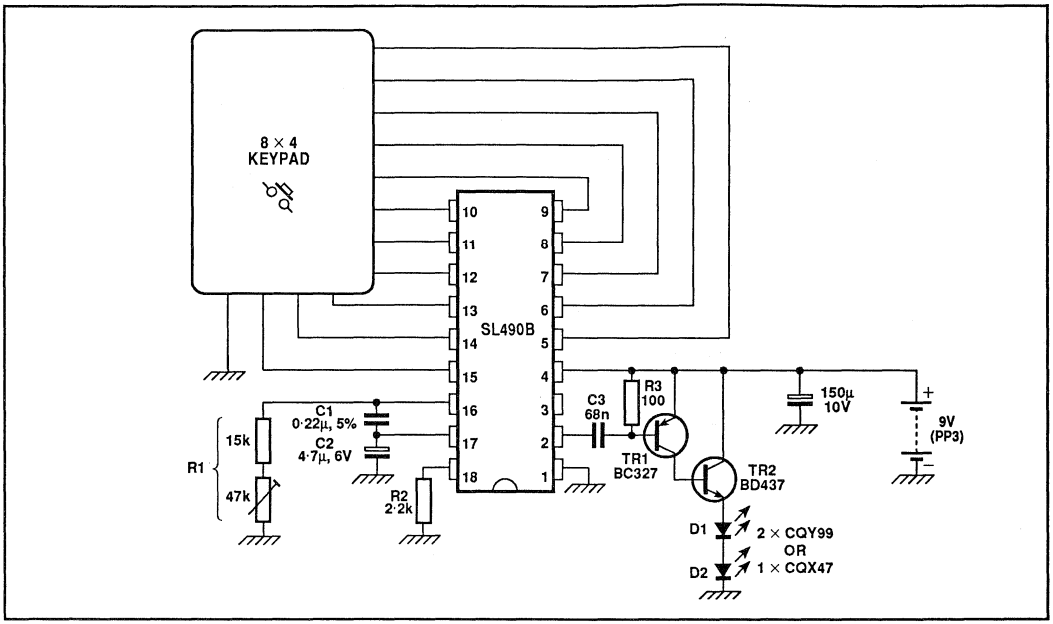


Fig. 5 Infra-red application circuit

OPERATING NOTES

Fig. 5 shows the circuit for a simple infra-red transmitter where the PPM output pulses from pin 2 of the SL490B are differentated by C3 and R3 and amplified by TR1 to produce current pulses about 15µs wide. These pulses are further amplified by TR2 and applied to the infra-red diodes D1 and D2.

The current in the diodes and the infra-red output is controlled by the quantity, type, and connection method of the diodes and also by the gain, at high currents, of the transistors.

The most common solution where cost is important is to use two single-chip diodes, such as the CQY99 connected in series.

Improved output can be obtained by using four CQY99 diodes in a series/parallel arrangement, but it is usually simpler to use two multi-chip diodes such as the CQX47 connected in parallel or a single CQX19, which gives similar results.

A significant increase in range can be obtained by using diodes such as the CQY99 in conjunction with a plated plastic parabolic reflector.

When building the transmitter, care should be taken with the choice of the capacitor C4 and with the circuit layout, particularly when multi-chip diodes are being used, as the current pulses can be as high as 6 to 8A.

Transistor choice is also important and any substitutes should have high current gain characteristics and switching speeds compatible with the application.

An increase in output can be obtained by connecting TR2 in common emitter configuration, but care should be taken not to exceed the rating of the diodes.

Choice of PPM Frequency

When the transmitter is being used with an infra-red link, with high current pulses fed to the diodes as in Fig. 5, power consumption will increase with frequency. It is thus advisable that, with a battery power supply, the slowest PPM rate consistent with adequate response time should be chosen.

Section 7

PWM Waveform Generators

GEC PLESSEY
SEMICONDUCTORS

MA818

THREE-PHASE PULSE WIDTH MODULATION WAVEFORM GENERATOR

The MA818 PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

The six TTL level PWM outputs (Fig. 2) control the six switches in a three-phase inverter bridge. This is usually via an external isolation and amplification stage.

Rotational frequency is defined to 12 bits for high accuracy and a zero setting is included in order to implement DC injection braking with no software overhead. Any power waveform can be implemented as this is user-defined in an external PROM/EPROM. For users requiring an on-chip pre-programmed waveform, the functionally identical MA828 is recommended.

Information contained within the pulse width modulated sequences controls the shape, power frequency, amplitude, and rotational direction (as defined by the red-yellow-blue phase sequence) of the output waveform. Parameters such as the carrier frequency, minimum pulse width, and pulse delay time may be defined during the initialisation of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in each output phase of the inverter bridge, in order to accommodate variations in the turn-on and turn-off times of families of power devices.

The MA818 is easily controlled by a microprocessor and its fully-digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral, reading the power waveform directly from a PROM/EPROM and requiring microprocessor intervention only when operating parameters need to be changed.

An 8-bit multiplexed data bus is used to receive addresses and data from the microprocessor/controller. This is a standard MOTEL™ bus, compatible with most microprocessors/controllers.

The MA818 is fabricated in CMOS for low power consumption.

FEATURES

- Fully Digital Operation
- Interfaces with Most Microprocessors
- Wide Power-Frequency Range
- Carrier Frequency Selectable up to 24kHz
- Waveform Stored in External PROM/EPROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- DC Injection Braking

MOTEL is a registered Trademark of Intel Corp. and Motorola Corp.

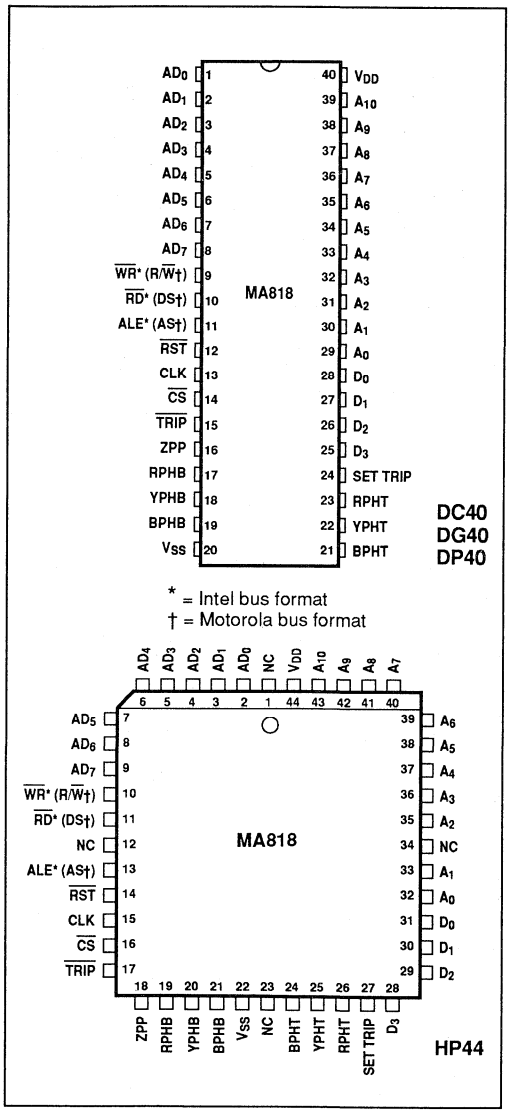


Fig. 1 Pin connections – top view (not to scale)

PIN DESCRIPTIONS

Pin.no. DC/DG/DP40	Pin.no. HP44	Name	Type	Function
1	2	AD_0	I	Multiplexed Address/Data (LSB)
2	3	AD_1	I	Multiplexed Address/Data
3	4	AD_2	I	Multiplexed Address/Data
4	5	AD_3	I	Multiplexed Address/Data
5	6	AD_4	I	Multiplexed Address/Data
6	7	AD_5	I	Multiplexed Address/Data
7	8	AD_6	I	Multiplexed Address/Data
8	9	AD_7	I	Multiplexed Address/Data(MSB)
9	10	Intel: $\overline{WR}$ Motorola: R/$\overline{W}$	I	Intel bus control: $\overline{\text{Write}}$ Strobe Motorola bus control: Read/$\overline{\text{Write}}$ select
10	11	Intel: $\overline{RD}$ Motorola: DS	I	Intel bus control: $\overline{\text{Read}}$ Strobe Motorola bus control: Data Strobe
11	13	Intel: ALE Motorola: AS	I	Intel bus control: Address Latch Enable Motorola bus control: Address Strobe
12	14	$\overline{RST}$	I	Reset internal counters, active low
13	15	CLK	I	Clock input
14	16	$\overline{CS}$	I	Chip Select input, active low
15	17	$\overline{TRIP}$	O	Output trip status; low = output tripped
16	18	ZPP	O	Zero Phase Pulse
17	19	RPHB	O	Red Phase, Bottom power switch
18	20	YPHB	O	Yellow Phase, Bottom power switch
19	21	BPHB	O	Blue Phase, Bottom power switch
20	22	V_{SS}	P	Negative power supply (0V)
21	24	BPHT	O	Blue Phase, Top power switch
22	25	YPHT	O	Yellow Phase, Top power switch
23	26	RPHT	O	Red Phase, Top power switch
24	27	SET TRIP	I	Set output trip. 90kΩ internal pull-up resistor
25	28	D_3	I	Eprom Data (LSB)
26	29	D_2	I	Eprom Data
27	30	D_1	I	Eprom Data
28	31	D_0	I	Eprom Data (MSB)
29	32	A_0	O	Eprom Address (LSB)
30	33	A_1	O	Eprom Address
31	35	A_2	O	Eprom Address
32	36	A_3	O	Eprom Address
33	37	A_4	O	Eprom Address
34	38	A_5	O	Eprom Address
35	39	A_6	O	Eprom Address
36	40	A_7	O	Eprom Address
37	41	A_8	O	Eprom Address
38	42	A_9	O	Eprom Address
39	43	A_{10}	O	Eprom Address (LSB)
40	44	V_{DD}	P	Positive power supply

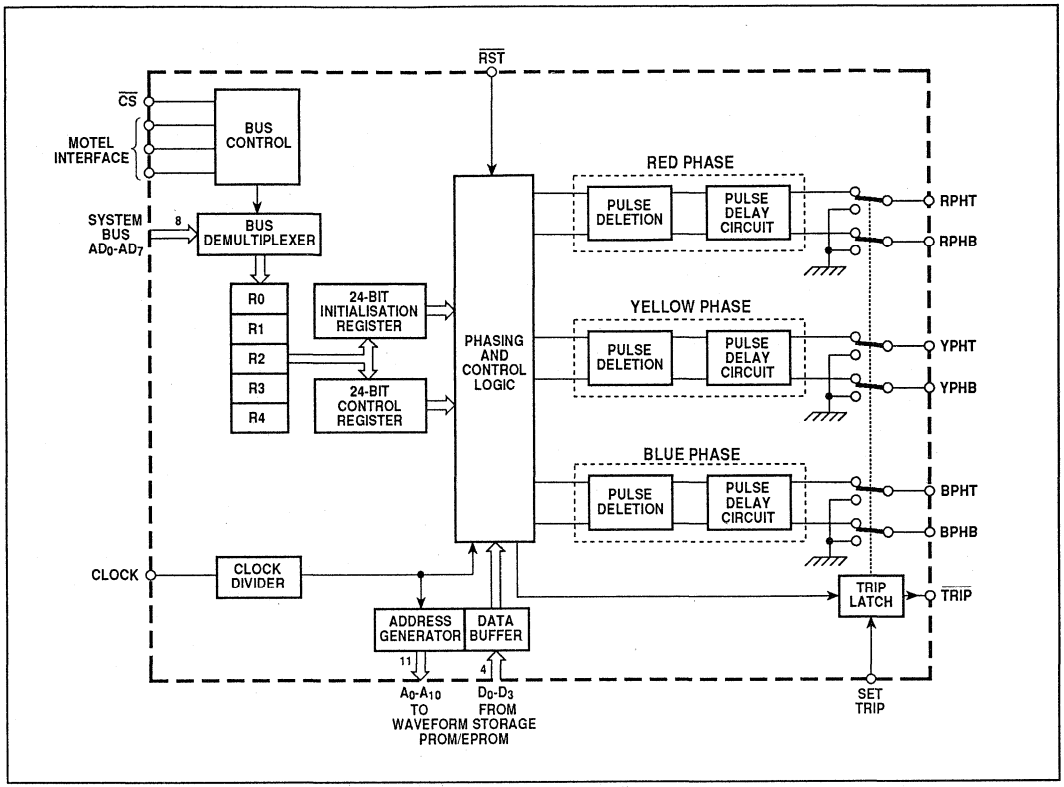


Fig. 2 MA818 internal block diagram

FUNCTIONAL DESCRIPTION

An asynchronous method of PWM generation is used with uniform or 'double-edged' regular sampling of the waveform stored in the PROM/EPROM as illustrated in Fig.3. The use of an external PROM/EPROM allows the user to define the optimum power waveform for the particular motor being used.

The triangle carrier wave frequency is selectable up to 24kHz (assuming the maximum clock frequency of 12.5MHz is used) enabling ultrasonic operation for noise critical applications. Power frequency ranges of up to 4kHz (with 12.5MHz clock) are possible, with the actual output frequency resolved to 12-bit accuracy within the chosen range in order to give precise motor speed control and smooth frequency changing. The output phase sequence of the PWM outputs can also be changed to allow both forward and reverse motor operation.

PWM output pulses can be 'tailored' to the inverter characteristics by defining the minimum allowable pulse width (the MA818 will delete all shorter pulses from the 'pure' PWM pulse train) and the pulse delay (underlap) time without the need for external circuitry. This gives cost advantages in both component savings and in allowing the same PWM circuitry to be used for control of a number of different motor drive circuits simply by changing the microprocessor software.

Power frequency amplitude control is also provided with an overmodulation option to assist in rapid motor braking.

An asynchronous trip input allows the PWM outputs to be shut down immediately, overriding the microprocessor control in the event of an emergency.

Other possible MA818 applications are as a 3-phase waveform generator as part of a switched-mode power supply (SMPS) or of an uninterruptible power supply (UPS). In such applications the high carrier frequency allows a very small switching transformer to be used.

MICROPROCESSOR INTERFACE

The MA818 interfaces to the controlling microprocessor by means of a multiplexed bus of the MOTEL format. This interface bus has the ability to adapt itself automatically to the format and timing of both MOTorola and IntEL interface buses (hence MOTEL). Internally, the detection circuitry latches the status of the DS/$\overline{RD}$ line when AS/ALE goes high. If the result is high. Then the Intel mode is used; if the result is low then the Motorola mode is used. This procedure is carried out each time that AS/ALE goes high. In practice this mode selection is transparent to the user. For bus connection and timing information refer to the description relevant to the microprocessor/controller being used.

Industry standard microprocessors such as the 8085, 8088, etc. and microcontrollers such as the 8051, 8052 and 6805 are all compatible with the interface on the MA818. This interface consists of 8 data lines, AD_0 - AD_7 (write only in this instance), which are multiplexed to carry both the address and data information, 3 bus control lines, labelled $\overline{WR}$,$\overline{RD}$ and ALE in Intel mode and R/$\overline{W}$, DS and AS in Motorola mode, and a Chip Select input. $\overline{CS}$, which allows the MA818 to share the same bus as other microprocessor peripherals. It should be noted that all bus timings are derived from the microprocessor and are independent of the MA818 clock input.

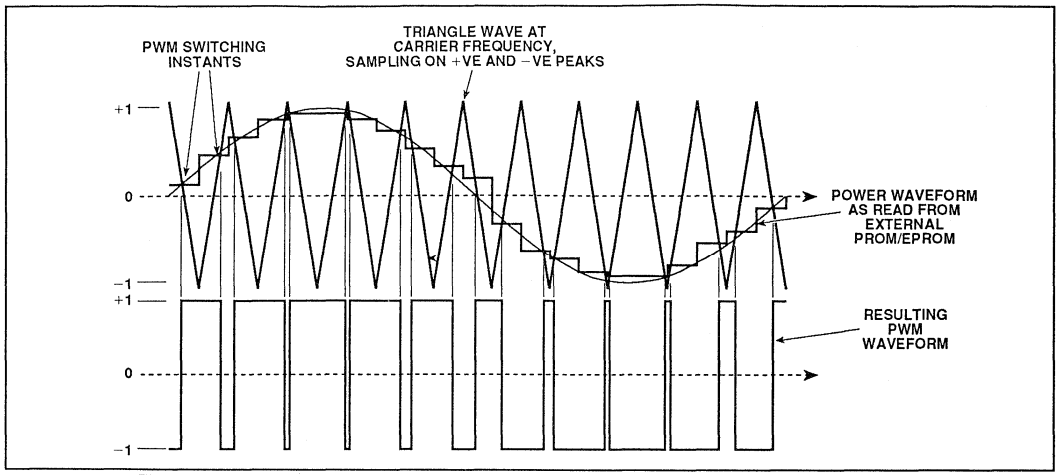


Fig. 3 Asynchronous PWM generation with'double-edged' regular sampling as used by the MA818

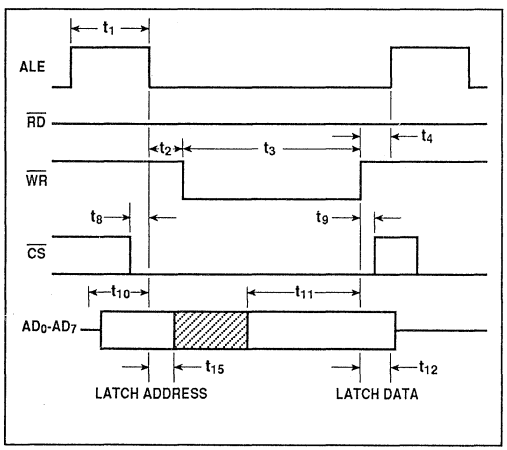


Fig. 4 Intel bus timing definitions

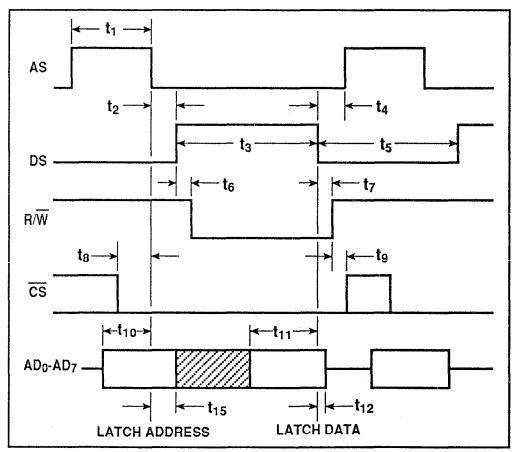


Fig. 5 Motorola bus timing definitions

Parameter	Symbol	Min.	Units
ALE high period	t_1	70	ns
Delay time, ALE to $\overline{WR}$	t_2	40	ns
$\overline{WR}$ low period	t_3	200	ns
Delay time, $\overline{WR}$ high to ALE high	t_4	40	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Data setup time	t_{11}	100	ns
Data hold time	t_{12}	30	ns

Table 1 Intel bus timings at V_{DD} = 5V, T_{AMB} = +25°C

Parameter	Symbol	Min.	Units
AS high period	t_1	90	ns
Delay time, as low to DS high	t_2	40	ns
DS high period	t_3	210	ns
Delay time, DS low to AS high	t_4	40	ns
DS low period	t_5	200	ns
DS high to R/$\overline{W}$ low setup time	t_6	10	ns
R/$\overline{W}$ hold time	t_7	10	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Write data setup time	t_{11}	110	ns
Write data hold time	t_{12}	30	ns

Table 2 Motorola bus timings at V_{DD} = 5V, T_{AMB} = +25°C

MICROPROCESSOR BUS TIMING

Intel Mode (Fig. 4 and Table 1)

The address is latched by the falling edge of ALE. Data is written from the bus into the MA818 on the rising edge of $\overline{WR}$. $\overline{RD}$ is not used in this mode because the registers in the MA818 are write only. However, this pin must be connected to $\overline{RD}$ (or tied high) to enable the MA818 to select the correct interface format.

Motorola Mode (Fig. 5 and Table 2)

The address is latched on the falling edge of the AS line. Data is written from the bus into the MA818 (only when R/$\overline{W}$ is low) on the falling edge of DS (providing $\overline{CS}$ is low).

CONTROLLLNG THE MA818

The MA818 is controlled by loading data into two 24-bit registers via the microprocessor interface. These registers are the initialisation register and the control register.

The initialisation register would normally be loaded before motor operation (i.e., prior to the PWM outputs being activated) and sets up the basic operating parameters associated with the motor and inverter. This data would not normally be updated during motor operation.

The control register is used to control the PWM outputs (and hence the motor) during operation e.g., stop/start, speed, forward/reverse etc. and would normally be loaded and changed only after the initialisation register has been loaded.

As the MOTEL bus interface is restricted to an 8-bit wide format, data to be loaded into either of the 24-bit register is first written to three 8-bit temporary registers R0, R1 and R2 before being transferred to the desired 24-bit register. The data is accepted (and acted upon) only when transferred to one of the 24-bit registers.

Transfer of data from the temporary registers to either the initialisation register or the control register is achieved by a write instruction to a dummy register. Writing to dummy register R3 results in data transfer from R0, R1 and R2 to the control register, while writing to dummy register R4 transfers data from R0, R1 and R2 to the initialisation register. It does not matter what data is written to the dummy registers R3 and R4 as they are not real registers. It is merely the write instruction to either of these registers which is acted upon in order to load the initialisation and control registers.

AD_2	AD_1	AD_0	Register	Comment
0	0	0	R0	Temporary register R0
0	0	0	R1	Temporary register R1
0	1	0	R2	Temporary register R2
0	1	0	R3	Transfers control data
1	0	1	R4	Transfers initialisation data

Table 3 MA818 register addressing

Initialisation Register Function

The 24-bit initialisation register contains parameters which, under normal operation, will be defined during the power-up sequence. These parameters are particular to the drive circuitry used, and therefore changing these parameters during a PWM cycle is not recommended. Information in this register should only be modified while $\overline{RST}$ is active (i.e. low) so that the PWM outputs are inhibited (low) during the updating process.

The parameters set in the initialisation register are as follows:

Carrier frequency

Low carrier frequencies reduce switching losses whereas high carrier frequencies increase waveform resolution and can allow ultrasonic operation.

Power frequency range

This sets the maximum power frequency that can be carried within the PWM output waveforms. This would normally be set to a value to prevent the motor system being operated outside its design parameters.

Pulse delay time ('underlap')

For each phase of the PWM cycle there are two control signals, one for the top switch connected to the positive inverter DC supply and one for the bottom switch connected to the negative inverter DC supply. In theory, the states of these two switches are always complementary. However, due to the finite and non-equal turn-on and turn- off times of power devices, it is desirable when changing the state of the output pair, to provide a short delay time during which both outputs are off in order to avoid a short circuit through the switching elements.

Pulse deletion time

A pure PWM sequence produces pulses which can vary in width between 0% and 100% of the duty cycle. Therefore, in theory, pulse widths can become infinitesimally narrow. In practice this causes problems in the power switches due to storage effects and therefore a minimum pulse width time is required. All pulses shorter than the minimum specified are deleted.

Counter reset

This facility allows the internal power frequency counter of the MA818 to be set to zero, disabling the normal frequency control and giving a 50% output duty cycle.

Initialisation Register Programming

The initialisation register data is loaded in 8-bit segments into the three 8-bit temporary registers R0-R2. When all the initialisation data has been loaded into these registers it is transferred into the 24-bit initialisation register by writing to the dummy register R4.

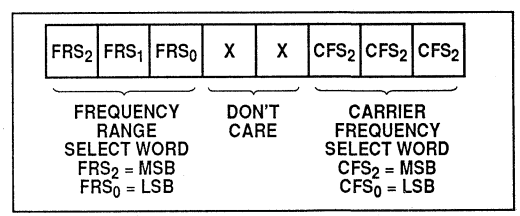


Fig. 6 Temporary register R1

Carrier frequency selection

The carrier frequency is a function of the externally applied clock frequency and a division ratio *n*, determined by the 3-bit CFS word set during initialisation. The values of *n* are selected as shown in Table 4.

CFS word	101	100	011	010	001	000
Value of n	32	16	8	4	2	1

Table 4 Values of clock division ratio n

The carrier frequency, f_{CARR}, is then given by:

$$f_{CARR} = \frac{k}{512 \times n}$$

where k = clock frequency and n = 1, 2, 4, 8, 16 or 32 (as set by CFS)

Power frequency range selection

The power frequency range selected here defines the maximum limit of the power frequency. The operating power frequency is controlled by the 12-bit Power Frequency Select (PFS) word in the control register but may not exceed the value set here.

The power frequency range is a function of the carrier waveform frequency (f_{CARR}) and a multiplication factor m, determined by the 3-bit FRS word. The value of m is determined as shown in Table 5.

FRS word	110	101	100	011	010	001	000
Value of m	64	32	16	8	4	2	1

Table 5 Values of carrier frequency multiplicaion factor m

The power frequency range, f_{RANGE}, is then given by:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

where f_{CARR} = carrier frequency and m = 1, 2, 4, 8, 16, 32 or 64 (as set by CFS).

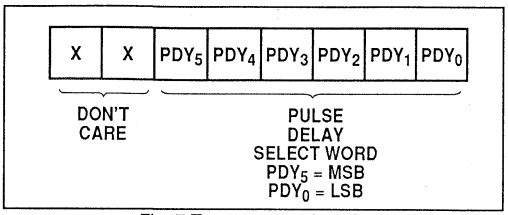


Fig. 7 Temporary register R2

Pulse delay time

The pulse delay time affects all six PWM outputs by delaying the rising edges of each of the outputs by an equal amount.

The pulse delay time is a function of the carrier waveform frequency and *pdy*, defined by the 6-bit pulse delay time select word (PDY). The value of *pdy* is selected as shown in Table 6.

PDY word	111111	111110	...etc...	000000
Value of pdy	1	2	...etc...	64

Table 6 Values of pdy

The pulse delay time, t_{pdy}, is then given by:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

where *pdy* = 1-64 (as set by PDY) and f_{CARR} = carrier frequency. Fig 8 shows the effect of the pulse delay circuit.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig. 2), the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set in the initialisation register. The actual shortest pulse generated is given by $t_{pd} - t_{pdy}$.

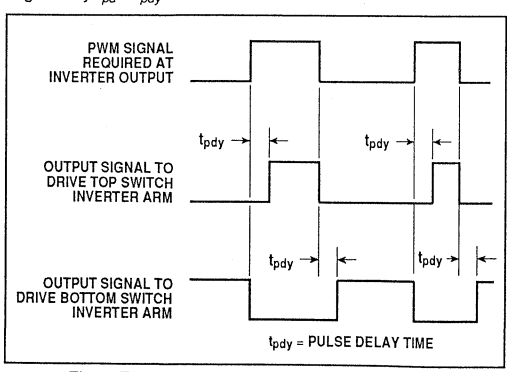


Fig. 8 Effect of pulse delay on PWM pulse train

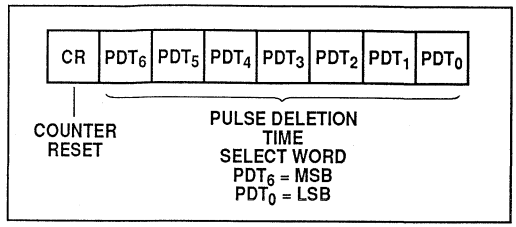


Fig. 9 Temporary register R0

Pulse deletion time

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the initialisation register. If a pulse (either positive or negative) is greater than or equal in duration to the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, t_{pd}, is a function of the carrier wave frequency and *pdt*, defined by the 7-bit pulse deletion time word (PDT). The value of *pdt* is selected as shown in Table 7.

PDT word	1111111	1111110	...etc...	0000000
Value of pdt	1	2	...etc...	128

Table 7 Values of pdt

The pulse deletion time, t_{pd}, is then given by:

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

where *pdt* = 1-128 (as set by PDT) and f_{CARR} = carrier frequency.

Fig. 10 shows the effect of pulse deletion on a pure PWM waveform.

Counter reset

When the CR bit is active (i.e., low) the internal power frequency phase counter is set to 0 degrees for the red phase. The power frequency is then set to 0Hz and cannot be changed via the normal frequency control.

Control Register Function

This 24-bit register contains the parameters that would normally be modified during PWM cycles in order to control the operation of the motor.

The parameters set in the control register are as follows:

Power frequency (speed)

Allows the power frequency of the PWM outputs to be adjusted within the range specified in the initialisation register

Forward/reverse

Allows the direction of rotation of the AC motor to be changed by changing the phase sequence of the PWM outputs.

Power frequency amplitude

By altering the widths of the PWM output pulses while maintaining their relative widths, the amplitude of the power waveform is effectively altered whilst maintaining the same power frequency.

Overmodulation

Allows the output waveform amplitude to be doubled so that a quasi-squarewave is produced. A combination of overmodulation and a lower power frequency can be used to achieve rapid braking in AC motors.

Output inhibit

Allows the outputs to be set to the low state while the PWM generation continues internally. Useful for temporarily inhibiting the outputs without having to to change other register contents.

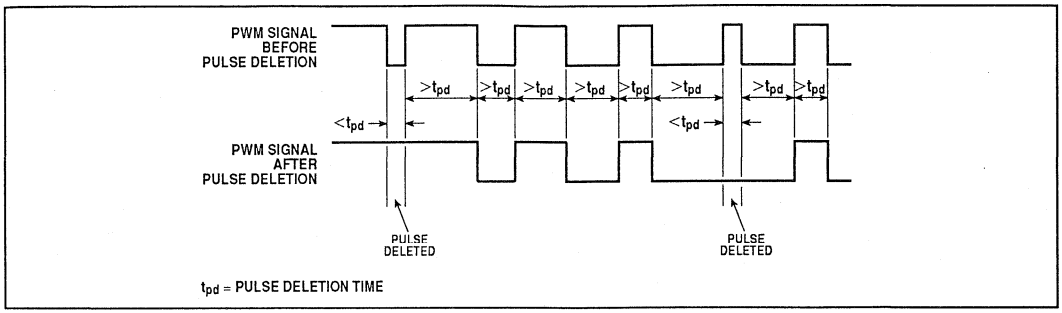


Fig. 10 The effect of the pulse deletion circuit

Control Register Programming

The control register should only be programmed once the initialisation register contains the basic operating parameters of the MA818.

As with the initialisation register, control register data is loaded into the three 8-bit temporary registers R0 - R2. When all the data has been loaded into these registers it is transferred into the 24-bit control register by writing to the dummy register R3. It is recommended that all three temporary registers are updated before writing to R3 in order to ensure that a conformal set of data is transferred to the control register for execution.

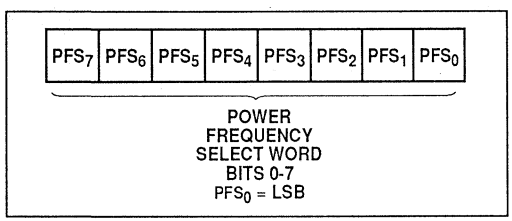


Fig. 11 Temporary register R0

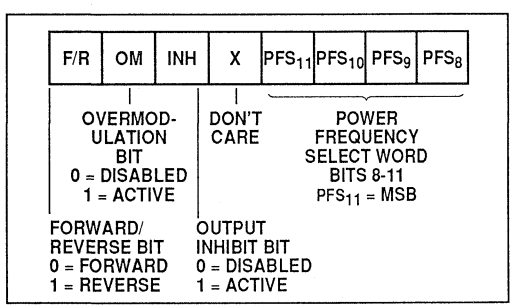


Fig. 12 Temporary register R1

Power frequency selection

The power frequency is selected as a proportion of the power frequency range (defined in the initialisation register) by the 12-bit power frequency select word, PFS, allowing the power frequency to be defined in 4096 equal steps. As the PFS word spans the two temporary registers R0 and R1 it is therefore essential, when changing the power frequency, that both these registers are updated before writing to R3.

The power frequency (f_{POWER}) is given by:

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

where *pfs* = decimal value of the 12-bit PFS word and f_{RANGE} = power frequency range set in the initialisation register.

Output inhibit selection

When active (i.e., low) the output inhibit bit INH sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When the inhibit is released the PWM outputs continue immediately. Note that as the inhibit is asserted after the pulse deletion and pulse delay circuits, pulses shorter than the normal minimum pulse width may be produced initially.

Overmodulation selection

The overmodulation bit OM is, in effect, the ninth bit (MSB) of the amplitude word. When active (i.e., high) the output waveform will be controlled in the 100% to 200% range by the amplitude word.

The percentage amplitude control is now given by:

$$\text{Overmodulated Amplitude} = A_{POWER} \times 100\%$$

where A_{POWER} = the power amplitude

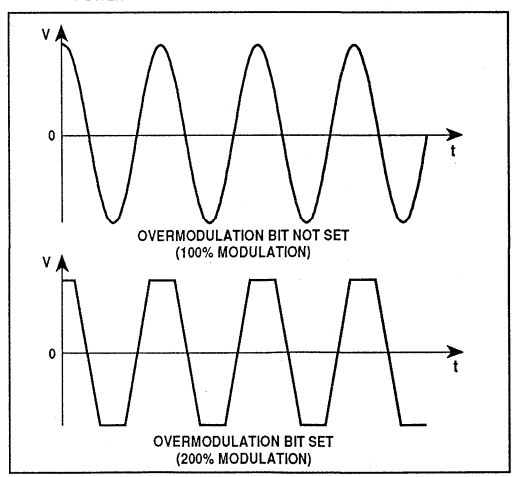


Fig. 13 Voltage waveforms as seen at the motor terminals, showing the effect of setting the overmodulation bit

Forward/ reverse selection

The phase sequence of the three-phase PWM output waveforms is controlled by the Forward/Reverse bit F/R. The actual effect of changing this bit from 0 (forward) to 1 (reverse) is to reverse the power frequency phase counter from incrementing the phase angle to decrementing it. The required output waveforms are all continuous with time during a forward/ reverse change.

In the forward mode the output phase sequence is red-yellow-blue and in the reverse mode the sequence is blue-yellow-red.

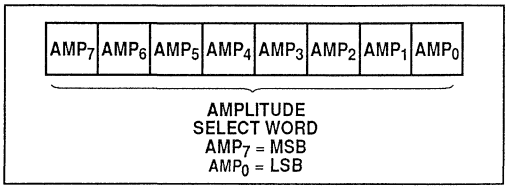


Fig.14 Temporary register R2

Amplitude selection

The power waveform amplitude is determined by scaling the amplitude of the waveform samples stored in the external PROM/EPROM by the value of the 8-bit amplitude select word (AMP).

The percentage amplitude control is given by:

$$\text{Power Amplitude, } A_{POWER} = \frac{A}{225} \times 100\%$$

where A = decimal value of AMP.

MA818 PROGRAMMING EXAMPLE

The following example assumes that a master clock of 12·288 MHz is used (12·288 MHz crystals are readily available). This clock frequency will allow a maximum carrier frequency of 24 kHz and a maximum power frequency of 4 kHz.

Initialisation Register Programming Example

A power waveform range of up to 250Hz is required with a carrier frequency of 6kHz, a pulse deletion time of 10µs and an underlap of 5µs.

1. Setting the carrier frequency

The carrier frequency should be set first as the power frequency, pulse deletion time and pulse delay time are all defined relative to the carrier frequency.

We must calculate the value of n that will give the required carrier frequency:

$$f_{CARR} = \frac{k}{512 \times n}$$

$$\Rightarrow \mathbf{n} = \frac{k}{512 \times f_{CARR}} = \frac{12{\cdot}288 \times 10^6}{512 \times 6 \times 10^3} = \mathbf{4}$$

From Table 4, n = 4 corresponds to a 3-bit CFS word of 010 in temporary register R1.

2. Setting the power frequency range

We must calculate the value of m that will give the required power frequency:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

$$\Rightarrow \mathbf{m} = \frac{f_{RANGE} \times 384}{f_{CARR}} = \frac{250 \times 384}{6 \times 10^3} = \mathbf{16}$$

From Table 5, m = 16 corresponds to a 3-bit FRS word of 100 in temporary register R1.

3. Setting the pulse delay time

As the pulse delay time affects the actual minimum pulse width seen at the PWM outputs, it is sensible to set the pulse delay time before the pulse deletion time, so that the effect of the pulse delay time can be allowed for when setting the pulse deletion time.

We must calculate the value of *pdy* that will give the required pulse delay time:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdy} = t_{pdy} \times f_{CARR} \times 512$$

$$= 5 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{15{\cdot}4}$$

However, the value of *pdy* must be an integer. As the purpose of the pulse delay is to prevent 'shoot-through' (where both top and bottom arms of the inverter are on simultaneously), it is sensible to round the pulse delay time up to a higher, rather than a lower figure.

Thus, if we assign the value 16 to *pdy* this gives a delay time of 5·2µs. From Table 6, *pdy* = 16 corresponds to a 6-bit PDY word of 110000 in temporary register R2.

4. Setting the pulse deletion time

In setting the pulse deletion time (i.e., the minimum pulse width) account must be taken of the pulse delay time, as the actual minimum pulse width seen at the PWM outputs is equal to $t_{pd} - t_{pdy}$.

Therefore, the value of the pulse deletion time must, in this instance, be set 5·2µs longer than the minimum pulse length required

Minimum pulse length required = 10µs

∴ tPD to be set to 10µs+5·2µs = 15·2µs

Now,

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdt} = f_{pd} \times f_{CARR} \times 512$$

$$= 15{\cdot}2 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{46{\cdot}7}$$

Again, *pdt* must be an integer and so must be either rounded up or down – the choice of which will depend on the application. Assuming we choose in this case the value 46 for *pdt*, this gives a value of t_{pd} of 15 µs and an actual minimum pulse width of 15−5·2µs = 9·8µs.

From Table 7, *pdt* = 46 corresponds to a value of PDT, the 7-bit word in temporary register R0 of 1010010.

The data which must be programmed into the three temporary registers R0, R1 and R2 (for transter into the initialisation register) in order to achieve the parameters in the example given, is shown in Fig. 15.

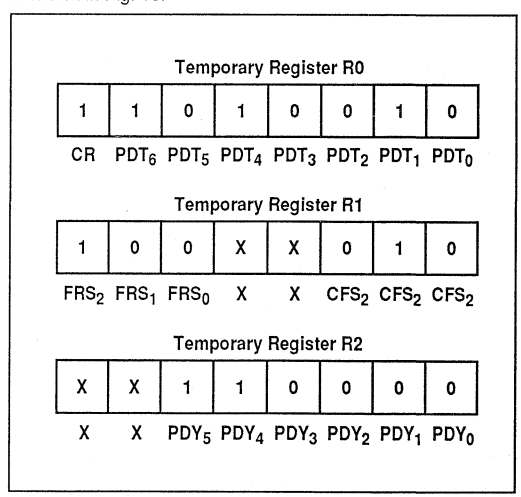


Fig. 15

Control Register Programming Example

The control register would normally be updated many times while the motor is running, but just one example is given here. It is assumed that the initialisation register has already been programmed with the parameters given in the previous example.

A power waveform of 100Hz is required with a PWM waveform amplitude of 80% of that stored in the EPROM. The phase sequence should be set to give forward motor rotation. The outputs should be enabled and no overmodulation is required.

1. Setting the power frequency

The power frequency, f_{POWER}, can be selected to 12-bit accuracy (i.e 4096 equal steps) from 0Hz to f_{RANGE} as defined in the initialisation register. In this case, with f_{RANGE} = 250Hz, the power frequency can be adjusted in increments of 0·06Hz.

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

$$\Rightarrow \mathbf{pfs} = \frac{f_{POWER} \times 4096}{f_{RANGE}} = \frac{100 \times 4096}{250} = \mathbf{1638{\cdot}4}$$

We can only have *pfs* as an integer, so if we assign *pfs* = 1638 this gives f_{POWER} = 99.97 Hz. The 12-bit binary equivalent of this value gives a PFS word of 011001100110 in temporary registers R0 and R1.

2. Setting overmodulation, forward/reverse, output inhibit

Overmodulation is not required therefore OM = 0.

Forward motor control is required (i.e., the phase sequence of the PWM outputs should be red-yellow-blue) therefore forward/reverse bit F/R = 0.

Output inhibit should be inactive (i e., the outputs should be active), therefore INH= 1.

These bits are all set in temporary register R1.

3. Setting the power waveform amplitude

$$A_{POWER} = \frac{A}{225} \times 100\%$$

$$\Rightarrow \mathbf{A} = \frac{A_{POWER} \times 255}{100} = \frac{80 \times 255}{100} = \mathbf{204}$$

The 8-bit binary equivalent of this value gives an AMP word of 11001100 in temporary register R2. The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the control register) in order to achieve the parameters in the example given, is shown in Fig. 16.

Temporary Register R0

0	1	1	0	0	0	1	1
PFS_7	PFS_6	PFS_5	PFS_4	PFS_3	PFS_2	PFS_1	PFS_0

Temporary Register R1

0	0	1	X	0	1	1	0
F/R	OM	INH	X	PFS_{11}	PFS_{10}	PFS_9	PFS_8

Temporary Register R2

1	1	0	0	1	1	0	0
AMP_7	AMP_6	AMP_5	AMP_4	AMP_3	AMP_2	AMP_1	AMP_0

Fig. 16

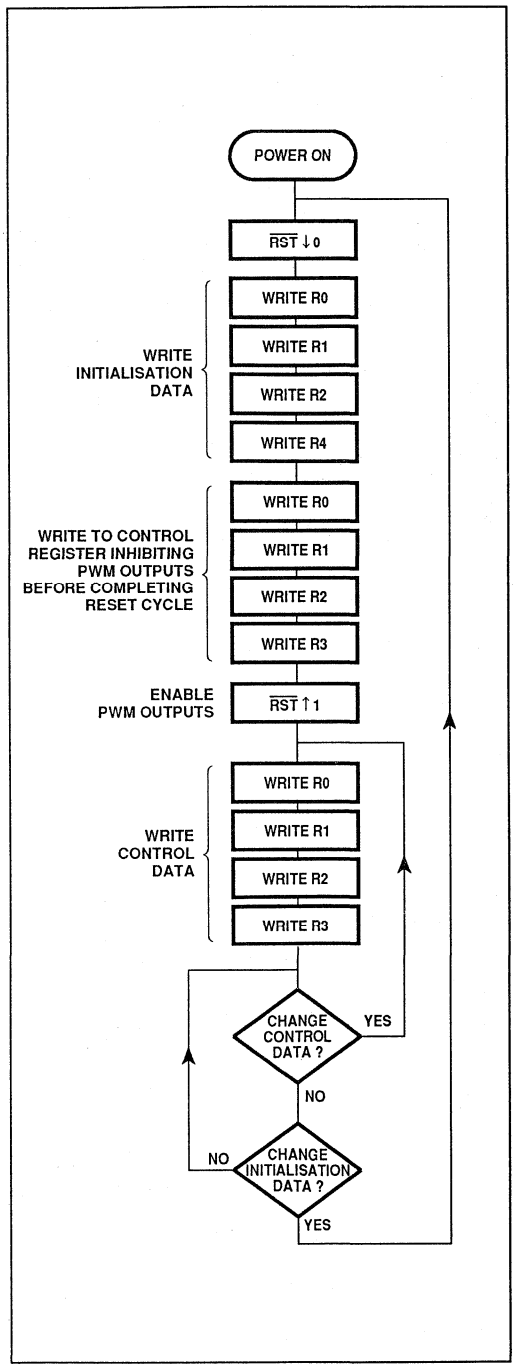


Fig. 17 Typical MA818 programming routine

HARDWARE INPUT/OUTPUT FUNCTIONS

Set Output Trip (SET TRIP input)

The SET TRIP input is provided separately from the microprocessor interface in order to allow an external source to override the microprocessor and provide a rapid shutdown facility. For example, logic signals from overcurrent sensing circuitry or the microprocessor 'watchdog' might be used to activate this input.

When the SET TRIP input is taken to a logic high, the output trip latch is activated. This results in the $\overline{TRIP}$ output and the six PWM outputs being latched low immediately. This condition can only be cleared by applying a reset cycle to the $\overline{RST}$ input.

Because of the asynchronous nature of the SET TRIP input, it is important that when not in use it is tied low and isolated from potential sources of noise. On no account should this input be left floating.

Output Trip Status ($\overline{TRIP}$ output)

The $\overline{TRIP}$ output indicates the status of the output trip latch and is active low.

Reset ($\overline{RST}$ input)

The $\overline{RST}$ input performs the following functions when activbe (low):

1. All PWM outputs are forced low (if not already low) thereby turning off the drive switches.
2. All internal counters are reset to zero (this corresponds to 0° for the red phase output).
3. The rising edge of $\overline{RST}$ reactivates the PWM outputs resetting the output trip and setting the $\overline{TRIP}$ output high – assuming that the SET TRIP input is inactive (i.e. low).

Zero Phase Pulse (ZPP output)

The ZPP output provides pulses at the same frequency as the power frequency with a 1 : 2 mark-space ratio. When in the forward mode of operation the falling edge of ZPP corresponds to 0° for the red phase PWM output. In the reverse mode, the rising edge of ZPP corresponds to 0° for the red phase PWM output.

Clock (CLK input)

The CLK input provides a timing reference used by the MA818 for all timings related to the PWM outputs. The microprocessor interface, however, derives all its timings from the microprocessor and therefore the microprocessor and the MA818 may be run either from the same or from different clocks.

PWM WAVEFORM ASSIGNMENT

The waveform amplitude data used to construct the PWM output sequences is read by the MA818 from an external 2K×8 PROM/EPROM. The use of an external PROM/EPROM allows the user to define the exact waveform required.

Waveform Definition

Good waveform resolution is achieved by storing 768 8-bit amplitude samples representing the positive 180° span of the waveform. It is assumed that the data is symmetrical about the 90° axis.

The MA818 constructs the full 360° waveform by assigning negative values to the same samples for the second half of the cycle. It uses these samples to calculate the three instantaneous amplitudes for all three phases. The 768 8- bit samples are linearly spaced over the 0° to 180° span, giving an angular resolution of approximately 0·23°

Waveform segment	Sample number
0°- 60°	0 - 255
60·23°- 120°	256 - 511
120·23°- 179·77°	512 - 767

Table 8 180° of the 360° cycle is divided into 768 8-bit samples

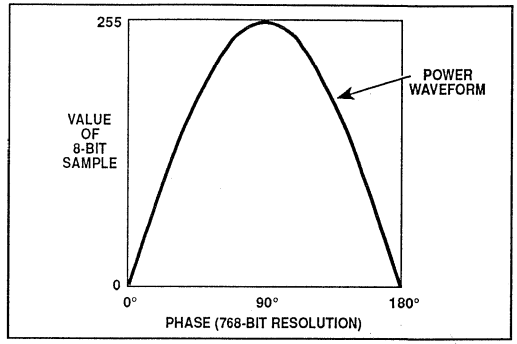


Fig. 18 180° sample of typical power waveform

WAVEFORM STORAGE

An industry standard 2K×8 PROM or EPROM (2716 or 27C16) is required for waveform storage. As less than half the memory capacity of the PROM/EPROM is needed to store the waveform, this is used to advantage in order to minimise the pin count of the MA818. Each 8-bit data word representing a sample of the waveform is stored as two 4-bit nibbles in the least significant nibble position of the 8-bit PROM/EPROM locations. Hence the most significant nibble is unused (and may therefore be left unprogrammed) so only 4 data lines (D_0 - D_3) are required.

The 768 waveform samples are therefore stored as 1546 four-bit samples. Fig. 19 illustrates the method used for mapping the data into the PROM/EPROM. The least signiflcant nibbles are stored sequentially from location 0_H to 300_H, and the most significant nibbles are stored from 400_H to 700_H. The MA818 reads Ihe data by accessing the two 4-bit nibbles (using A_{10} to select the high and low nibble memory areas) and then concatenates them internally to form the 8-bit waveform sample byte.

The reading of data from the the PROM/EPROM is performed automatically by the MA818 without microprocessor intervention whenever the PWM generation is active.

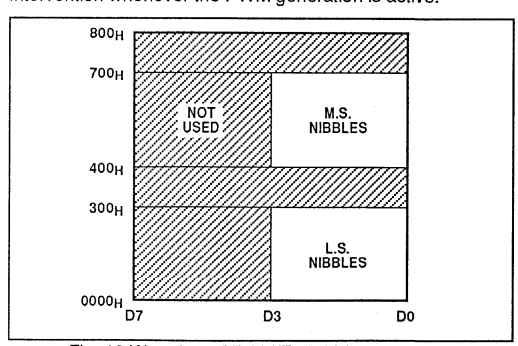


Fig. 19 Waveform PROM/EPROM memory map

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):
V_{DD} = +5V±5%, T_{AMB} = +25°C

DC Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input high voltage	V_{IH}	2			V	
Input low voltage	V_{IL}			0·8	V	
Input leakage current	I_{IN}			10	µA	$V_{IN} = V_{SS}$ or V_{DD}
Output high voltage	V_{OH}	4·0	>4·5		V	I_{OH} = −4mA
Output low voltage	V_{OL}		<0·2	0·4	V	I_{OL} = 4mA
Supply current (static)	$I_{DD\ (static)}$			100	µA	All outputs open circuit
Supply current (dynamic)	$I_{DD\ (dynamic)}$		<10	20	mA	f_{CLK} = 10MHz
Supply voltage	V_{DD}	4·75	5·0	7·5	V	

NOTE 1. The SET TRIP input has an internal pull-up resistor with an approximate value of 90kΩ

AC Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock frequency	f_{CLK}			12·5	MHz	M : S ratio = 1 : 1 ±20%
SET TRIP = 0 →outputs tripped	t_{TRIP}		<1	3	µs	
→$\overline{TRIP}$ = 0			<1	3	µs	
EPROM address to output delay	t_{ACC}			450	ns	

NOTE 2. For microprocessor interface timings, see Intel and Motorola bus timings (Tables 1 and 2).

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	10V
Voltage on any pin	V_{SS}−0·3V to V_{DD}+0·3V
Current through any I/O pin	±10mA
Storage temperature	−65°C to +125°C
Operating temperature range	0°C to +70°C

The temperature ranges quoted apply to all package types. Many package types are available and extended temperature ranges can be offered on some. Further information is available on request.

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

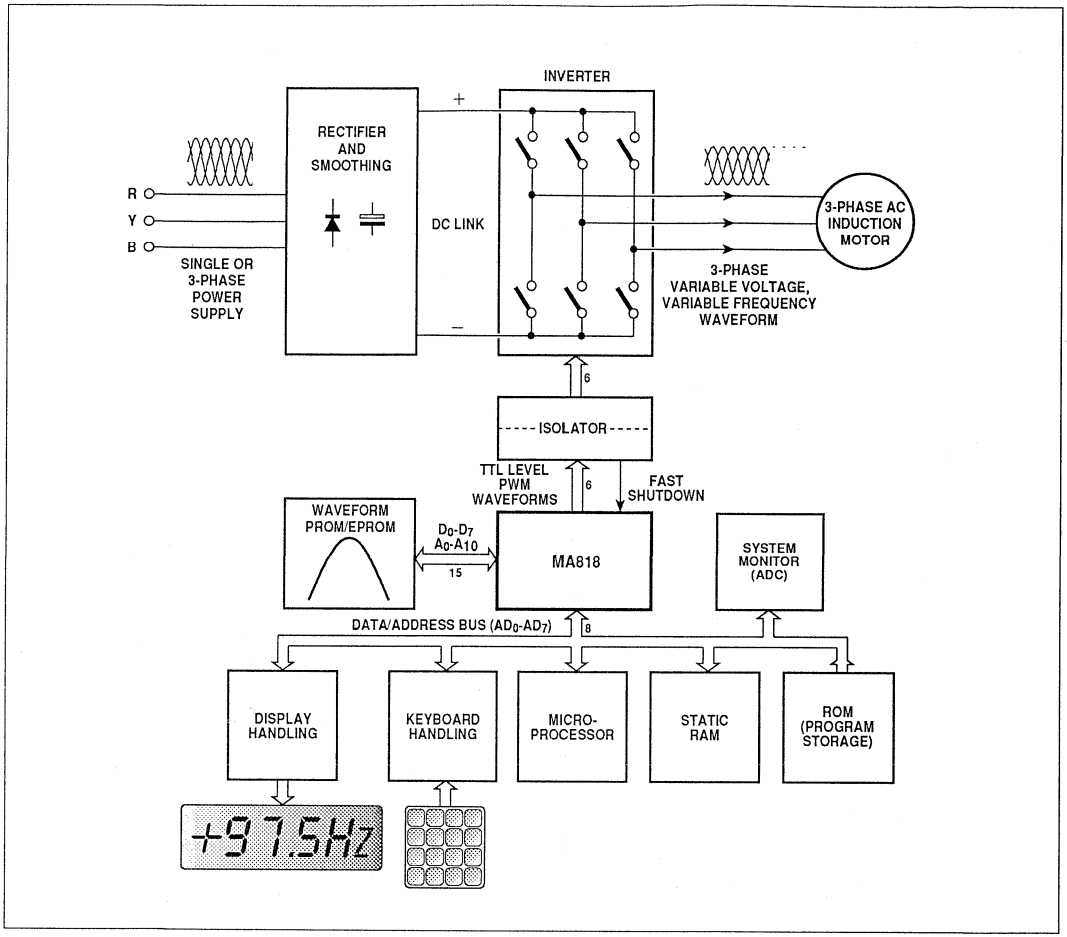


Fig. 20 A typical MA818 application

MA828 FAMILY

THREE-PHASE PULSE WIDTH MODULATION WAVEFORM GENERATOR

The MA828 PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

The six TTL level PWM outputs (Fig. 2) control the six switches in a three-phase inverter bridge. This is usually via an external isolation and amplification stage.

The MA828 is fabricated in CMOS for low power consumption.

Information contained within the pulse width modulated sequences controls the shape, power frequency, amplitude, and rotational direction (as defined by the red-yellow-blue phase sequence) of the output waveform. Parameters such as the carrier frequency, minimum pulse width, and pulse delay time may be defined during the initialisation of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in each output phase of the inverter bridge, in order to accommodate variations in the turn-on and turn-off times of families of power devices.

The MA828 is easily controlled by a microprocessor and its fully-digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral, reading the power waveform directly from an internal ROM and requiring microprocessor intervention only when operating parameters need to be changed.

An 8-bit multiplexed data bus is used to receive addresses and data from the microprocessor/controller. This is a standard MOTEL™ bus, compatible with most microprocessors/controllers.

Rotational frequency is defined to 12 bits for high accuracy and a zero setting is included in order to implement DC injection braking with no software overhead.

This family is functionally identical to the MA818 PWM generator IC except that the waveform ROM is integrated on-chip; in addition, the MA828 features three Zero Phase Pulse (ZPP) outputs and a Waveform Sampling Synchronisation output (WSS) for use as feedback in, for example, slip compensaton systems. Two standard wave shapes are available to cover most applications; in addition, any symmetrical wave shape can be integrated on-chip to order.

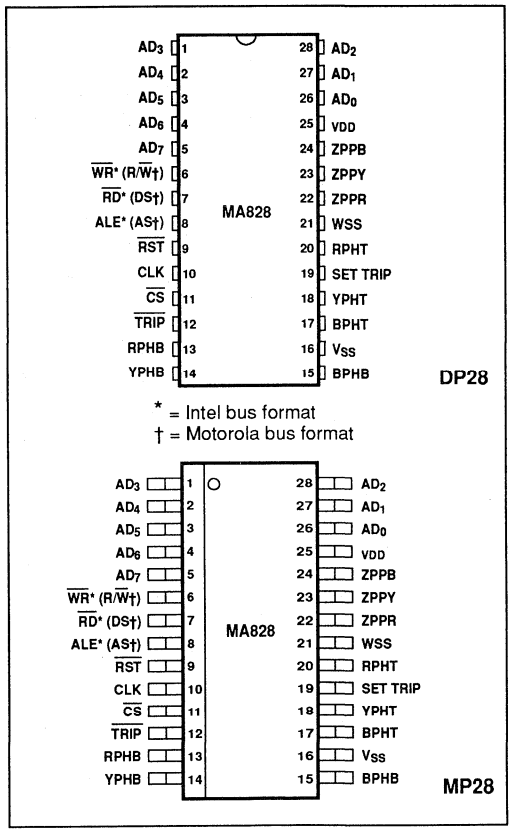


Fig. 1 Pin connections – top view (not to scale)

FEATURES

- Fully Digital Operation
- Interfaces with Most Microprocessors
- Wide Power-Frequency Range
- 12-Bit Speed Control Accuracy
- Carrier Frequency Selectable up to 24kHz
- Waveform Stored in Internal ROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- DC Injection Braking

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PIN DESCRIPTIONS

Pin No.	Name	Type	Function
26	AD_0	I	Multiplexed Address/Data (LSB)
27	AD_1	I	Multiplexed Address/Data
28	AD_2	I	Multiplexed Address/Data
1	AD_3	I	Multiplexed Address/Data
2	AD_4	I	Multiplexed Address/Data
3	AD_5	I	Multiplexed Address/Data
4	AD_6	I	Multiplexed Address/Data
5	AD_7	I	Multiplexed Address/Data(MSB)
6	Intel: $\overline{WR}$ Motorola: R/$\overline{W}$	I	Intel bus control: $\overline{\text{Write}}$ Strobe Motorola bus control: Read/$\overline{\text{Write}}$ select
7	Intel: $\overline{RD}$ Motorola: DS	I	Intel bus control: $\overline{\text{Read}}$ Strobe Motorola bus control: Data Strobe
8	Intel: ALE Motorola: AS	I	Intel bus control: Address Latch Enable Motorola bus control: Address Strobe
9	$\overline{RST}$	I	Reset internal counters, active low
10	CLK	I	Clock input
11	$\overline{CS}$	I	Chip Select input, active low
12	$\overline{TRIP}$	O	Output trip status; low = output tripped
22	ZPPR	O	Zero Phase Pulse, Red phase
23	ZPPY	O	Zero Phase Pulse, Yellow phase
24	ZPPB	O	Zero Phase Pulse, Blue phase
13	RPHB	O	Red Phase, Bottom power switch
14	YPHB	P	Yellow Phase, Bottom power switch
15	BPHB	O	Blue Phase, Bottom power switch
17	BPHT	O	Blue Phase, Top power switch
18	YPHT	O	Yellow Phase, Top power switch
20	RPHT	O	Red Phase, Top power switch
19	SET TRIP	I	Set output trip. 90kΩ internal pull-up resistor
21	WSS	O	Waveform Sampling Synchronisation
25	V_{DD}	P	Positive power supply
16	V_{SS}	P	Negative power supply (0V)

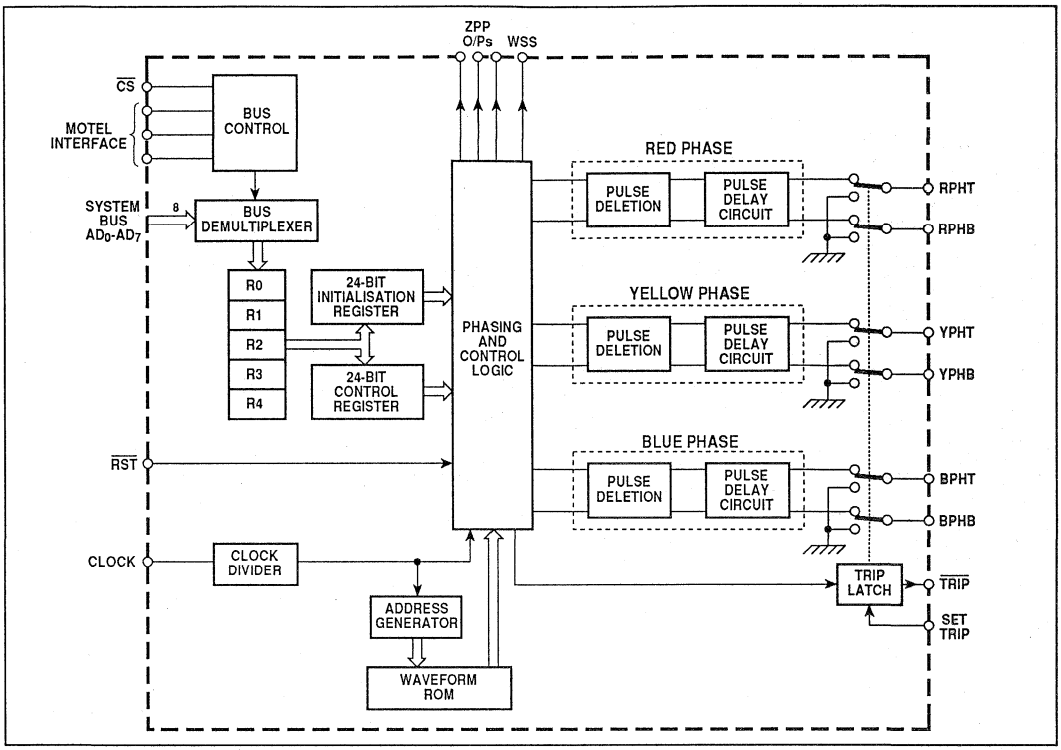


Fig. 2 MA828 internal block diagram

FUNCTIONAL DESCRIPTION

An asynchronous method of PWM generation is used with uniform or 'double-edged' regular sampling of the waveform stored in the internal ROM as illustrated in Fig. 3.

The triangle carrier wave frequency is selectable up to 24kHz (assuming the maximum clock frequency of 12.5MHz is used), enabling ultrasonic operation for noise critical applications. With 12.5MHz clock, power frequency ranges of up to 4kHz are possible, with the actual output frequency resolved to 12-bit accuracy within the chosen range in order to give precise motor speed control and smooth frequency changing. The output phase sequence of the PWM outputs can also be changed to allow both forward and reverse motor operation.

PWM output pulses can be 'tailored' to the inverter characteristics by defining the minimum allowable pulse width (the MA828 will delete all shorter pulses from the 'pure' PWM pulse train) and the pulse delay (underlap) time without the need for external circuitry. This gives cost advantages in both component savings and in allowing the same PWM circuitry to be used for control of a number of different motor drive circuits simply by changing the microprocessor software.

Powor frequency amplitude control is also provided with an overmodulation option to assist in rapid motor braking. Alternatively, braking may be implemented by setting the rotational speed to 0Hz. This is termed 'DC injection braking', in which the rotation of the motor is opposed by allowing DC to flow in the windings.

A trip input allows the PWM outputs to be shut down immediately, overriding the microprocessor control in the event of an emergency.

The Waveform Sampling Synchronisation (WSS) output may be used in conjunction with the ZPP signals to provide feedback of the actual rotational speed from the rotor. This is of particular use in slip compensated systems.

Other possible MA828 applications are as a 3-phase waveform generator as part of a switched-mode power supply (SMPS) or of an uninterruptible power supply (UPS). In such applications the high carrier frequency allows a very small switching transformer to be used.

MICROPROCESSOR INTERFACE

The MA828 interfaces to the controlling microprocessor by means of a multiplexed bus of the MOTEL format. This interface bus has the ability to adapt itself automatically to the format and timing of both MOTorola and IntEL interface buses (hence MOTEL). Internally, the detection circuitry latches the status of the DS/$\overline{RD}$ line when AS/ALE goes high. If the result is high. Then the Intel mode is used; if the result is low then the Motorola mode is used. This procedure is carried out each time that AS/ALE goes high. In practice this mode selection is transparent to the user. For bus connection and timing information refer to the description relevant to the microprocessor/controller being used.

Industry standard microprocessors such as the 8085, 8088, etc. and microcontrollers such as the 8051, 8052 and 6805 are all compatible with the interface on the MA828. This interface consists of 8 data lines, AD_0 - AD_7 (write-only in this instance), which are multiplexed to carry both the address and data information, 3 bus control lines, labelled $\overline{WR}$,$\overline{RD}$ and ALE in Intel mode and R/$\overline{W}$, DS and AS in Motorola mode, and a Chip Select input. $\overline{CS}$, which allows the MA828 to share the same bus as other microprocessor peripherals. It should be noted that all bus timings are derived from the microprocessor and are independent of the MA828 clock input.

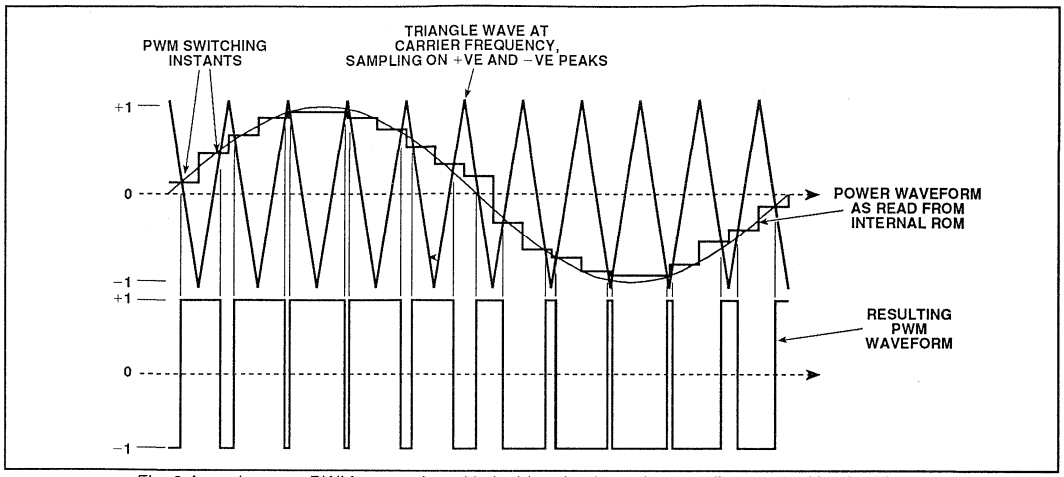


Fig. 3 Asynchronous PWM generation with'double-edged' regular sampling as used by the MA828

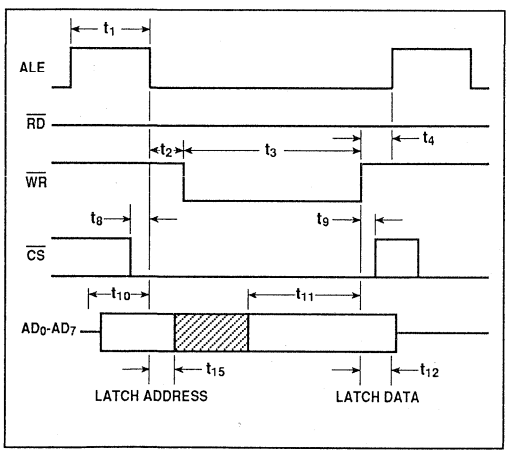


Fig. 4 Intel bus timing definitions

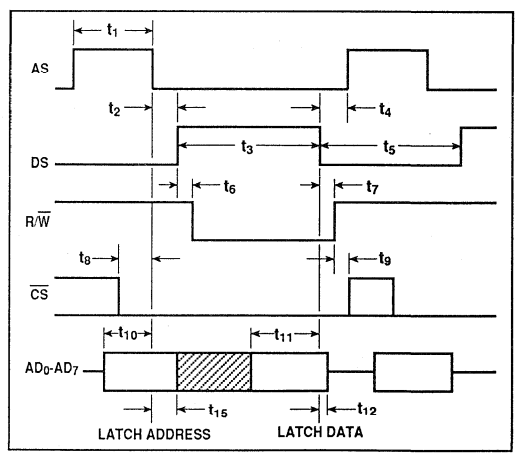


Fig. 5 Motorola bus timing definitions

Parameter	Symbol	Min.	Units
ALE high period	t_1	70	ns
Delay time, ALE to $\overline{WR}$	t_2	40	ns
$\overline{WR}$ low period	t_3	200	ns
Delay time, $\overline{WR}$ high to ALE high	t_4	40	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Data setup time	t_{11}	100	ns
Data hold time	t_{12}	30	ns

Table 1 Intel bus timings at V_{DD} = 5V, T_{AMB} = +25°C

Parameter	Symbol	Min.	Units
AS high period	t_1	90	ns
Delay time, as low to DS high	t_2	40	ns
DS high period	t_3	210	ns
Delay time, DS low to AS high	t_4	40	ns
DS low period	t_5	200	ns
DS high to R/$\overline{W}$ low setup time	t_6	10	ns
R/$\overline{W}$ hold time	t_7	10	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Write data setup time	t_{11}	110	ns
Write data hold time	t_{12}	30	ns

Table 2 Motorola bus timings at V_{DD} = 5V, T_{AMB} = +25°C

MICROPROCESSOR BUS TIMING

Intel Mode (Fig. 4 and Table 1)

The address is latched by the falling edge of ALE. Data is written from the bus into the MA828 on the rising edge of $\overline{WR}$. $\overline{RD}$ is not used in this mode because the registers in the MA828 are write only. However, this pin must be connected to $\overline{RD}$ (or tied high) to enable the MA828 to select the correct interface format.

Motorola Mode (Fig. 5 and Table 2)

The address is latched on the falling edge of the AS line. Data is written from the bus into the MA828 (only when R/$\overline{W}$ is low) on the falling edge of DS (providing $\overline{CS}$ is low).

CONTROLLLNG THE MA828

The MA828 is controlled by loading data into two 24-bit registers via the microprocessor interface. These registers are the initialisation register and the control register.

The initialisation register would normally be loaded before motor operation (i.e., prior to the PWM outputs being activated) and sets up the basic operating parameters associated with the motor and inverter. This data would not normally be updated during motor operation.

The control register is used to control the PWM outputs (and hence the motor) during operation e.g., stop/start, speed, forward/reverse etc. and would normally be loaded and changed only after the initialisation register has been loaded.

As the MOTEL bus interface is restricted to an 8-bit wide format, data to be loaded into either of the 24-bit register is first written to three 8-bit temporary registers R0, R1 and R2 before being transferred to the desired 24-bit register. The data is accepted (and acted upon) only when transferred to one of the 24-bit registers.

Transfer of data from the temporary registers to either the initialisation register or the control register is achieved by a write instruction to a dummy register. Writing to dummy register R3 results in data transfer from R0, R1 and R2 to the control register, while writing to dummy register R4 transfers data from R0, R1 and R2 to the initialisation register. It does not matter what data is written to the dummy registers R3 and R4 as they are not real registers. It is merely the write instruction to either of these registers which is acted upon in order to load the initialisation and control registers.

AD_2	AD_1	AD_0	Register	Comment
0	0	0	R0	Temporary register R0
0	0	0	R1	Temporary register R1
0	1	0	R2	Temporary register R2
0	1	0	R3	Transfers control data
1	0	1	R4	Transfers initialisation data

Table 3 MA828 register addressing

Initialisation Register Function

The 24-bit initialisation register contains parameters which, under normal operation, will be defined during the power-up sequence. These parameters are particular to the drive circuitry used, and therefore changing these parameters during a PWM cycle is not recommended. Information in this register should only be modified while $\overline{RST}$ is active (i.e. low) so that the PWM outputs are inhibited (low) during the updating process.

The parameters set in the initialisation register are as follows:

Carrier frequency

Low carrier frequencies reduce switching losses whereas high carrier frequencies increase waveform resolution and can allow ultrasonic operation.

Power frequency range

This sets the maximum power frequency that can be carried within the PWM output waveforms. This would normally be set to a value to prevent the motor system being operated outside its design parameters.

Pulse delay time ('underlap')

For each phase of the PWM cycle there are two control signals, one for the top switch connected to the positive inverter DC supply and one for the bottom switch connected to the negative inverter DC supply. In theory, the states of these two switches are always complementary. However, due to the finite and non-equal turn-on and turn- off times of power devices, it is desirable when changing the state of the output pair, to provide a short delay time during which both outputs are off in order to avoid a short circuit through the switching elements.

Pulse deletion time

A pure PWM sequence produces pulses which can vary in width between 0% and 100% of the duty cycle. Therefore, in theory, pulse widths can become infinitesimally narrow. In practice this causes problems in the power switches due to storage effects and therefore a minimum pulse width time is required. All pulses shorter than the minimum specified are deleted.

Counter reset

This facility allows the internal power frequency counter of the MA828 to be set to zero, disabling the normal frequency control and giving a 50% output duty cycle.

Initialisation Register Programming

The initialisation register data is loaded in 8-bit segments into the three 8-bit temporary registers R0-R2. When all the initialisation data has been loaded into these registers it is transferred into the 24-bit initialisation register by writing to the dummy register R4.

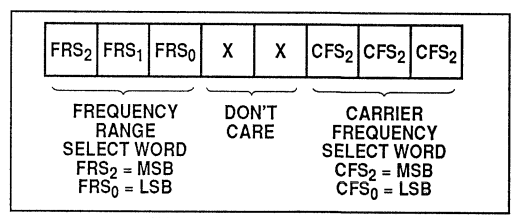


Fig. 6 Temporary register R1

Carrier frequency selection

The carrier frequency is a function of the externally applied clock frequency and a division ratio *n*, determined by the 3-bit CFS word set during initialisation. The values of *n* are selected as shown in Table 4.

CFS word	101	100	011	010	001	000
Value of n	32	16	8	4	2	1

Table 4 Values of clock division ratio n

The carrier frequency, f_{CARR}, is then given by:

$$f_{CARR} = \frac{k}{512 \times n}$$

where k = clock frequency and n = 1, 2, 4, 8, 16 or 32 (as set by CFS)

Power frequency range selection

The power frequency range selected here defines the maximum limit of the power frequency. The operating power frequency is controlled by the 12-bit Power Frequency Select (PFS) word in the control register but may not exceed the value set here.

The power frequency range is a function of the carrier waveform frequency (f_{CARR}) and a multiplication factor m, determined by the 3-bit FRS word. The value of m is determined as shown in Table 5.

FRS word	110	101	100	011	010	001	000
Value of m	64	32	16	8	4	2	1

Table 5 Values of carrier frequency multiplicaion factor m

The power frequency range, f_{RANGE}, is then given by:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

where f_{CARR} = carrier frequency and m = 1, 2, 4, 8, 16, 32 or 64 (as set by CFS).

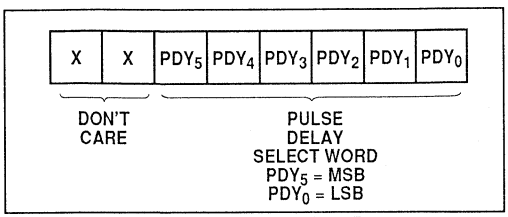


Fig. 7 Temporary register R2

Pulse delay time

The pulse delay time affects all six PWM outputs by delaying the rising edges of each of the outputs by an equal amount.

The pulse delay time is a function of the carrier waveform frequency and *pdy*, defined by the 6-bit pulse delay time select word (PDY). The value of *pdy* is selected as shown in Table 6.

PDY word	111111	111110	...etc...	000000
Value of pdy	1	2	...etc...	64

Table 6 Values of pdy

The pulse delay time, t_{pdy}, is then given by:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

where *pdy* = 1-64 (as set by PDY) and f_{CARR} = carrier frequency. Fig 8 shows the effect of the pulse delay circuit.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig. 2), the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set in the initialisation register. The actual shortest pulse generated is given by $t_{pd} - t_{pdy}$.

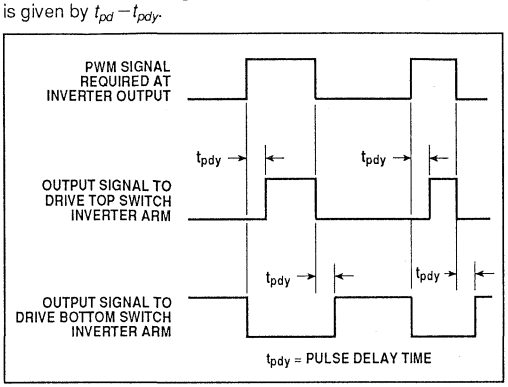


Fig. 8 Effect of pulse delay on PWM pulse train

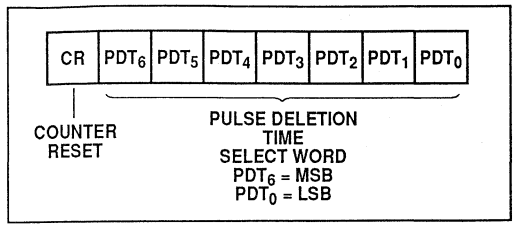


Fig. 9 Temporary register R0

Pulse deletion time

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the initialisation register. If a pulse (either positive or negative) is greater than or equal in duration to the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, t_{pd}, is a function of the carrier wave frequency and *pdt*, defined by the 7-bit pulse deletion time word (PDT). The value of *pdt* is selected as shown in Table 7.

PDT word	1111111	1111110	...etc...	0000000
Value of pdt	1	2	...etc...	128

Table 7 Values of pdt

The pulse deletion time, t_{pd}, is then given by:

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

where *pdt* = 1-128 (as set by PDT) and f_{CARR} = carrier frequency.

Fig. 10 shows the effect of pulse deletion on a pure PWM waveform.

Counter reset

When the CR bit is active (i.e., low) the internal power frequency phase counter is set to 0 degrees for the red phase. The power frequency is then set to 0Hz and cannot be changed via the normal frequency control.

Control Register Function

This 24-bit register contains the parameters that would normally be modified during PWM cycles in order to control the operation of the motor.

The parameters set in the control register are as follows:

Power frequency (speed)

Allows the power frequency of the PWM outputs to be adjusted within the range specified in the initialisation register

Forward/reverse

Allows the direction of rotation of the AC motor to be changed by changing the phase sequence of the PWM outputs.

Power frequency amplitude

By altering the widths of the PWM output pulses while maintaining their relative widths, the amplitude of the power waveform is effectively altered whilst maintaining the same power frequency.

Overmodulation

Allows the output waveform amplitude to be doubled so that a quasi-squarewave is produced. A combination of overmodulation and a lower power frequency can be used to achieve rapid braking in AC motors.

Output inhibit

Allows the outputs to be set to the low state while the PWM generation continues internally. Useful for temporarily inhibiting the outputs without having to to change other register contents.

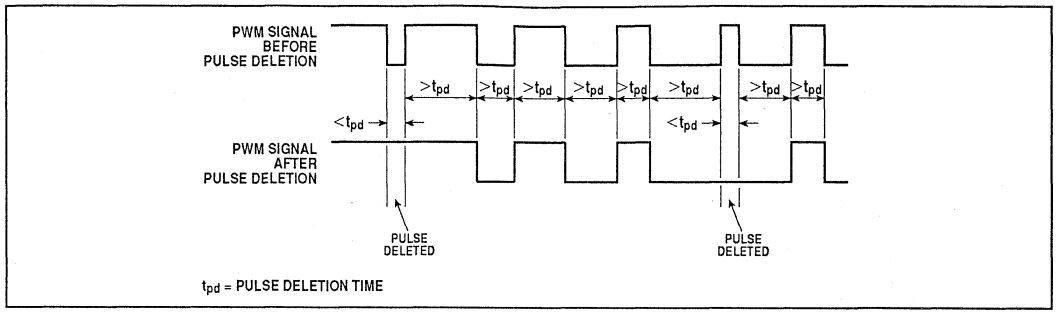


Fig. 10 The effect of the pulse deletion circuit

Control Register Programming

The control register should only be programmed once the initialisation register contains the basic operating parameters of the MA828.

As with the initialisation register, control register data is loaded into the three 8-bit temporary registers R0 - R2. When all the data has been loaded into these registers it is transferred into the 24-bit control register by writing to the dummy register R3. It is recommended that all three temporary registers are updated before writing to R3 in order to ensure that a conformal set of data is transferred to the control register for execution.

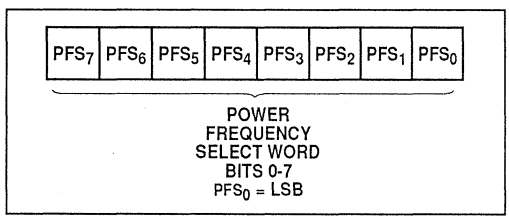


Fig. 11 Temporary register R0

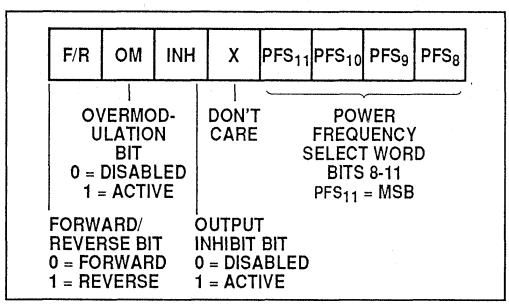


Fig. 12 Temporary register R1

Power frequency selection

The power frequency is selected as a proportion of the power frequency range (defined in the initialisation register) by the 12-bit power frequency select word, PFS, allowing the power frequency to be defined in 4096 equal steps. As the PFS word spans the two temporary registers R0 and R1 it is therefore essential, when changing the power frequency, that both these registers are updated before writing to R3.

The power frequency (f_{POWER}) is given by:

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

where *pfs* = decimal value of the 12-bit PFS word and f_{RANGE} = power frequency range set in the initialisation register.

Output inhibit selection

When active (i.e., low) the output inhibit bit INH sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When the inhibit is released the PWM outputs continue immediately. Note that as the inhibit is asserted after the pulse deletion and pulse delay circuits, pulses shorter than the normal minimum pulse width may be produced initially.

Overmodulation selection

The overmodulation bit OM is, in effect, the ninth bit (MSB) of the amplitude word. When active (i.e., high) the output waveform will be controlled in the 100% to 200% range by the amplitude word.

The percentage amplitude control is now given by:

$$\text{Overmodulated Amplitude} = A_{POWER} \times 100\%$$

where A_{POWER} = the power amplitude

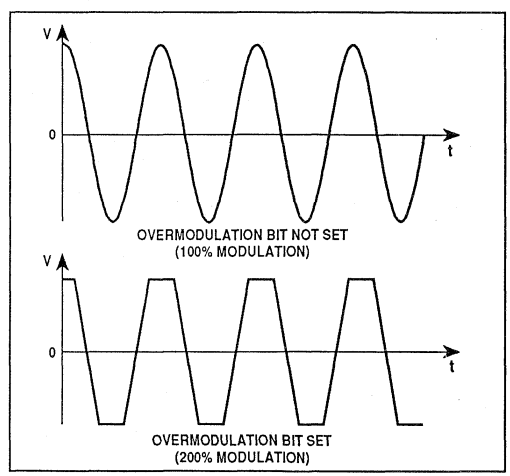


Fig. 13 Voltage waveforms as seen at the motor terminals, showing the effect of setting the overmodulation bit

Forward/ reverse selection

The phase sequence of the three-phase PWM output waveforms is controlled by the Forward/Reverse bit F/R. The actual effect of changing this bit from 0 (forward) to 1 (reverse) is to reverse the power frequency phase counter from incrementing the phase angle to decrementing it. The required output waveforms are all continuous with time during a forward/ reverse change.

In the forward mode the output phase sequence is red-yellow-blue and in the reverse mode the sequence is blue-yellow-red.

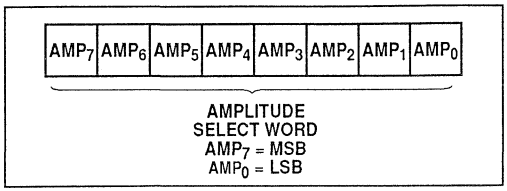


Fig.14 Temporary register R2

Amplitude selection

The power waveform amplitude is determined by scaling the amplitude of the waveform samples stored in the ROM by the value of the 8-bit amplitude select word (AMP).

The percentage amplitude control is given by:

$$\text{Power Amplitude, } A_{POWER} = \frac{A}{225} \times 100\%$$

where A = decimal value of AMP.

POWER-UP CONDITIONS

All bits in both the Initialisation and Control registers power-up in the low state. This means that Counter Reset ($\overline{CR}$) is active and a 50% duty cycle will be output from all PWM outputs until further initialising action is taken. Holding $\overline{RST}$ low or using the SET TRIP input will ensure that the PWM outputs remain inactive (i.e., low) during this period.

MA828 PROGRAMMING EXAMPLE

The following example assumes that a master clock of 12·288 MHz is used (12·288 MHz crystals are readily available). This clock frequency will allow a maximum carrier frequency of 24 kHz and a maximum power frequency of 4 kHz.

Initialisation Register Programming Example

A power waveform range of up to 250Hz is required with a carrier frequency of 6kHz, a pulse deletion time of 10µs and an underlap of 5µs.

1. Setting the carrier frequency

The carrier frequency should be set first as the power frequency, pulse deletion time and pulse delay time are all defined relative to the carrier frequency.

We must calculate the value of n that will give the required carrier frequency:

$$f_{CARR} = \frac{k}{512 \times n}$$

$$\Rightarrow \mathbf{n} = \frac{k}{512 \times f_{CARR}} = \frac{12{\cdot}288 \times 10^6}{512 \times 6 \times 10^3} = \mathbf{4}$$

From Table 4, n = 4 corresponds to a 3-bit CFS word of 010 in temporary register R1.

2. Setting the power frequency range

We must calculate the value of m that will give the required power frequency:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

$$\Rightarrow \mathbf{m} = \frac{f_{RANGE} \times 384}{f_{CARR}} = \frac{250 \times 384}{6 \times 10^3} = \mathbf{16}$$

From Table 5, m = 16 corresponds to a 3-bit FRS word of 100 in temporary register R1.

3. Setting the pulse delay time

As the pulse delay time affects the actual minimum pulse width seen at the PWM outputs, it is sensible to set the pulse delay time before the pulse deletion time, so that the effect of the pulse delay time can be allowed for when setting the pulse deletion time.

We must calculate the value of *pdy* that will give the required pulse delay time:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdy} = t_{pdy} \times f_{CARR} \times 512$$

$$= 5 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{15{\cdot}4}$$

However, the value of *pdy* must be an integer. As the purpose of the pulse delay is to prevent 'shoot-through' (where both top and bottom arms of the inverter are on simultaneously), it is sensible to round the pulse delay time up to a higher, rather than a lower figure.

Thus, if we assign the value 16 to *pdy* this gives a delay time of 5·2µs. From Table 6, *pdy* = 16 corresponds to a 6-bit PDY word of 110000 in temporary register R2.

4. Setting the pulse deletion time

In setting the pulse deletion time (i.e., the minimum pulse width) account must be taken of the pulse delay time, as the actual minimum pulse width seen at the PWM outputs is equal to $t_{pd} - t_{pdy}$.

Therefore, the value of the pulse deletion time must, in this instance, be set 5·2µs longer than the minimum pulse length required

Minimum pulse length required = 10µs

∴ tPD to be set to 10µs+5·2µs = 15·2µs

Now,

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdt} = f_{pd} \times f_{CARR} \times 512$$

$$= 15{\cdot}2 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{46{\cdot}7}$$

Again, *pdt* must be an integer and so must be either rounded up or down – the choice of which will depend on the application. Assuming we choose in this case the value 46 for *pdt*, this gives a value of t_{pd} of 15 µs and an actual minimum pulse width of 15−5·2µs = 9·8µs.

From Table 7, *pdt* = 46 corresponds to a value of PDT, the 7-bit word in temporary register R0 of 1010010.

The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the initialisation register) in order to achieve the parameters in the example given, is shown in Fig. 15.

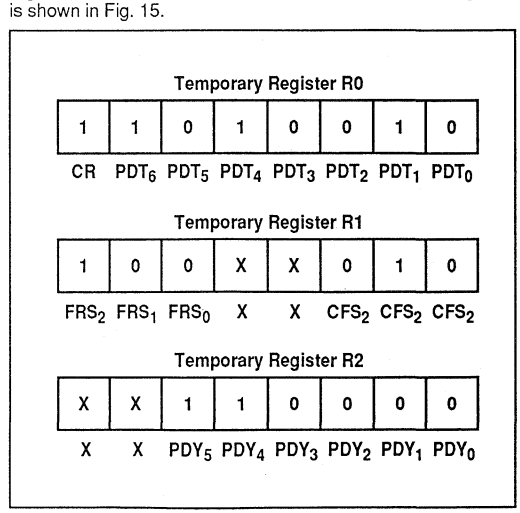


Fig. 15

Control Register Programming Example

The control register would normally be updated many times while the motor is running, but just one example is given here. It is assumed that the initialisation register has already heen programmed with the parameters given in the previous example.

A power waveform of 100Hz is required with a PWM waveform amplitude of 80% of that stored in the ROM. The phase sequence should be set to give forward motor rotation. The outputs should be enabled and no overmodulation is required.

1. Setting the power frequency

The power frequency, f_{POWER}, can be selected to 12-bit accuracy (i.e 4096 equal steps) from 0Hz to f_{RANGE} as defined in the initialisation register. In this case, with f_{RANGE} = 250Hz, the power frequency can be adjusted in increments of 0·06Hz.

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

$$\Rightarrow \mathbf{pfs} = \frac{f_{POWER} \times 4096}{f_{RANGE}} = \frac{100 \times 4096}{250} = \mathbf{1638{\cdot}4}$$

We can only have *pfs* as an integer, so if we assign *pfs* = 1638 this gives f_{POWER} = 99.97 Hz. The 12-bit binary equivalent of this value gives a PFS word of 011001100110 in temporary registers R0 and R1.

2. Setting overmodulation, forward/reverse, output inhibit

Overmodulation is not required therefore OM = 0.

Forward motor control is required (i.e., the phase sequence of the PWM outputs should be red-yellow-blue) therefore forward/reverse bit F/R = 0.

Output inhibit should be inactive (i e., the outputs should be active), therefore INH= 1.

These bits are all set in temporary register R1.

3. Setting the power waveform amplitude

$$A_{POWER} = \frac{A}{225} \times 100\%$$

$$\Rightarrow \mathbf{A} = \frac{A_{POWER} \times 255}{100} = \frac{80 \times 255}{100} = \mathbf{204}$$

The 8-bit binary equivalent of this value gives an AMP word of 11001100 in temporary register R2. The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the control register) in order to achieve the parameters in the example given, is shown in Fig. 16.

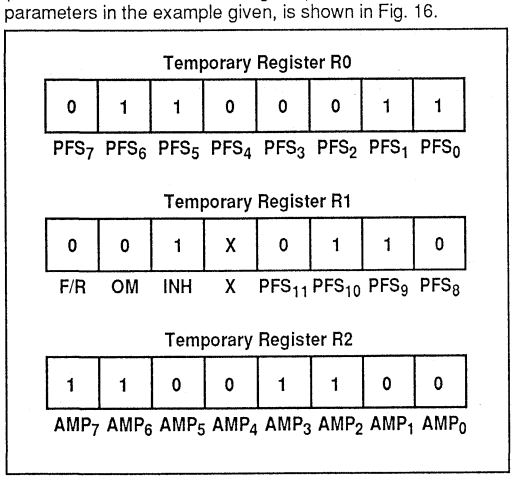


Fig. 16

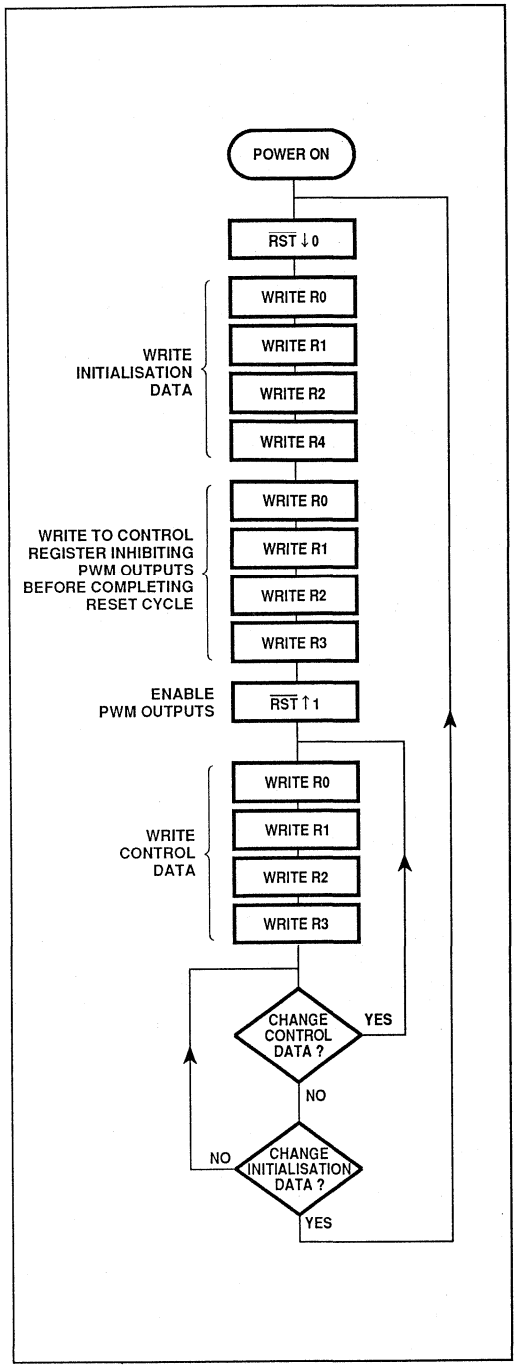


Fig. 17 Typical MA828 programming routine

HARDWARE INPUT/OUTPUT FUNCTIONS

Set Output Trip (SET TRIP input)

The SET TRIP input is provided separately from the microprocessor interface in order to allow an external source to override the microprocessor and provide a rapid shutdown facility. For example, logic signals from overcurrent sensing circuitry or the microprocessor 'watchdog' might be used to activate this input.

When the SET TRIP input is taken to a logic high, the output trip latch is activated. This results in the $\overline{\text{TRIP}}$ output and the six PWM outputs being latched low immediately. This condition can only be cleared by applying a reset cycle to the $\overline{\text{RST}}$ input.

It is essential that when not in use SET TRIP is tied low and isolated from potential sources of noise; on no account should it be left floating.

SET TRIP is latched internally at the master clock rate in order to reduce noise sensitivity.

Output Trip Status ($\overline{\text{TRIP}}$ output)

The $\overline{\text{TRIP}}$ output indicates the status of the output trip latch and is active low.

Reset ($\overline{\text{RST}}$ input)

The $\overline{\text{RST}}$ input performs the following functions when activbe (low):

1. All PWM outputs are forced low (if not already low) thereby turning off the drive switches.
2. All internal counters are reset to zero (this corresponds to 0° for the red phase output).
3. The rising edge of $\overline{\text{RST}}$ reactivates the PWM outputs resetting the output trip and setting the $\overline{\text{TRIP}}$ output high – assuming that the SET TRIP input is inactive (i.e. low).

Zero Phase Pulses (ZPPR, ZPPY and ZPPB outputs)

The zero phase pulse outputs provide pulses at the same frequency as the power frequency with a 1 : 2 mark-space ratio. When in the forward mode of operation the falling edge of ZPPR corresponds to 0° for the red phase, the falling edge of ZPPY to 0° for the yellow phase and the ZPPB falling edge to 0° for the blue phase. In the reverse mode, the rising edge of a zero phase pulse corresponds to 0° for the relevant phase PWM output.

Waveform Sampling Synchronisation (WSS output)

This output provides a square wave signal of 50% duty cycle at a frequency 1536 times higher than the fundamental of the power waveform. Each successive pulse of WSS corresponds to the MA828 reading the next location of the waveform ROM. It may be used in conjunction with the ZPP signals to monitor the position of the machine rotor and may form part of a closed loop control system such as slip compensation.

Clock (CLK input)

The CLK input provides a timing reference used by the MA828 for all timings related to the PWM outputs. The microprocessor interface, however, derives all its timings from the microprocessor and therefore the microprocessor and the MA828 may be run either from the same or from different clocks.

WAVEFORM DEFINITION

The waveform amplitude data used to construct the PWM output sequences is read from the internal 384×8 ROM. This contains the 90° span of the waveform as shown in Fig. 18. Each successive 8-bit sample linearly represents the instantaneous amplitude of the waveform. It is assumed that the waveform is symmetrical about the 9o°, 180° and 270° axes. The MA828 reconstructs the full 360° waveform by reading the 0°-90° section held in ROM and assigning negative values for the second half of the cycle.

These samples are used to calculate the instantaneous amplitudes for all three phases, which will be 120° transposed in the normal R-Y-B orientation for forward rotation or B-Y-R for reverse rotation. The 384 8-bit samples are regularly spaced over the 0° to 90° span, giving an angular resolution of approximately 0·23°.

Waveform segment	Sample number
0°- 30°	0 - 127
30·23°- 60°	128 - 255
60·23°- 89·77°	256 - 383

Table 8 90° of the 360° cycle is divided into 384 8-bit samples

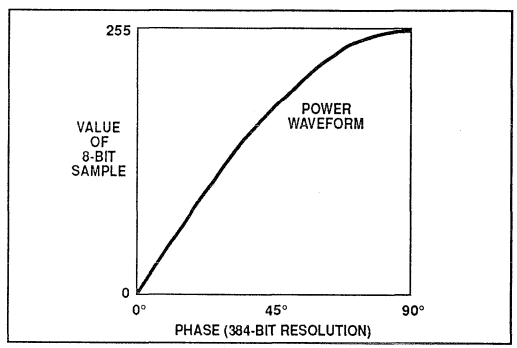


Fig. 18 90° sample of typical power waveform

PRODUCT DESIGNATION

Two standard option exist, defining waveform shape. These are designated MA828-1 and MA828-2 as follows:

MA828-1

Sine+third harmonic at one-sixth the amplitude of the fundamental:

$$x(t) = A\,[sin\,(\omega t) + \frac{1}{6} sin\,3(\omega t)]$$

MA828-2

Pure sinewave:

$$x(t) = A\,[sin\,(\omega t)]$$

Additional wave shapes can be implemented to order, provided they are symmetrical about the 90°, 180° and 270° axes. Contact your local GEC Plessey Semiconductors Customer Service Centre for further details.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

V_{DD} = +5V±5%, T_{AMB} = +25°C

DC Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input high voltage	V_{IH}	2			V	
Input low voltage	V_{IL}			0·8	V	
Input leakage current	I_{IN}			10	μA	$V_{IN} = V_{SS}$ or V_{DD}
Output high voltage	V_{OH}	4·0	>4·5		V	I_{OH} = −4mA
Output low voltage	V_{OL}		<0·2	0·4	V	I_{OL} = 4mA
Supply current (static)	$I_{DD\ (static)}$			100	μA	All outputs open circuit
Supply current (dynamic)	$I_{DD\ (dynamic)}$		<10	20	mA	f_{CLK} = 10MHz
Supply voltage	V_{DD}	4·75	5·0	7·5	V	

AC Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Clock frequency	f_{CLK}			12·5	MHz	M : S ratio = 1 : 1 ±20%
SET TRIP = 0 → outputs tripped	t_{TRIP}		$2/f_{CLK}$	$3/f_{CLK}$	μs	f_{CLK} in MHz
→ $\overline{TRIP}$ = 0			$2/f_{CLK}$	$3/f_{CLK}$	μs	f_{CLK} in MHz

NOTE 1. For microprocessor interface timings, see Intel and Motorola bus timings (Tables 1 and 2).

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	10V
Voltage on any pin	V_{SS}−0·3V to V_{DD}+0·3V
Current through any I/O pin	±10mA
Storage temperature	−65°C to +125°C
Operating temperature range	0°C to +70°C

The temperature ranges quoted apply to all package types. Many package types are available and extended temperature ranges can be offered for some. Further information is available on request.

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

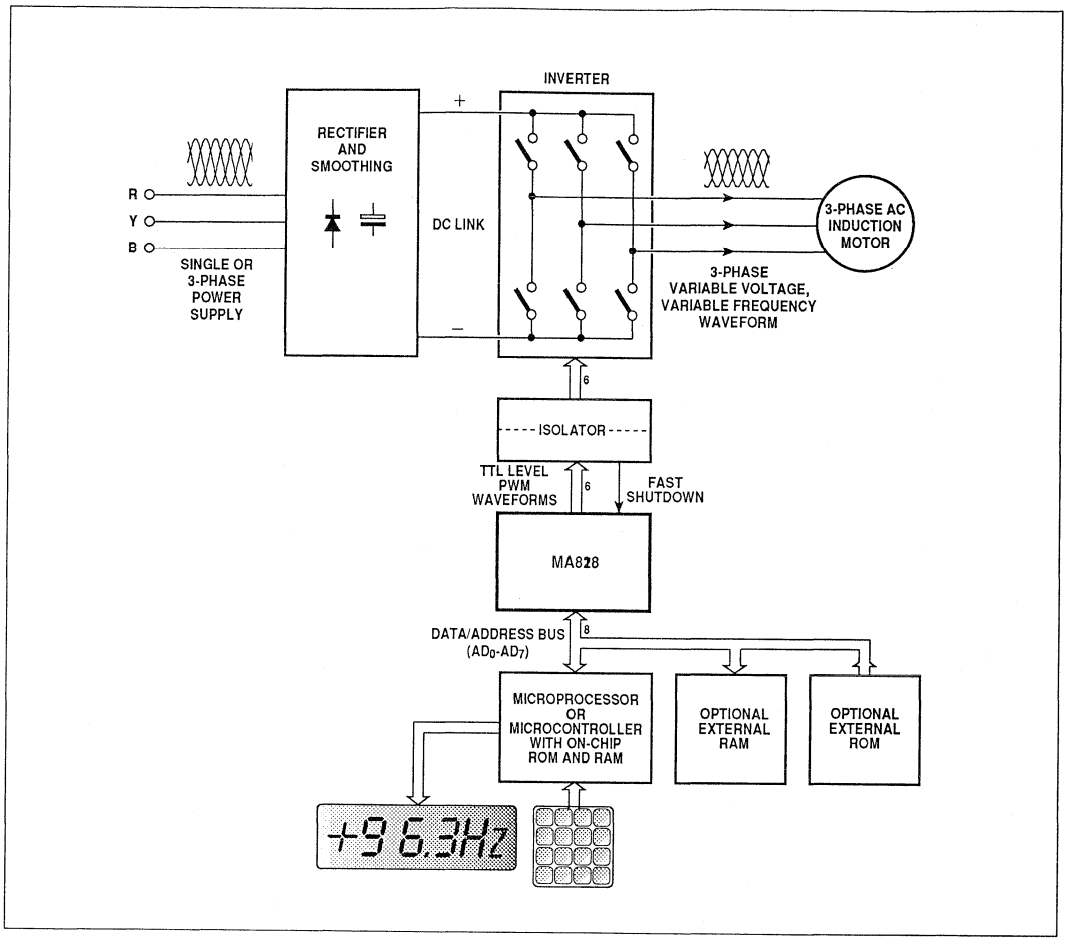


Fig. 19 A typical MA828 application

MA838 FAMILY

SINGLE PHASE PULSE WIDTH MODULATION WAVEFORM GENERATOR

The MA838 PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

Two TTL level PWM outputs control the upper and lower switches in an inverter arm. This is usually via an external isolation and amplification stage.

Information contained within the pulse width modulated sequences controls the shape, power frequency and amplitude of the output waveform. Parameters such as the carrier frequency, minimum pulse width, and pulse delay time may be defined during the initialisation of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in each output phase of the inverter bridge, in order to accommodate variations in the turn-on and turn-off times of families of power devices.

The MA838 is easily controlled by a microprocessor and its fully-digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral, reading the power waveform directly from an internal ROM and requiring microprocessor intervention only when operating parameters need to be changed.

An 8-bit multiplexed data bus is used to receive addresses and data from the microprocessor/controller. This is a standard MOTEL™ bus, compatible with most microprocessors/controllers.

The MA838 is fabricated in CMOS for low power consumption.

FEATURES

- Fully Digital Operation
- Interfaces with Most Microprocessors
- Wide Power-Frequency Range
- 12-Bit Speed Control Accuracy
- Carrier Frequency Selectable up to 24kHz
- Waveform Stored in Internal ROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- DC Injection Braking

MOTEL is a registered Trademark of Intel Corp. and Motorola Corp.

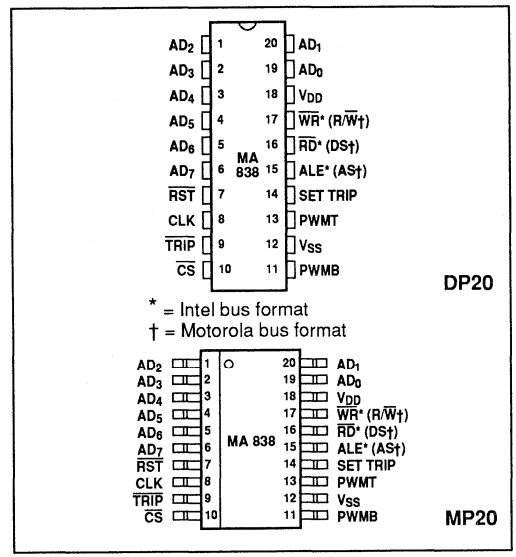


Fig. 1 Pin connections – top view (not to scale)

Rotational frequency is defined to 12 bits for high accuracy and a zero setting is included in order to implement DC injection braking with no software overhead.

This family is functionally similar to the MA828 PWM generator IC, with the following differences:

1. Package and pinout.
2. There are no ZPP outputs.
3. The Forard/Reverse control register bit is 'don't care'.
4. There are only two PWM outputs, PWMT and PWMB.
5. There is no WSS output.

Two standard wave shapes are available to cover most applications.

MA838-1
Sine plus third harmonic at one sixth the fundamental amplitude (for Drive Systems).

MA838-2
Pure sinewave (for Waveform Generation).

In addition, any symmetrical waveshape may be integrated on-chip, to order. More detailed information on the MA838 may be obtained by referring to the MA828 data sheet.

Section 8
Power Control

GEC PLESSEY
SEMICONDUCTORS

SL441C

ZERO VOLTAGE SWITCH

The SL441C is a symmetrical burst control integrated circuit in an 8 pin DIL package. When used with a triac, AC power may be regulated by varying the number of mains cycles applied to the load in a fixed timing period. The device is especially suited to room temperature control applications including panel heaters, fan heaters etc. Zero Voltage Switching has the advantage of minimising radio frequency interference.

FEATURES

- Balanced zero voltage point crossing detector, spike filter and pulse generator for reliable triggering of the triac.
- A period pulse generator and bistable which are arranged to provide symmetrical burst control and eliminate $^1/_2$ wave firing. (EN50.006 BS5406,1976)
- A ramp generator whose output is used to modify an internal reference voltage which is then compared with the voltage appearing on the thermistor to form a proportional control system. The period of the ramp generator is defined externally and may be chosen to limit 'lamp flicker' in accordance with EN50.006/BS5406, 1976.

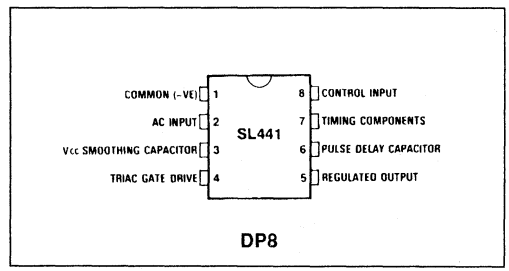


Fig.1 Pin Connections (top view)

- The comparison amplifier has inbuilt hysteresis to eliminate switching jitter and a spike filter/ sampling circuit to provide high immunity to both spikes and coherent 50Hz/60Hz.
- Thermistor malfunction may be sensed and power automatically removed.
- A supply voltage sensing circuit which inhibits firing pulses when the supply is inadequate to guarantee proper circuit operation. This eliminates stressing of the triac at switch-on.

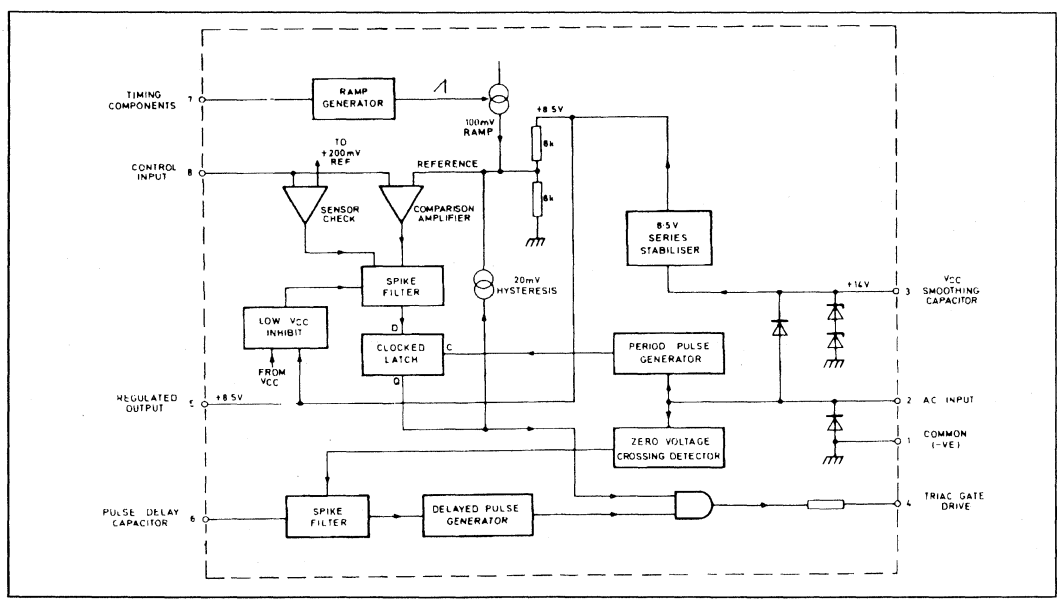


Fig. 2 Block Schematic of SL441C

ELECTRICAL CHARACTERISTICS

These Characteristics are guaranteed at the following temperatures (unless otherwise stated).
T_{amb} = +25°C
All voltages measured with respect to common (pin 1)

Characteristics	Min	Typ	Max	Units
Shunt regulating voltage pin 3 @ 16mA		14.7		V
Shunt regulating voltage pin 3 @ 16mA @ 75°C			16	V
Supply voltage trip level pin 3		12.2		V
Supply current (less I_4AV, I_5) (see Note 1)			7.5	mA
Regulated voltage pin 5	8.0	8.5	9.0	V
Regulated voltage temperature coefficient pin 5	-1		+1	mV/ °C
Triac gate drive pin 4 (see Note 2)				
Open circuit ON voltage		8.5		V
Open circuit OFF voltage			0.1	V
Output current into 2V drain	100	130		mA
Output current into 4V drain	65	80		mA
Output current into short circuit			200	mA
Internal drain resistance		800		Ω
Control input pin 8				
Bias current			1	µA
Hysteresis		20		mV
Sensor malfunction circuit operates at	150	200	250	mV
Input working voltage range	0		12	V
Internal reference voltage (Ramp start) (see Note 3)	4.0	4.25	4.5	V
Internal reference voltage (Ramp finish) (see Note 3)		4.35		V
Peak-to-peak amplitude of ramp	70	100	130	mV
Pin 6 output impedance (R6) (see Note 2)	21.5	27	32.5	kΩ
Maximum ripple voltage pin 3			1	V_{P-P}

NOTES
1. The supply current is 0.45 x (RMS current fed into pin 2). I_5 is the current drained from pin 5 externally. I_{4AV} is the average triac gate current supplied each mains cycle.
2. Triac firing pulse. t_p Pulse width = 0.69 $R6C_D$ microseconds typical
   t_f Pulse finish = 1.09 $R6C_D$ microseconds minimum after zero voltage point R6 in kohms. C_D in nF.
   See Application circuit
   t_p Nominal (C_D = 2.7nF) = 50 microseconds
   t_p Minimum (C_D = 2.7nF) = 63 microseconds
3. Ramp period = 0.85 ± 0.15 x R_TC_T sec. See Application circuit. The actual value of R_t must lie between 500kohms and 3Mohms.

ABSOLUTE MAXIMUM RATINGS

VOLTAGES
Voltage on pin V_8 - I Max. 12V
Voltage on pin V_4 - I Max. 10V

TEMPERATURE
Operating ambient temperature T_{AMB} -10°C to +75°C
Storage temperature T_{STG} -55°C to +150°C

CURRENTS
Supply current (pin 2) Peak value ± I_2M 50mA.
Non-repetitive peak current (tp ≤250µs) ±I_2SM 200mA.
Output current (pin 5) Max. 5mA Short circuit protected.
Output current (pin 4) average value I_4 (AV) Max 5mA Short circuit protected

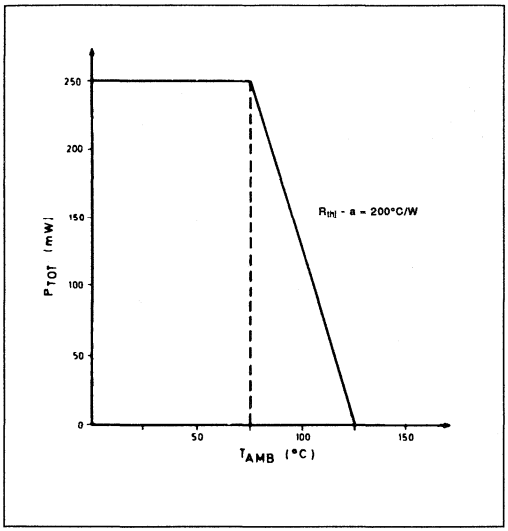


Fig. 3 Power Dissipation

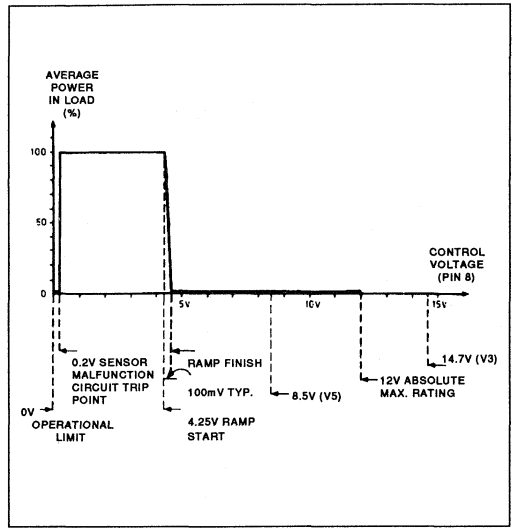


Fig. 4 Control Characteristic of Pin 8

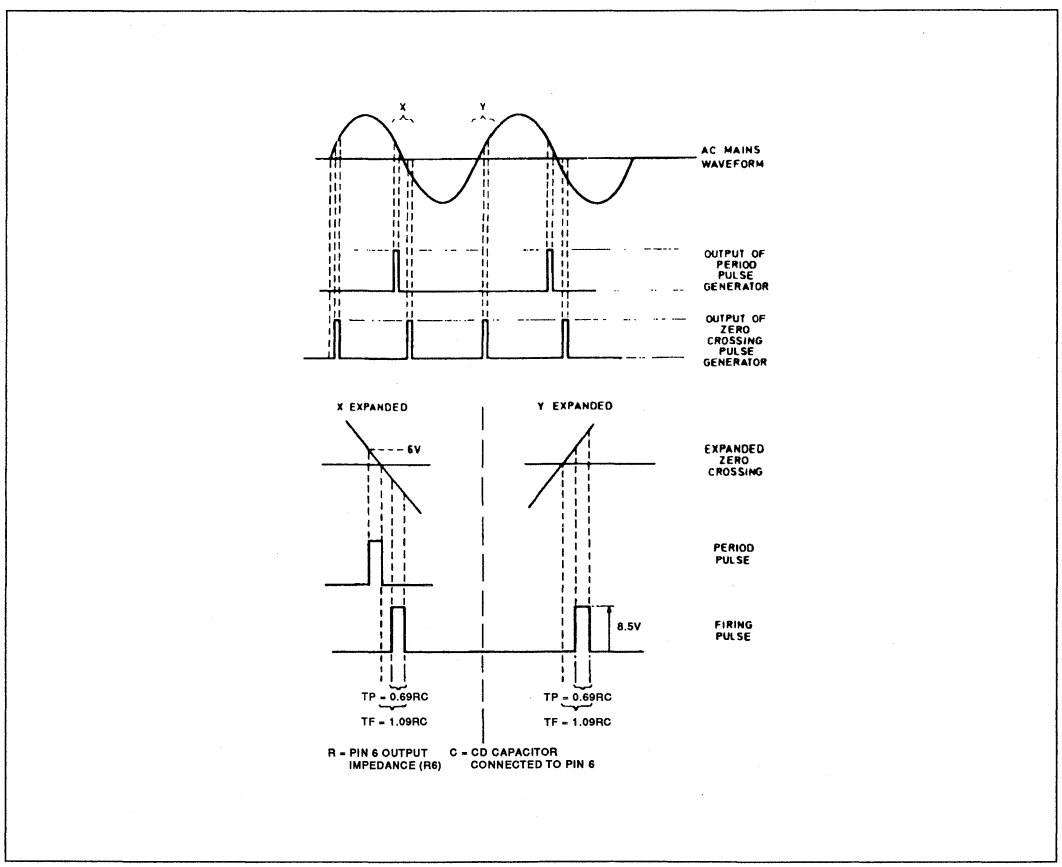


Fig. 5 Pulse Timing

TDA2088

PHASE CONTROL INTEGRATED CIRCUIT FOR CURRENT FEEDBACK APPLICATIONS

The TDA2088 is a bipolar integrated circuit phase controller, optimised for use in current feedback applications. It can also be used in open loop mode. The circuit was primarily designed for motor speed control in applications such as power tools and domestic appliances (foodmixers etc.).

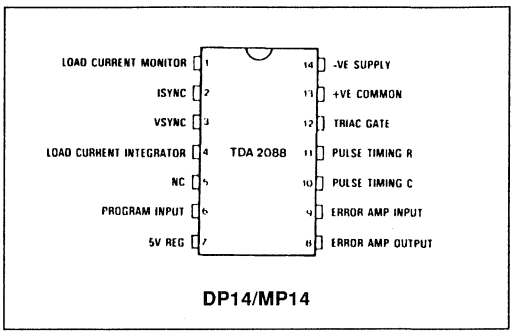


Fig.1 Pin Connections (top view)

FEATURES

- Powered direct from AC Mains or DC line.
- -5V supply avallablc for ancillary circuitry.
- Low supply current consumptlon.
- Negative triac firing pulses.
- Guaranteed minimum 100mA trlac drive current.
- Well-deflned control voltage/phase angle relationshlp.
- Speed compensated by sensing motor current.
- Simple optimisation of control loop parameters.

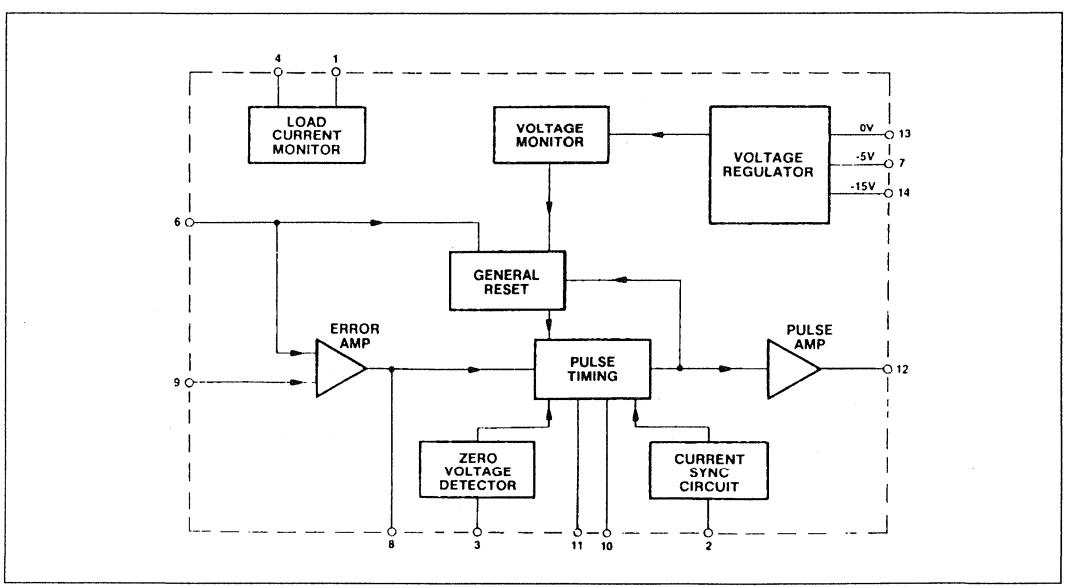


Fig. 2 Block Diagram of TDA2088

ELECTRICAL CHARACTERISTICS

These Characteristics are guaranteed at the following temperatures (unless otherwise stated).
T_{amb} = +25°C
All potentials measured with respect to common (Pin 13) (unless otherwise stated).

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
CURRENT CONSUMPTION					
Pin 14					
IC operating current		2.8	3.8	mA	Includes triac gate current for 50µs pulse
SHUNT VOLTAGE REGULATOR					
Pin 14					
Regulating voltage	-16	-14.75	-13.5	V	Full temperature range
Voltage monitor enable level	-11		-9	V	
SERIES REGULATOR					
Pin 7					
Regulating voltage (Vreg)	-5.35	-5	-4.65	V	1mA external load
Temperature coefficient			±1	mV/°C	
External load			10	mA	
Regulation	-75		+75	mV	For 0-5mA external load change
SPEED PROGRAM INPUT					
Pin 6					
Input voltage range	Vreg -0.5		0	V	
Input bias current			1	µA	
Zero power demand voltage	-100	-75	-50	mV	
ERROR AMPLIFIER					
Pin 6, 8 and 9					
Input offset voltage	-5		+15	mV	$V_6 - V_9$ to give $I_8 = 0$
Transconductance	80	100	120	µA/V	
Pin 8					
Output current drive	±20		±35	µA	
FIRING PULSE TIMING					
Pin 3					
Voltage SYNC trip level	±35	±50	±65	µA	
Pin 2					
Current SYNC trip level	±35	±50	±65	µA	
Pin 8					
Phase control voltage swing	Vreg		0	V	
Pin 10					
Firing pulse width		50		µs	C pin 16 = 47nF
Pulse repetition time		100		µs	C pin 16 = 47nF, R pin 11 = 200k
FIRING PULSE OUTPUT					
Pin 12					
Drive current	100	125	150	mA	Pin 12 V = -3V
Leakage current			10	µA	Pin 12 V = 0V
LOAD CURRENT SENSING					
Pin 1					
Offset voltage		±20	mV		
Pin 1 and 4					
Current gain	0.475	0.5	0.525		Pin 1 current = 100µA

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL	Value	Units
Triac gate voltage pin 12	4	V
Repetitive peak input current pin 14	80	mA
Non repetitive peak input current pin 14 (tp = 250µs)	200	mA
Non repetitive peak input current pin 1 negative half cycle (tp = 250µs)	200	mA
Peak input current (I_{SYNC}) pin 2	±1	mA
Peak input current (V_{SYNC}) pin 3	±1	mA
-5V regulator current pin 7	10	mA
Control amp input voltage pin 9	Vreg	V
THERMAL		
Operating ambient temperature	0 to +85	°C
Storage temperature	-55 to +150	°C

SPECIAL FEATURES

Low Supply Current Consumption

Due to the low current consumption of the device the power dissipation in the mains dropper resistor may be as low as 1.1W on a 220V AC supply (0.5W on 110V).

By incorporating both a shunt and a series voltage regulator in the IC desion, a high ripple voltage can be accommodated on the supply smoothing capacitor.

The combination of the above two features result in reduced size and a minimum count of components used in the power supply circuitry.

Powered Direct from AC Mains or DC Line

This device incorporates a shunt regulator (-15V) such that it may be powered from an AC or DC supply via current limiting components or the device may be powered direct from a -12V DC supply.

-5V Supply available for Ancillary Circuitry

A -5V series regulator is incorporated to provide a smooth supply for the internal analog control functions. This supply may be used externally to power ancillary circuitry such as timing circuits and other logic control circuits etc. as well as driving potentiometers for the analog control inputs.

Due to this supply technique, greater symmetry between positive and negative half cycle firing phase angle will result.

Low Supply Inhibit Circuit

Timing functions and triac gate drive pulses are inhibited until there is sufficient supply voltage across the device to guarantee complete gate drive pulses.

This ensures that bulk conduction is established in the triac and correct linear operation of the control system is maintained.

Negative Triac Gate Firing Pulses

Since the device works with the positive supply common, the triac gate pulses are negative going. This is an advantage when selecting a suitable triac since most triac manufacturers prefer this drive polarity.

The device is designed to give a triac pulse that is greater than 100mA for a period of 50 microseconds with standard pulse timing components (47nF. pin 10). Repeated triac gate pulses are given if the triac fails to latch or becomes unlatched due to motor brush bounce.

Well-Defined Control Voltage/Phase Angle Relationship

An internal -5V reference circuit is used as the charging voltage for the pulse timing ramp capacitor and as the reference voltage for the speed input potentiometer. This ensures that maximum phase angle can be obtained by adjusting the resistor or capacitor on the pulse timing circuit without affecting the maximum setting.

Average Load Current Sensing

The load current is normally sensed in the positive mains half cycle by means of a low impedance resistor in series with the triac and load. The voltage drop across this resistor is converted back into a low current source by a second resistor and fed into the load current sensing input (pin 1) of the IC. In high load current applications where the power dissipated in a series sensing resistor would be unacceptable, a current transformer may he utilised.

Section 9
Application Notes

GEC PLESSEY
SEMICONDUCTORS

SATELLITE RECEIVER DESIGN

The start-up phase of engineering developments is often characterised by a multiplicity of opinions and solutions to the problem, adding great interest but not a little confusion to the subject. In the course of time the situation clarifies with one or two solutions gradually gaining wide acceptance due to their simplicity and cost effective nature. Such is the situation in the satellite receiver market at the present time, where standards are few and far between with even transmission characteristics differing from one broadcast company to another, but with a trend towards a more standard receiver emerging.

In order to simplify the situation, only the single conversion and block conversion systems will be discussed here although much of the applications information and most of the products will be appropriate to other situations.

SINGLE CONVERSION RECEIVERS

The simplest form of receiver is probably the single conversion type shown in Fig 1. Here, the incoming signal is amplified and mixed with the local oscillator signal to produce a lower intermediate frequency in a similar manner to a conventional TV. Unfortunately both the amplifying and mixing processes have to be performed close to the dish, the first due to noise considerations, the second because it is not economic to transmit the high trequencies used in satellite reception via a relatively long coaxial cable.

The intermediate frequency is received by the indoor unit where an IF filter passes only the required signal to the FM demodulator. The choice of this intermediate frequency is one of the main areas of disagreement between designers, some using the existing 70MHz standard used in microwave link communications, but others adopting various higher frequencies up to 612MHz, making use of the low cost demodulators, SAW filters and amplifiers becoming available for these frequencies.

Now that the high cost objections to high IF usage have been overcome, other technical advantages, such as greater demodulator linearity (due to the lower percentage deviation) and simpler receiver design (because the inherently higher image rejection makes tracking filters unnecessary), will eventually ensure the universal adoption of high intermediate frequencies.

Design of single conversion receivers is complicated to some degree because programme selection is determined at the head end, requiring in the simplest case of a nonsynthesised receiver, a variable DC tuning voltage to be passed from the indoor to outdoor units.

This will probably require an additional cable, because the DC power supply for the head end unit will already be carried by the signal coax Where synthesised tuning is required the situation is additionally complicated as digital tuning information or a variable frequency reference must be transferred to the head end. Because the programme selection is determined at the receiver head end, the single conversion receiver has the disadvantage that reception of only one signal is possible from a dish, removing the possibility ot watching alternative programmes in different rooms of a house and making the system unsuitable for feeding apartment blocks or hotels.

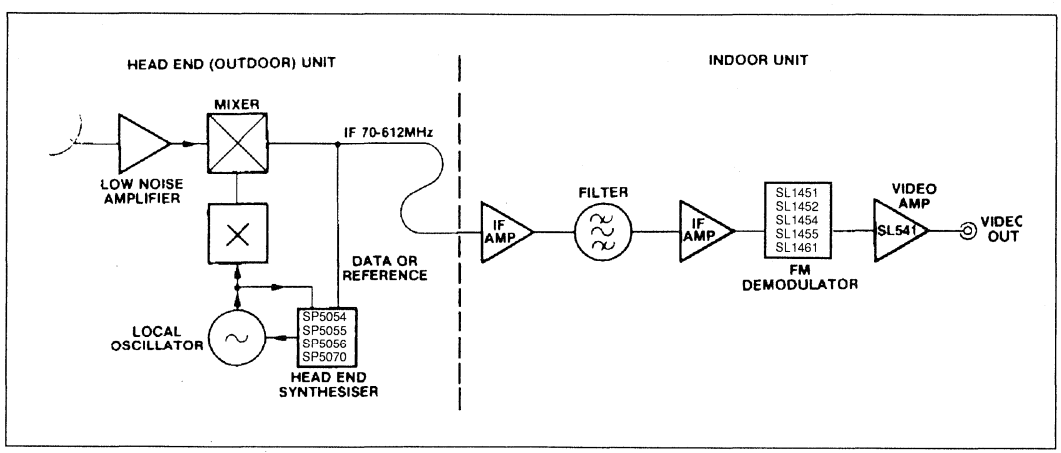


Figure 1: Simplified Block Diagram of Single Conversion Receiver

BLOCK CONVERSION RECEIVER

The block converter type of receiver shown in Fig 2 overcomes most of the disadvantages of the single conversion type by using a fixed frequency local oscillator at the head end. By this method all the available signals in the satellite band sharing the same polarisation are down-converted to an intermediate frequency usually ranging from 950MHz to 1450MHz or 1750MHz for transmission to the indoor unit. This technique transfers programme selection to the indoor unit and so removes the need for data or reference transmission to the head end. The technique also allows connection of several receiver units tuned to different signals and provides good image rejection due to the use of a relatively high IF. Programme selection is obtained by further down-converting the required signal to a fixed second IF using a voltage controlled local oscillator. A SAW filter or other type of bandpass filter is used at this point to reject unwanted signals. The choice of second IF is flexible as in the case of the single conversion receiver, with the same arguments causing a trend towards the use of higher frequencies.

SIGNAL TO NOISE THRESHOLD

In a frequency modulated system, as used in satellite TV reception, the demodulated signal to noise ratio decreases linearly with decreasing carrier to noise ratio before demodulation, until a level known as the threshold point is reached Below the threshold point, the output signal to noise ratio decreases rapidly, producing short duration high amplitude impulses which in the context of TV reception manifest themselves as light or dark spots on the picture commonly known as 'sparklies'. The threshold is defined as that point where the output signal to noise ratio departs by 1dB from the straight line relationship with the input carrier to noise ratio.

THRESHOLD EXTENSION

In an ideal world, the best method of obtaining a perfect picture at all times would be to ensure a good carrier to noise ratio under all reception conditions by using an adequate receiving dish, but in urban situations or in fringe areas, the size of dish required might be unacceptable and some method of extending the threshold point of the detector is desirable.

Although in many cases some form of threshold extension will be found necessary to achieve the required receiver performance, it should be noted that (as is often the case in engineering) improved performance in one direction means a compromise in another Threshold-extended FM demodulators are no exception, and unless carefully designed, problems such as picture tearing on fast black to white transitions can occur Although threshold extension techniques can successfully delay the onset of sparklies, under poor carrier to noise ratio conditions the effect **will** occur, generally producing noise pulses of longer duration than those from an unextended demodulator such as the SL1452.

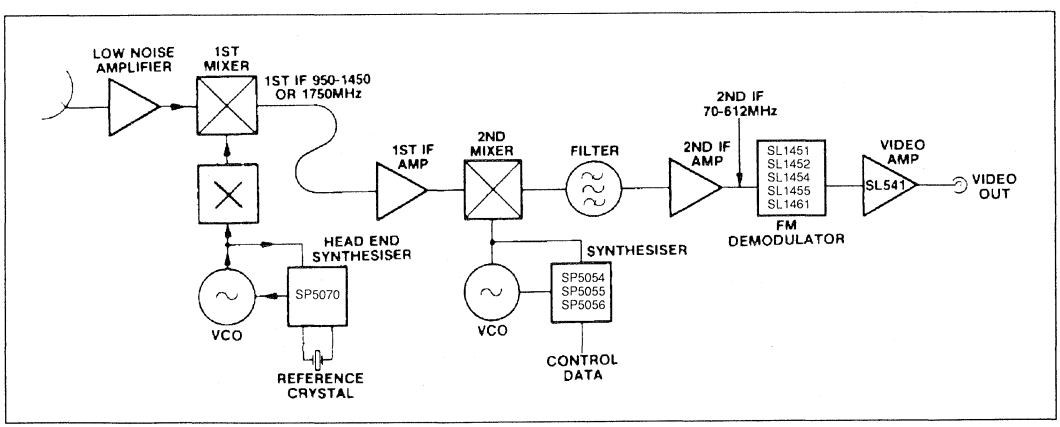


Figure 2: Simplified Block Diagram of Block Conversion Satellite Receiver

FREQUENCY SYNTHESISER APPLICATIONS

SP5070 2.4GHz FREQUENCY SYNTHESISER

In the block converter type of receiver shown in Fig.1, the local oscillator signal to the first mixer is a fixed frequency and is often controlled by a dielectric stabiliser. A more stable control of frequency may be obtained by using a phase locked loop synthesiser with crystal reference, such as the SP5054 or SP5055. Although either of these products could be used in such an application, the need for a 16-bit input word to select the operating frequency is a disadvantage when the device is situated at the remote end of the receiver downlead. Local generation of the necessary data word using CMOS logic elements or sending a suitably coded data word along the downlead are possible solutions to the problem, but it may be simpler to use the SP5070 fixed frequency synthesiser. The SP5070 can synthesise any frequency in the range 300MHz to 2.4GHz when fed with the appropriate reference.

The C-band satellite signals cover the range from about 3.67 to 4.17GHz and usinq a frequencv doubling mixer with low side oscillator injection, down conversion to the 950-1450MHz standard IF range will occur if the oscillator frequency is set at 1.36GHz. Since the multiplication ratio between the local oscillator and the reference input to the SP5070 is 256, a 5.3125MHz crystal reference will be required, as shown in Fig 2. A similar system but with a much greater degree of local oscillator multiplication could be used in a block down converter for 12GHz DBS reception.

The SP5070 can also be used for head end tuning in single conversion receivers by feeding a variable reference frequency along the downlead from the indoor unit. Since the reference is at a very different frequency from the IF the two can be easily separated with a minimum of filtering.

The variable reference frequency for this type of system is best generated using a low frequency synthesiser contained in the indoor unit, and a system using the GPS NJ8820 is shown in Figs 2 and 3.

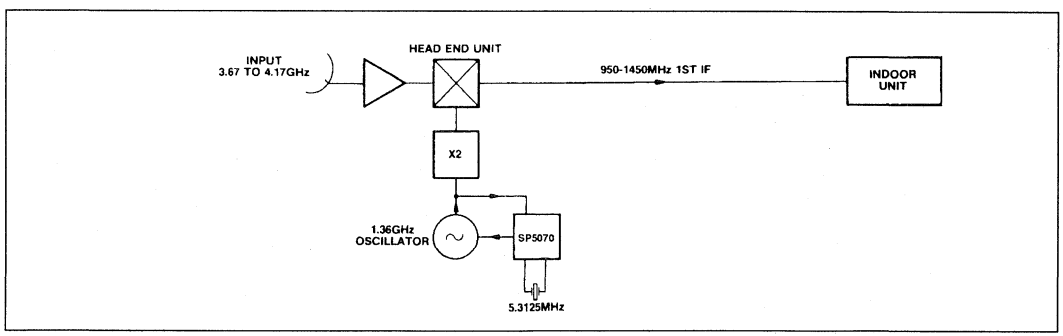


Figure 1: Synthesised Block Down Converter System

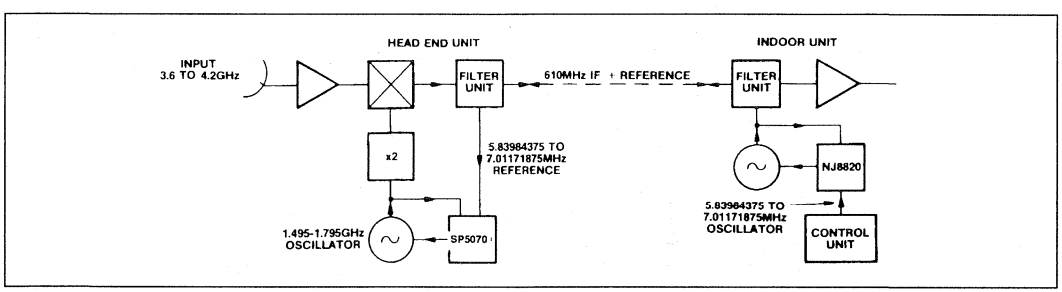


Figure 2: Block Diagram of Synthesised Single Conversion Receiver

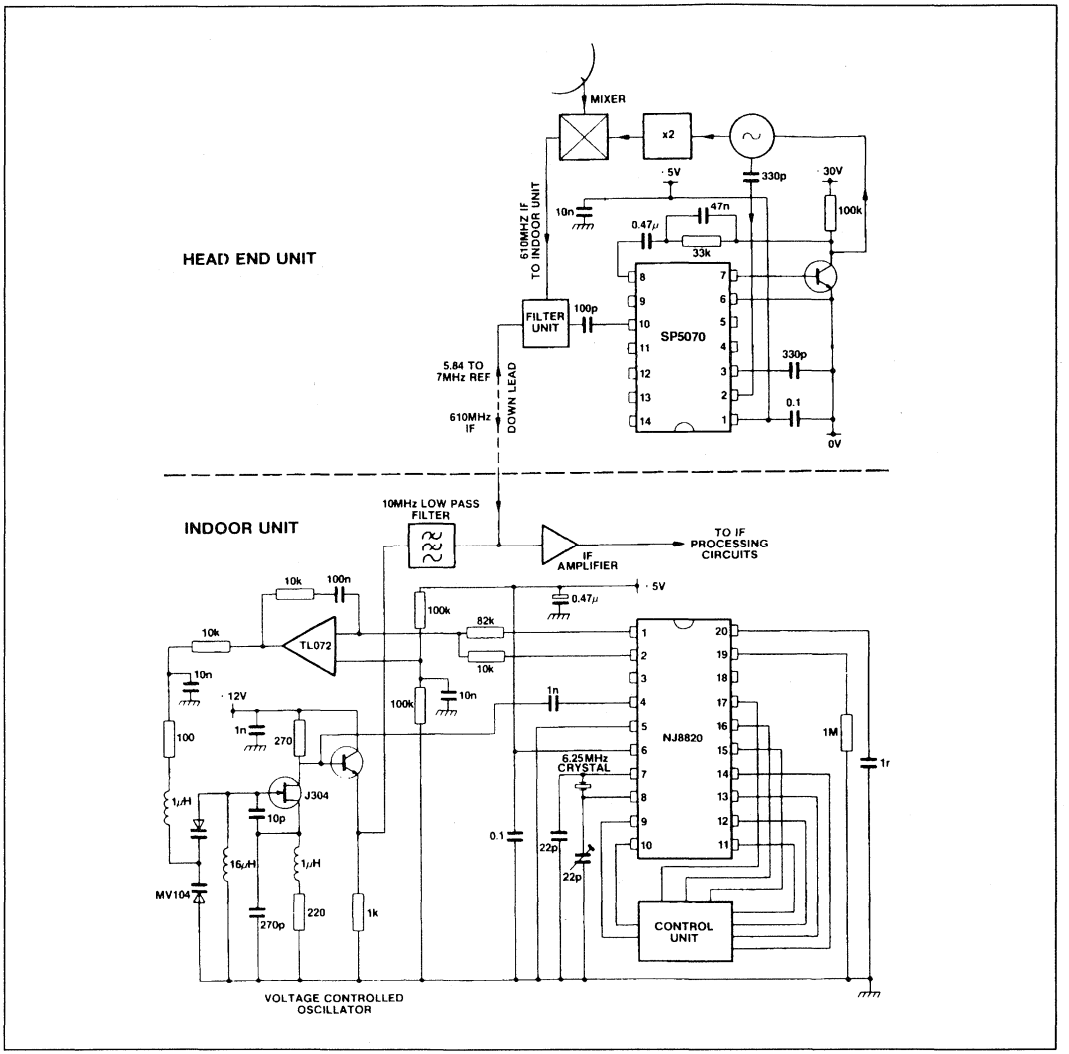


Figure 3: Circuit of Double Synthesiser

Using a frequency doubling mixer or x2 multiplier and assuming a 3.6 to 4.2GHz tuning requirement, 610MHz IF and a low side local oscillator, the required oscillator frequency range will be 1.495 to 1.795GHz.

The ratio of reference frequency to synthesised frequency of the SP5070 is 256, giving a reference requirement to be produced by the NJ8820 of 5.83984375 to 7.01171875MHz. Similarly if the step size at the mixer is set at 10MHz the reference step becomes 19.53125kHz.

Although these numbers are beginning to look somewhat formidable, the NJ8820 is capable of producing the required output if a 6.25MHz reference crystal is used with the reference counter programmed to divide by 160, or 320 including the fixed divide by 2. Frequency adjustment to anywhere in the required range can now be obtained by setting the ratio of the N counter in the NJ8820 as follows:

$$\text{Step size of NJ8820} = \frac{\text{crystal reference frequency}}{160 \times 2}$$

$$= \frac{6.25\text{MHz}}{320}$$

$$= 19.53125\text{kHz}$$

Programming input for reference counter.

= binary 160

= 00010100000

To tune a minimum frequency of 5.83984375MHz (for a mixer LO input of 2.99GHz) requires input to the NJ8820 N counter of:

$$\frac{5.83984375\text{MHz}}{19.53125\text{kHz}} = 299$$

= 0100101011

NOTE: Using this scheme the ratio at the NJ8820 N counter is equal to the local oscillator mixer input frequency in GHz x 100. For example, if the LO input to the mixer is required to be 3.15GHz the ratio will be 315 or binary 0100111011.

The flexible programming ability of the NJ8820 will allow a receiver using this system to be controlled using either a microprocessor or a multi-position switch in conjunction with a PROM as shown in the NJ8820 data sheet.

SP5054 2.6GHZ SYNTHESISER

Block conversion receivers generally produce a first IF ranging from 950MHz to 1450MHz in the case of the US C-band services, and from 950MHz to 1750MHz for the proposed DBS services. Using a high side local oscillator necessary to obtain the required tuning range, and with a European standard 480MHz 2nd IF the required frequency range will be 1430MHz to 2230MHz. Although calculating a suitable reference frequency to just cover the maximum requirement will give the smallest step size and therefore greatest resolution if fine tuning for AFC is used, the step size for any data bit does not coincide with the 19.18MHz standard DBS channel spacing, possibly increasing the complexity of the control software. A better solution might be to increase the reference frequency to 4.795MHz giving a rather curious minimum step size of 0.14984375MHz but producing a 19.18MHz step for the 27 data bit.

For a C-band system, a suitable reference frequency might be 5MHz giving a 20MHz step for the 27 data bit with a minimum step size of 0.15625MHz and a theoretical maximum synthesised frequency of 2.5598GHz, well above that required for a 612MHz IF.

REMOTE PROGRAMMING OF SP5000 SERIES SYNTHESISERS

Although remote programming of SP5000 series synthesisers appears complex at first sight, with a requirement for Chip Enable and Data Clock signals as well as the frequency data, the task can be greatly simplified using the circuit shown in Fig 6.

Obviously it is most convenient to have only a single downlead between the head end and indoor units of a satellite receiver, and therefore the system shown in Fig 6 sends data along the downlead at a relatively low frequency (125kHz) which can be easily filtered from the IFsignal. The data is sent as a burst of 125kHz, representing a '1', and a logic '0' by the absence of signal. The duration of each logic bit is 64 cycles of 125kHz equivalent to a time period of 0.512ms (see Fig.5).

Data Clock and Chip Enable inputs are generated locally from the data input to avoid having to encode these on the overworked downlead, the process being initiated by the leading edge of the first data bit which must always be logic 1. Since the first data bit is used only by the band select or ccntrol outputs, this causes no frequency setting limitation and the second bit is still available for use as a polarisation setting control.

CIRCUIT DESCRIPTION (FIG.6)

The 567 phase locked loop tone decoder chip is set to detect the bursts of 125kHz, producing a low output at pin 8 when the input is present. Loop and output filter components are selected to give fast response consistent with reasonable noise performance. As the first bit in the data stream must always be a logic '1', the negative-going edge at pin 8 produced at the beginning of bit 1 is used to trigger the R-S flip-flop formed by two CMOS NAND gates thus initiating the decoding process. Pin 8 also provides the data input to the SP5000 series device whilst the R-S flip-flop provides Chip Enable.

Once the R-S flip-flop is triggered, the output of the 567 oscillator, at or very close to 125kHz (depending on the presence or lack of 125kHz at the input) drives the 4040 counter. After 32 cycles of the 125kHz input data stream the Q6 output on pin 2 goes high providing a data clock signal to the synthesiser in the centre of the 64 cycle data period. Data clock pulses will continue from pin 2 until all 16 data bits are clocked, when the Q10 output on pin 14 goes high resetting the R-S flip-flop and terminating the chip enable signal. The R-S flip-flop also resets the 4040 leaving the system to be retriggered by the next data stream.

A suitably encoded data stream can be generated under

program control from a microprocessor or perhaps more easily by gating under program control the divided output from the microprocessor oscillator (often 4MHz, which, when divided by 32 gives 125kHz).

A low pass filter such as that shown in Fig.6 should be inserted between the downlead and data generating logic to prevent harmonics from the logic section interfering with the picture when fine tuning is used. The same filter will also prevent loading of the IF output by the logic.

Although as shown above there are various down conversion systems applicable to satellite reception, all have a requirement for some form of control system. A microprocessor used in this control function usually gives greatest flexibility allowing decoding of remote control and local keyboard inputs, generation of input data for synthesisers, channel display and a program memory feature using a single component.

MICROPROCESSOR CONTROL

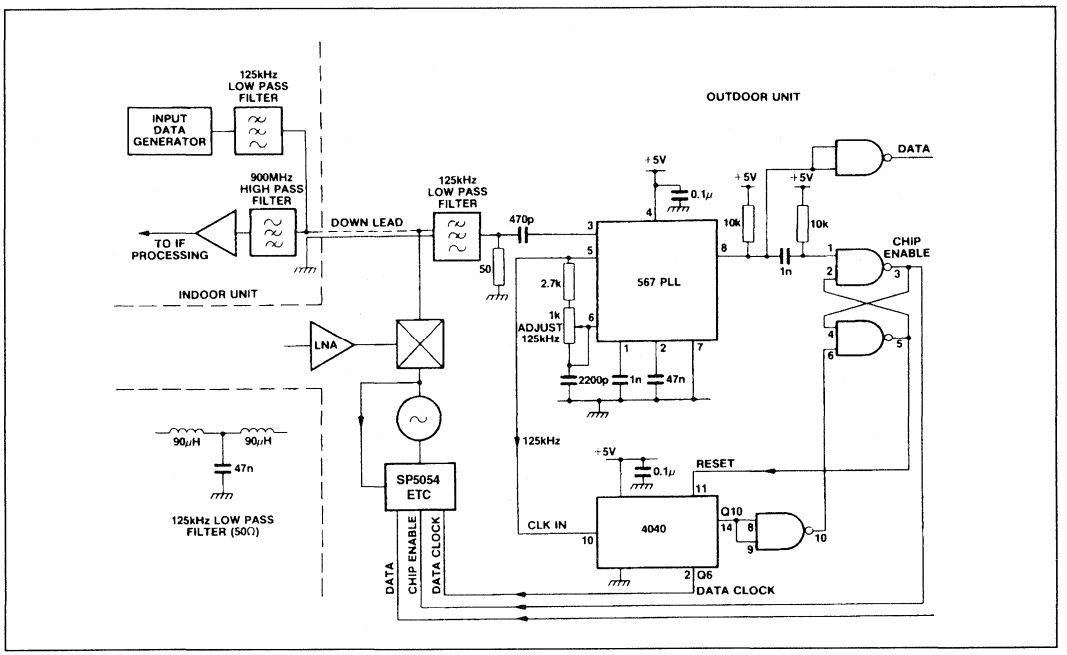


Figure 4: Remote Data Receiver Circuit Diagram

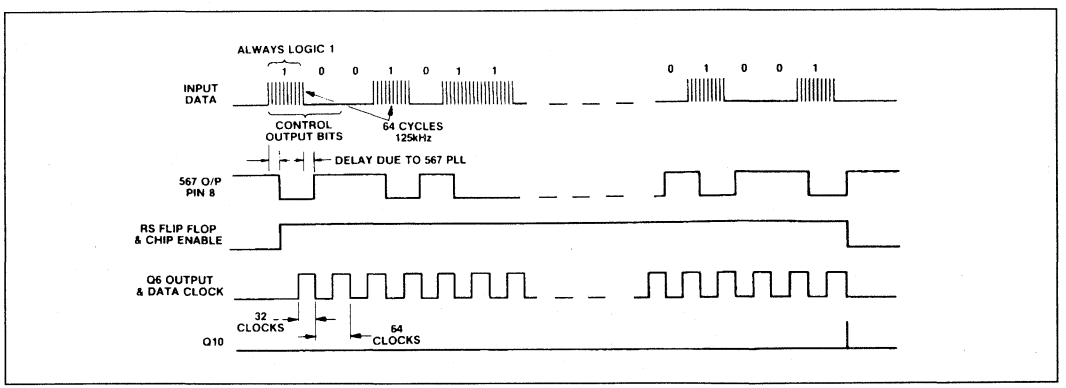


Figure 5: Remote Data Receiver Waveforms

A LOW COST 1.5 to 2.2GHz VOLTAGE CONTROLLED OSCILLATOR

The introduction of the GPS range of 2GHz synthesisers and prescalers for low cost applications such as consumer satellite TV reception has created the requirement for an economic VCO design covering a frequency range from around 1.5GHz to 2.2GHz. Although suitable hybrid oscillator designs are available from various manufacturers, these generally carry a price tag at least an order of magnitude higher than the synthesiser, thus making their use in consumer equipment hopelessly uneconomic.

The design shown in Fig.1 has been developed using low cost components which should be easily available, the varicap diodes being normal UHF TV tuning types and the transistor a standard catalog item.

A major problem when operating at these frequencies is that the series inductance of most capacitors becomes very significant compared with that required in the resonator circuit and also prevents good decoupling. These problems are overcome when designing fixed frequency oscillators by replacing the normal resonant circuits and decoupling capacitors with open or short circuited resonant transmission lines but a design requiring wide frequency variation must use more conventional techniques.

The transistor is biased to about 1.5mA using a 22kΩ resistor from collector to base. Any problems with decoupling at the emitter are avoided by connecting the emitter direct to ground. Stabilisation of the bias point relies on the 330Ω collector load resistor providing a degree of feedback A small inductor in series with the collector load resistor reduces any loading and improves the effectiveness of the +12V supply decoupling A series tuned circuit consisting of a small inductor and two varicap diodes is connected between collector and base with a 390pF capacitor providing DC isolation of the varicap diodes from the collector voltage. To avoid the introduction of any additional series inductance, the varicap diodes are connected direct to the transistor base without a coupling capacitor The oscillator frequency is varied by adjusting the varicap bias voltage from 0 to 30V via a 47kΩ isolating resistor Output amplitude from the basic oscillator is much higher than the input requirements of the synthesiser or prescaler and therefore about 10dB of attenuation is provided by a resistive attenuator.

As might be expected with an oscillator operating at this frequency, layout is fairly critical and the layout shown in Fig.2 should be followed accurately or extensive trials made before any variations are attempted. The prototype oscillators were made on standard 1/16 inch fibreglass board, but it was found impossible to mount the frequency determining components on the board without greatly affecting the frequency range available; these components are therefore mounted off board, relying on short lead lengths to provide sufficient rigidity.

OSCILLATOR SPECIFICATION

Operating Voltage: +9V to +14V
Frequency Range: 1.5GHz to 2.2GHz
Varicap Voltage Range: 0V to +30V
Output Level: (with 10dB attenuator) -10dBm (70mV)

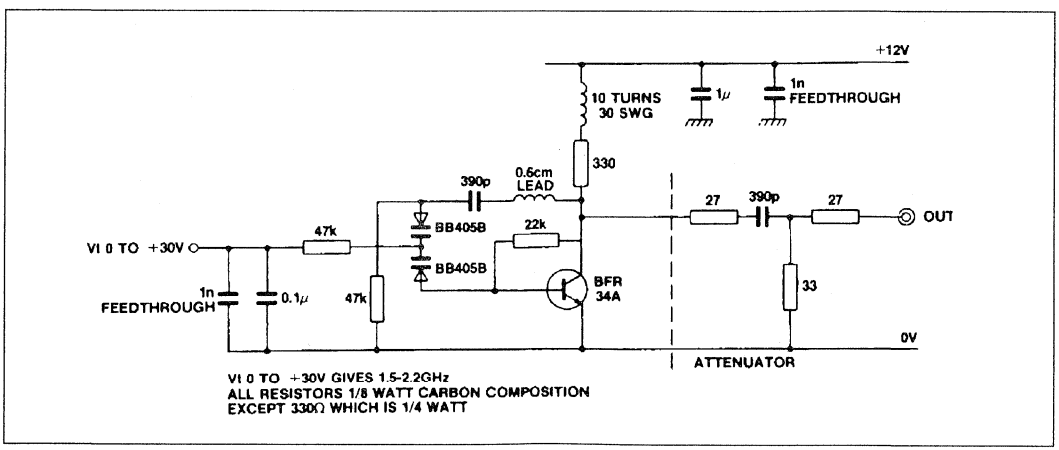


Figure 1: 2GHz VCO Circuit Diagram

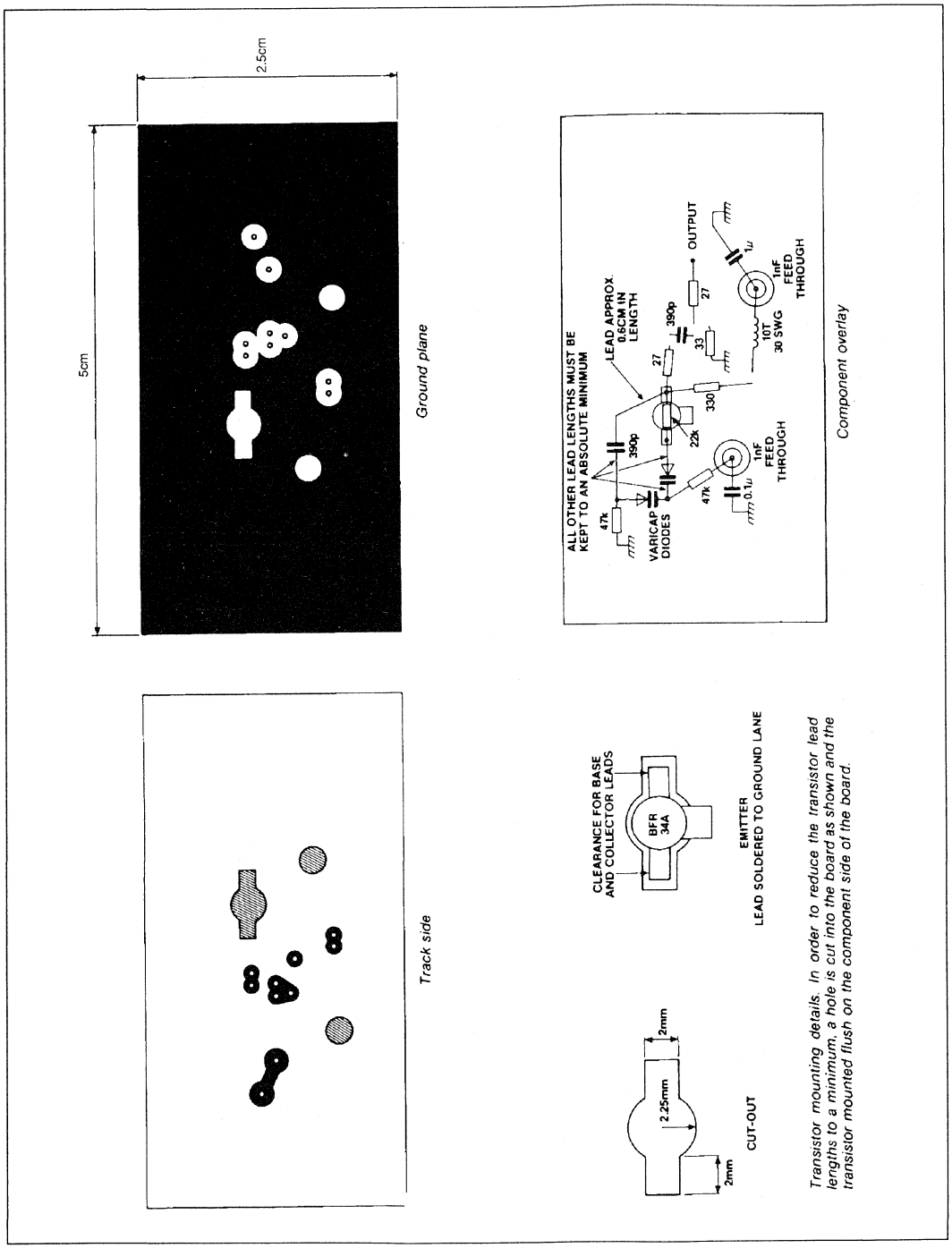


Figure 2: Oscillator printed board layout

A 600MHz AGC Controller IF Amplifier for the SL1455

From the SL1455 data sheet and application note, it will be seen that the degree of threshold extension and the video bandwidth are determined by the input level. For best results some method of accurately setting the input level and maintaining it under varying signal conditions is desirable . Various methods of controlling signal level are possible including the use of PIN diode attenuator, limiting amplifiers, etc. but the AGC system described here appears to offer a low cost flexible system with adjustable output level and wide AGC range (up to 45dB) which cannot be easily obtained by other means.

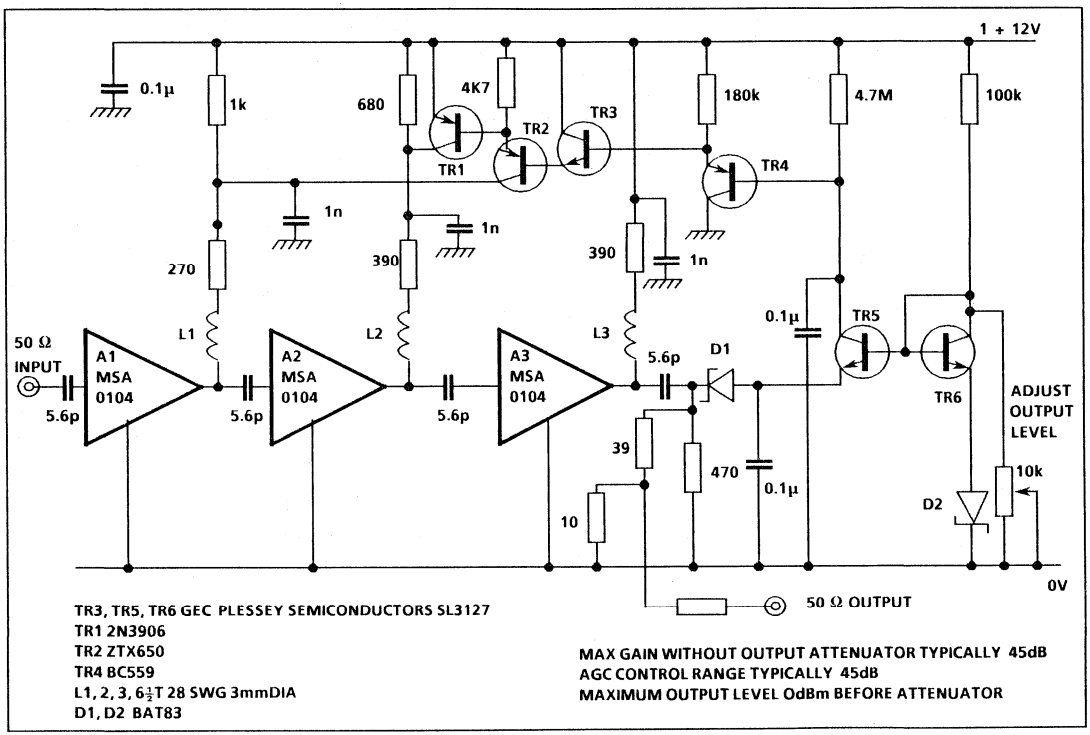


Fig.1

Gain is provided by a cascade of three Avantek MSA-0104 amplifiers with a gain of about 15dB per stage. The output from the third stage is detected and the resulting DC used to control the gain of the first two amplifier stages.

In order to allow detection at the low signal levels required by the SL1455, and to allow a degree of temperature compensation in the AGC point, a balanced arrangement of two transistors and Schottky diodes is used, increasing signal levels at the output producing an increasingly negative output at D1 anode. The negative output from the diode turns on TR5 which decreases the current in the first amplifier stage via the emitter followers TR2, 3 and 4 thus reducing the gain and maintaining constant output.

As the input signal is increased further, current in the first amplifier reduces until TR2 is no longer passing sufficient current to hold TR1 on, at which point the supply current to amplifier two is reduced, continuing the AGC action until TR1 is fully switched off.

The 1K and 680Ω resistors in parallel with TR1 and TR2 set a minimum current level in the amplifiers which is designed to allow a minimum gain level consistent with sufficient signal handling to drive subsequent stages. This together with the sequencing of the gain reduction system prevents overload in any of the amplifiers for all input signal levels within the dynamic range.

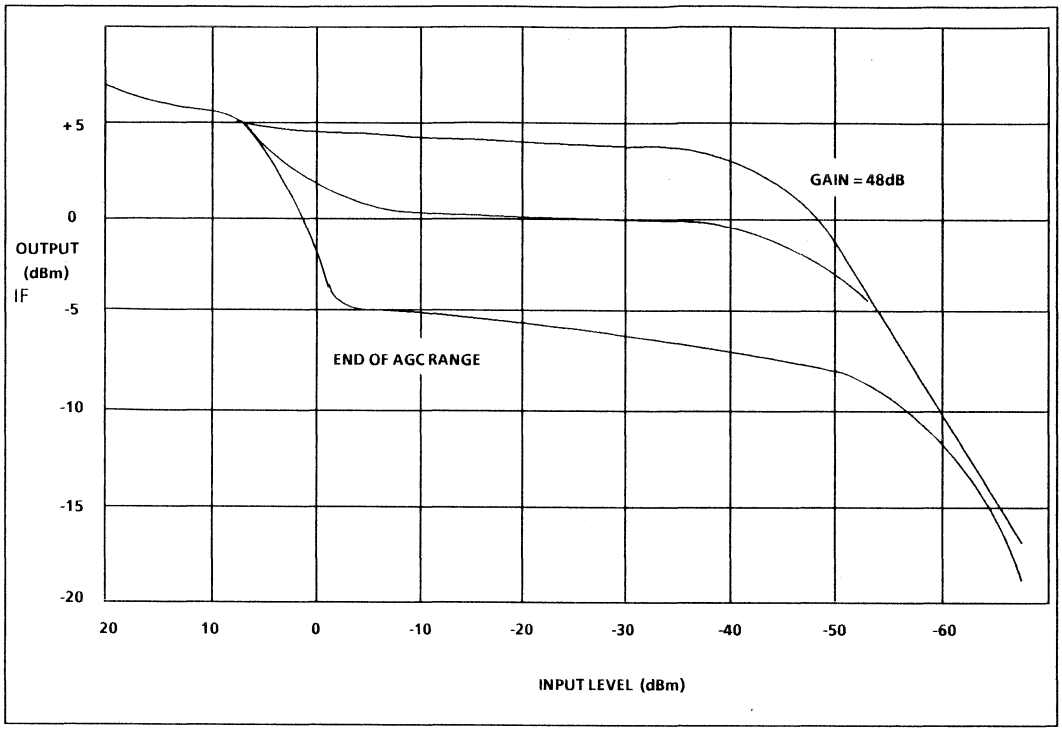


Fig. 2 Characteristics of IF strip with AGC at 610MHz

Despite the balanced detector arrangement, it is still not possible to provide reliable AGC detection at the typical -20dBm level required for best threshold performance in the SL1455 and therefore a fixed T type attenuator is used to reduce the output level.

Fine control of output level is provided by the potentiometer RV1 which allows adjustment for IC and other component tolerances.

SL486 INFRA-RED RANGING AND DIRECTIONAL INFORMATION

There is a requirement in many situations for a receiver to obtain ranging and directional information from a remote transmitter. This note describes how the SL486 may be used to provide this information. A block diagram of the ranging system is shown at Fig. 1.

The SL486 is a high gain pre-amplifier designed to form an interface between an infra-red receiver diode and the digital input of remote control receivers. The device contains two other circuit elements, one to provide a stretched output pulse facility and a voltage regulator to allow operation from a wide range of supplies.

The infra-red ranging application utilises the automatic gain control (AGC) decouple output on pin 8 of the SL486. 20ms bursts of 100kHz infra-red radiation are received by the SL486. These bursts produce an AGC voltage as shown in figure 2a. This voltage waveform has a variance of 300mv on a DC level. The 300mV signal varies with range and it is this signal which is used to provide the ranging information. The DC level varies slightly around 2V with changes in the surrounding light level, and so an ambient sample and hold is necessary to maintain an ambient reference level.

A synchronising pulse generator is edge triggered from the buffered AGC signal to provide a sample pulse for the ambient sample and hold circuit.

This synchronising pulse is also used to drive the sample pulse generator which produces a short duration sample pulse for the output sample and hold stages.

With the ambient infra-red level subtracted from this signal, a pulse is extracted from the resulting waveform to give a 10ms wide pulse whose height corresponds to the distance from the remote transmitter. This pulsed voltage is sampled and held to give a DC voltage level which represents range.

In order for directionality to be achieved at the receiver station, two ranging systems are used in parallel; with the receiving diodes mounted at 90° to each other.

The system's open loop range may be limited to a desired maximum operating range by simply altering a parallel resistor value on the receiver diode.

The operation of the system is illustrated in Fig.2 in terms of the circuit waveforms.

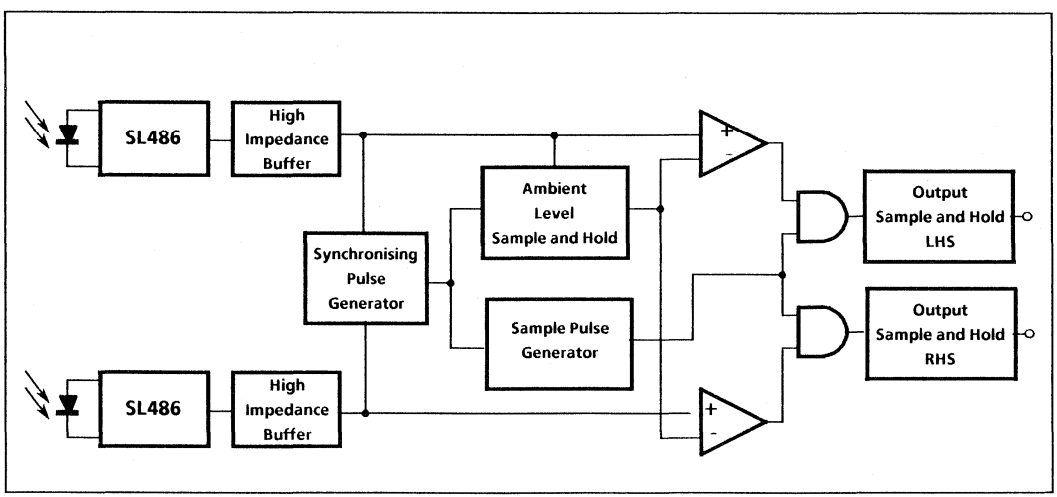
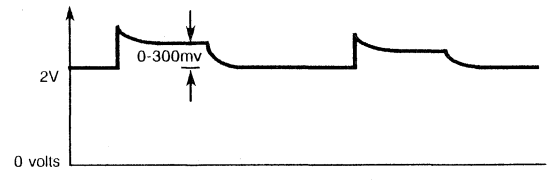


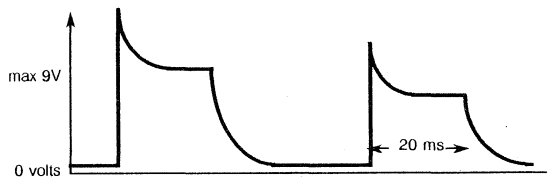
Fig.1 System block diagram

a. This buffered AGC output waveform is the system's starting point. The buffer is necessary to prevent loading of the SL486 AGC pin.



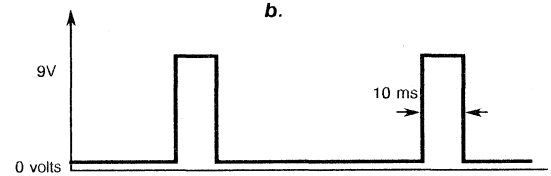
a.

b. With the 2 volt ambient level subtracted and the result amplified, this waveform is obtained. The shelf height is proportional to range.



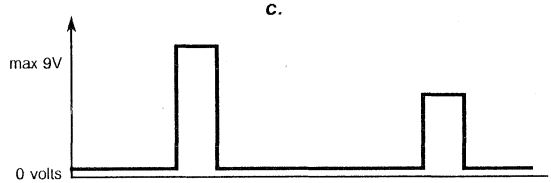
b.

c. This sample waveform is generated so that the shelf in b. may be extracted.



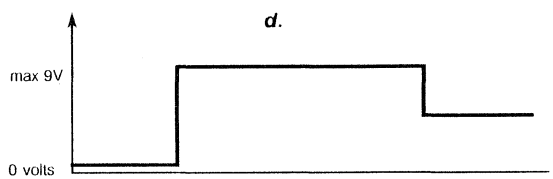
c.

d. The result of AND'ing together b. and c. produces this waveform whose pulse height represents range. This may then be sampled and held.



d.

e. This sample and held dc level is proportional range from the transmitter. A strong signal represents closer proximity.



e.

Fig. 2. System Waveforms

MA818

A MICROPROCESSOR CONTROLLED DIGITAL PWM MOTOR CONTROLLED IC

With a growing trend towards microprocessor control of pulse width modulated AC motor drives, GEC Plessey Semiconductors introduces the first fully digital stand–alone PWM generator IC for use in such drive units.

AIM

Several manufacturers have for some years been producing analog pulse width modulated (PWM) generator circuits for use in drive systems. These rely upon potentiometer control of parameters such as speed, acceleration and deceleration rates, pulse deletion and pulse delay (underlap) times. However, a growing demand has emerged in the drives market for digitally controlled drive units with direct keypad entry of operating parameters, and often with the ability to communicate with external computers/controllers.

To this end, GEC Plessey Semiconductors have produced the first fully digital PWM generator IC family incorporating an industry standard microprocessor interface to produce full feature motor control with minimal hardware and software overhead whilst giving unprecedented stability, accuracy and speed range.

In addition, this low cost solution can be software configured to be used with the whole spectrum of power switches (including silent operation with fast switches) and also incorporates DC injection braking capability.

PULSE WIDTH MODULATION TECHNIQUES

The process of pulse width modulation is shown in Fig. 1. the desired power waveform is compared to a triangular waveform of considerably higher frequency and slightly greater amplitude (*termed the carrier waveform*). The intersections of these two waveforms dictate the digital transitions of the PWM output.

The voltage swings of the digital PWM output are stepped up by a power switch stage (see later) before being fed to the machine. The inherent low–pass characteristic of the machine will filter out the high frequency components due to the chopping behaviour, leaving the desired power waveform only.

The MA818 (and family) use a very similar process to that described above, but differ in the sampling of the desired waveform, as shown in Fig. 2. Since the devices use a digital implementation of the PWM process to increase stability and reduce drift problems, the desired waveform is sampled at the peak and trough of the triangular carrier waveform. This is *(termed double edged regular sampling)* The comparison of the two waveforms is still carried out on a continuous basis however. The MA818 has three such PWM channels working simultaneously to produce the required outputs for a three phase machine, each being transposed 120° from the next.

The process described above is *asynchronous*, that is, the carrier frequency is set independently and is therefore not necessarily a fixed multiple of the desired frequency (which is varying). This allows for easy interfacing of the MA818 to the power electronics.

The alternative approach – *synchronous PWM* – locks the carrier frequency to an exact integer multiple of the power frequency. This implies that the carrier frequency varies with the power frequency which would make interfacing to the power electronic considerably more difficult, and some cases, impossible.

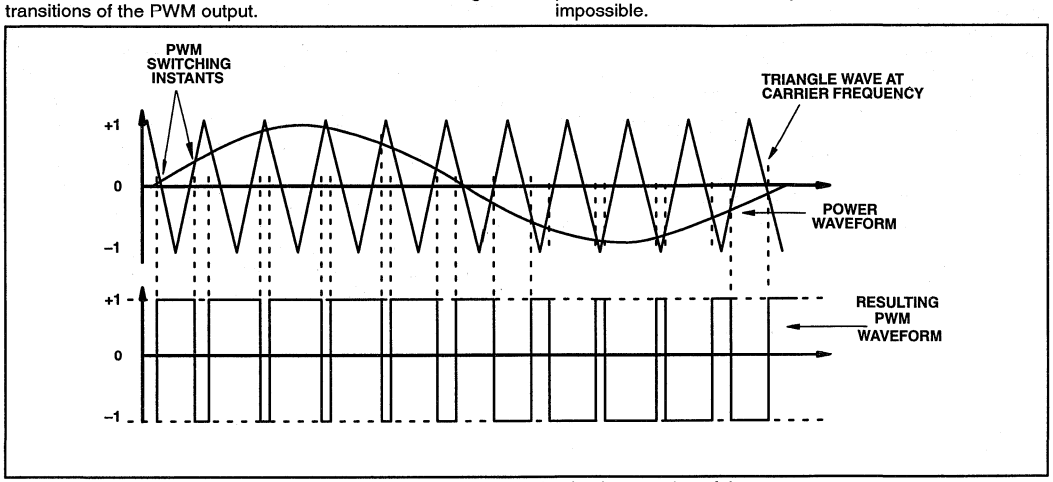


Fig. 1. Natural PWM as used in analog implementation of the process

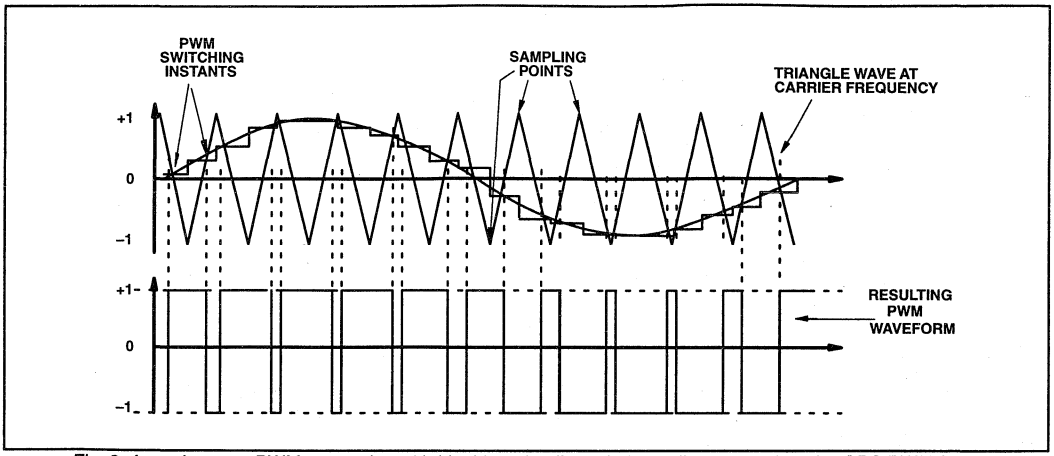


Fig. 2. Asynchronous PWM generation with 'double–edged' regular sampling as used on the GPS PWM family

FUNCTIONAL DESCRIPTION

Micropprocessor Interface

The block diagram in Fig. 3 shows the internal architecture of the MA818. The device is controlled via an 8–bit industry standard microprocessor interface. Decode logic has been integrated on–chip so that no 'glue–logic' is required between the microprocessor and the MA818. The device also features a novel 'bus identifier' which automatically adjusts the interface to accept Motorola or Intel machine cycle formats with no user intervention. This is referred to as a MOTEL* interface. Micro processors such as the 8085, 8088 etc. can be used directly with the device as can microcontrollers such as the 8051 and 6805.

Full chip select and read/write strobing inputs are provided and in addition a reset line allows the user to return the device to a known condition at any time.

The whole device, with the exception of the microprocessor interface, is timed via the clock input. The clock will normally be generated from a crystal of up to 12.5MHz to ensure good temperature and ageing characteristics.

It should be noted that the microprocessor interface is entirely independent of the clock generator circuit such that the microprocessor can load all parameters asynchronously.

Internally, the device has a series of registers which may be written to directly from the interface. These are used to tailor all aspects of the PWM output pulses, including carrier frequency, pulse deletion, pulse delay and rotational speed. This gives cost advantage both in terms of component savings and in allowing the same circuit to control a number of different motor drives simply by changing the microprocessor software.

** MOTEL is a registered trademark of Intel Corp and Motoro;a Corp.*

Carrier Frequency

The carrier frequency, i.e. the frequency of the triangular waveform is derived directly from the master clock input according to the contents of the Initialisation Register. Carrier frequencies up to 24kHz are available to allow the use of the entire spectrum of power switches from fast MOSFETs and IGBTs (at ultrasonic carrier frequencies) down to bipolars at low carrier frequencies. If a different carrier frequency is required, the crystal frequency may be changed.

Power Frequency Range Selection

The power frequency range (that is, the frequency range of the desired power output waveform) can be selected via the initilisations Register and is also a direct function of the carrier frequency. As a result, a 'sliding scale' is implemented giving power frequency ranges from 0 to 1,95Hz up to 0 to 4000Hz, depending upon the choice of carrier frequency. Hence an unprecedented range of frequencies can be selected. In fact there are forty–two combinations of carrier frequency and power frequency range. The power frequency range also serves to limit the maximum frequency supplied to the motor to provide a safe operating range.

Rotational Frequency Control

The actual frequency at which the waveform is emulated is governed by a 12–bit binary word, written directly to the MA818 by the micro. In addition, a sign bit is provided which changes the phase sequence from R–Y–B for forward rotation to B–Y–R for reverse rotation. Hence an effective 13 bits of speed control is achieved. This, in combination with the power frequency range control mentioned above gives speed control from ±500μHz to ±4000Hz without reconfiguring hardware, giving over 300 000 selectable speeds.

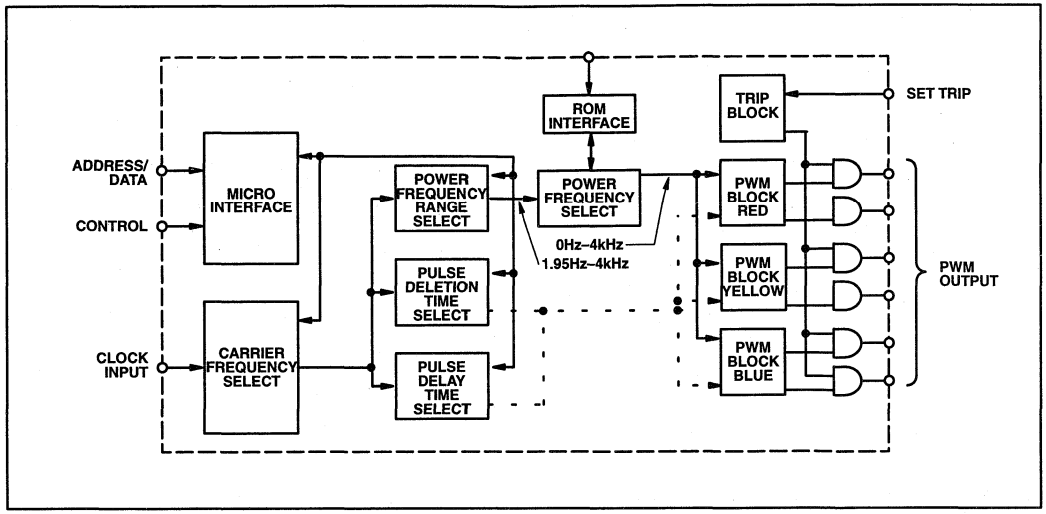


Fig. 3 Block diagram of the MA818

Zero frequency may always be selected irrespecive of the carrier frequency and power frequency range to provide a 'rotor retention' or DC injection brake facility. This is of particular use in machines tools where the work may be held perfectly stationary with no risk of run–on.

Power Waveform

The desired waveshape is read from an external ROM or EPROM in order that it may easily be changed to suit specific requirements. This ROM is connected directly to the MA818 via dedicated pins. No other circuit elements are necessary all addressing the decoding is done on–chip.

Only the positive half–cycle of the waveshape is stored in order to minimise the size of the ROM. Hence the only limitation placed on the waveshape is that it must be symmetrical about the 180° axis–see Fig. 4.

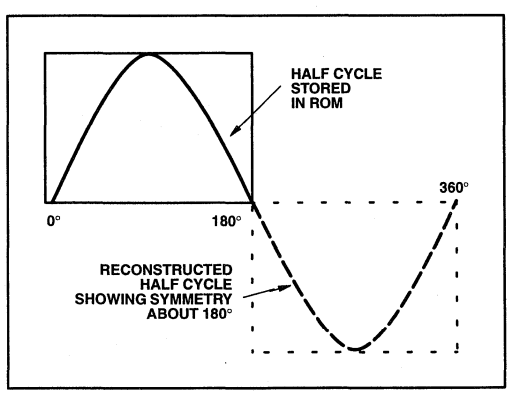


Fig. 4. Reconstruction of full cycle from ROM

For the vast majority of applications two specific wave shapes are sufficient:

1. Pure sine wave. Used in applications where waveform purity is of particular importance.

2. Sinewave with third harmonic superimposed at one sixth the amplitude of the fundamental.

Due to inverter operation it can be shown that the maximum achievable output from a PWM system such as this is only 86.6% of the input voltage swing. This clearly does not make for an efficient system and inevitably leads to motor derating.

In order to make full use of the input voltage swing it would be necessary to increase the output voltage to 1/0.866 = 1.154 of its nominal value – i.e. an increase of 15.4%.

This is achieved by adding an attenuated third harmonic components as shown in Fig. 5.

Fig. 5a shows the two individual frequency components and Fig. 5b shows the composite signal when they are summed. The phase output voltage remains unchanged but the line voltage is now increased by 16.7% due to the cancellation of cophasal (odd triplen) harmonics in a three phase system (as shown by the dotted line of Fig 5b).

This increase in performance is obtained with no increase in harmonic component of the output due to the harmonic cancellation effect.

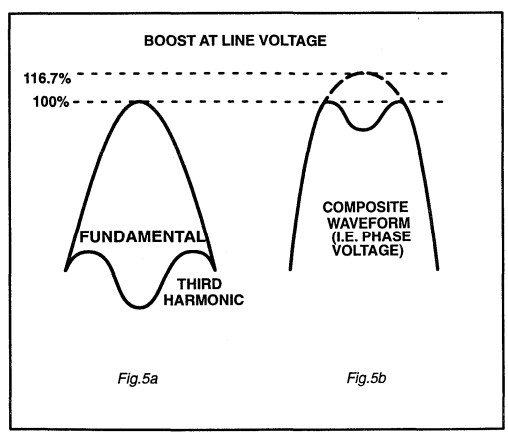


Fig. 5 Construction of composite phase voltage

AMPLITUDE CONTROL

In the majority of drive applications, two particular kinds of amplitude response are required, as shown below in Fig. 6.

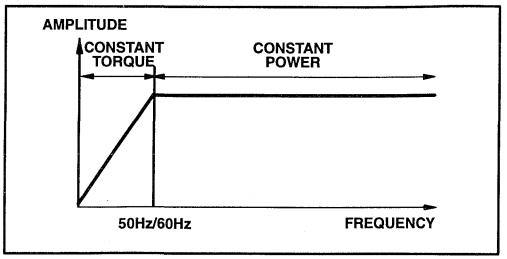


Fig. 6a Amplitude response for motor control

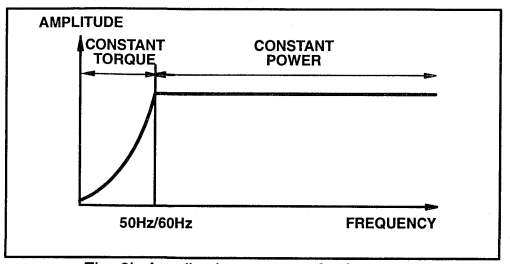


Fig. 6b Amplitude response for fan control

If the device is to be used with a motor load, a curve such as that shown in Fig. 6a will be required. Alternatively, if a fan is used a square–law curve such as Fig. 6b should be used.

Successive 8–bit amplitude words can be written to the MA818 from the controlling microprocessor in order to reproduce these curves, or for that matter, any complex amplitude function. Usually, these curves will be retained in a small look–up table within the microprocessor memory and the amplitude will be changed whenever the power frequency is altered.

If the device is to be used as part of a switched mode power supply, uninterruptible power supply or any other waveform generator application, a constant amplitude will generally be required. In this case the amplitude word will be set to full scale at all times.

Pulse Deletion/Pulse Delay

Fig. 7 shows the typical inverter network used in three phase PWM systems.

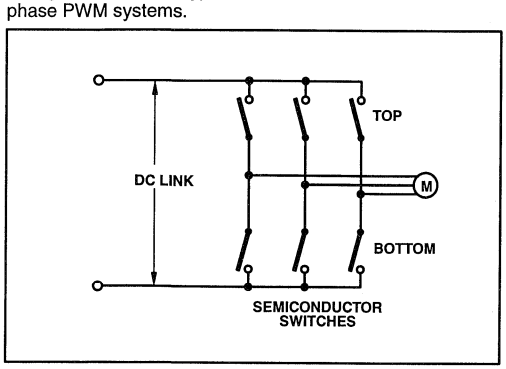


Fig. 7 Three phase power bridge

It is essential when firing the switches in a network such as that in Fig. 7 to ensure that both switches in any one vertical arm are off before one switch can be turned on. If this rule were not obeyed there would be a risk of *shoot–through* i.e. a dead short across the DC link when both switches are on simultaneously. Such a scenario would inevitably arise if the sense of both switches in an arm was changed simultaneously due to the finite turn–off time associated with semiconductor devices.

To circumvent this problem, the MA818 allows for a pulse delay or 'underlap' time when neither switch is enabled. When sufficient time has elapsed to ensure that both switches are fully off, another change of state is allowed. The net result of this is a quasi–complementary pulse train to the top and bottom switches rather than being strictly complementary. Fig. 8 shows the effect on a 'pure' PWM pulse train delay. the delay period can be predetermined by writing one byte to the MA818 and is also a function of the carrier frequency in order to provide a very wide range of values for all types of power switches. the range of delay times exceeds 400:1.

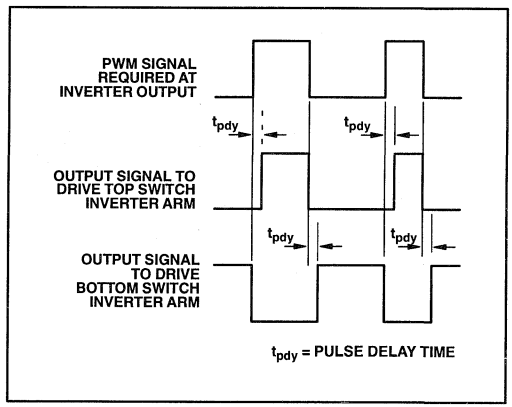


Fig. 8 Effect of pulse delay on PWM pulse train

The power dissipation of the power switches is largely dependent upon the number of switching events which the power devices have to endure in a given time. In order to minimise these losses, the MA818 deletes all pulses in the train of less than a pre–determined period. In this case no change of state will occur and the switching loss is reduced. this time is generally selected to correspond with the period of time taken for the power switch to turn on and immediately off again. Fig. 9 shows the effect of pulse deletion diagrammatically

The pulse deletion time is selected by writing one byte to the IC in the same way as pulse delay.

Other Features

The MA818 features six PWM outputs corresponding to the top and bottom switches of three phases. In addition, the device includes a low–going TTL signal to indicate the zero–crossing point (i.e. 0° point) of the red phase. This may be used to provide closed–loop speed control and is of particular use in slip compensated systems.

Another useful feature incorporated into this device is an emergency trip. The SET TRIP pin, when taken high, acts to disable all the TTL outputs without software intervention, effecting an immediate shutdown of the power electronics. A TRIP acknowledge signal is provided for monitoring purposes.

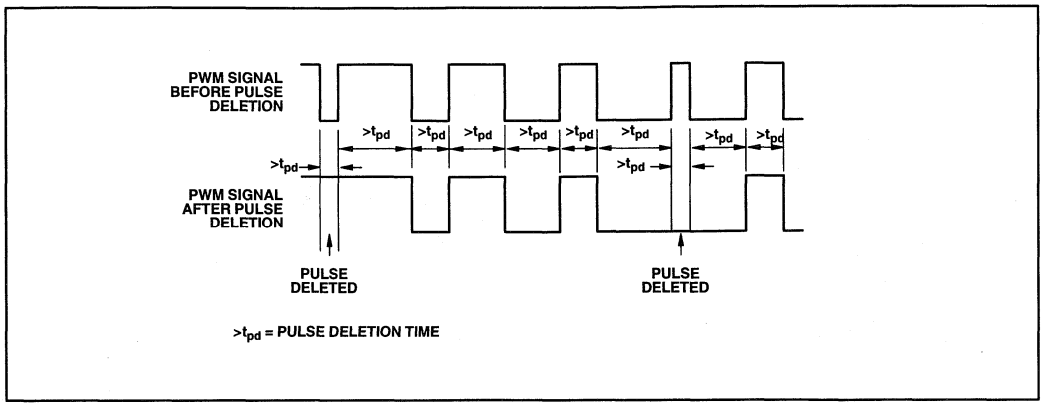


Fig. 9 Effect of pulse deletion on PWM pulse train

APPLICATIONS

Fig. 10 shows a typical application circuit for the MA818 in a drive system. Generally, a microcontroller having on–chip ROM and RAM will give a minimum component system, whilst still having enough I/O port lines to directly interface to the keypad, display and watchdog inputs.

Alternatively, a microprocessor can be used with separate ROM, RAM and I/O ports.

Clearly, it is possible to produce a working system using only three integrated circuits: a microcontroller, an MA818 and a waveform ROM. This represents a considerable saving in hardware development time compared to other alternatives.

Similar systems may be developed to provide soft start and dynamic braking using the MA818.

Note that once the various parameters have been written into the working registers within the MA818, the PWM sequence will begin and no further intervention from the microprocessor is required until, for example, the rotational speed needs to be changed. This frees the microprocessor to carry out other tasks, such as keypad scanning, display driving and watchdog functions. As a result of the small software overhead, the software development time and costs are considerably reduced.

The product range is backed up by a comprehensive range of literature, development hardware and software, including an Exercise Module operating from BASIC environment and a Demonstration Module containing typical software for use in a variable frequency drive environment. (All software is public domain and can be used in customer systems in order to reduce their development time). In addition, on line applications support is provided at all times to potential and existing customers.

The MA818 is available in production quantities and is currently designed into many commercial AC drives throughout the world.

FUTURE PRODUCTS

GEC Plessey Semiconductors has expanded its range of PWM generator ICs to include the MA828 family of devices. These are functionally identical to the MA818 but integrate the waveform ROM on–chip. thereby obviating the need to an external ROM. The MA828–1 is pre–programmed to emulate a sinewave plus superimposed third harmonic component whilst the MA828–2 emulates a pure sinewave. (Other waveforms may be supplied to order).

In addition a single phase version, the MA838, has on–chip ROM for use in motor control of white goods. This enables manufacturers to use a robust induction motor in preference to the traditional brushed universal motor thus making white goods inherently more reliable.

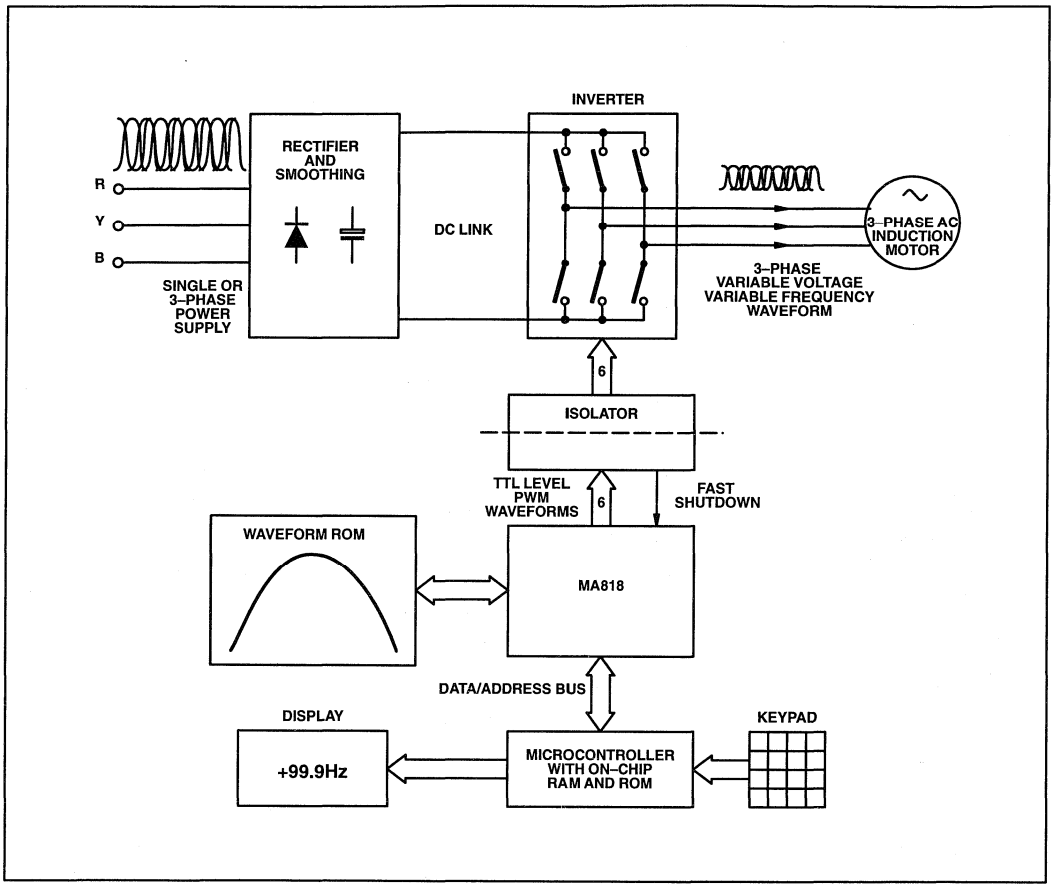


Fig. 10 Typical AC drive incorporating an MA818

PWM FAMILY: THREE PHASE MOTOR DRIVE DEMONSTRATION MODULE

The PWM family Demonstration Module has been manufactured in order to minimise the hardware and software development time needed to integrate the MA818/MA828/MA838 PWM generator ICs into a variable speed motor drive system. It comprises an Intel 8031 microprocessor–based board with relocatable software, for easy adaptation to the user's specific requirements. The six PWM outputs can be connected to an inverter bridge via suitable isolation.

FEATURES

- Fully Digital PWM Generation
- Full Microprocessor Control
- Speed Variable between ±0Hz and ±4000Hz
- Software Programmable Acceleration and Deceleration Times.
- Software Programmable Minimum Pulse Width and Underlap Times
- Direct Keypad Entry of Machine Parameters
- Full Display Capability
- RS232 Interface for Remote Control
- 'Jog' Facility to allow Machine Positioning
- Easily Interface to Inverter Bridge

GENERAL DESCRIPTION

The PWM family Demonstrator Module has been manufactured in order to minimise the hardware and software development time needed to integrate the MA818/MA828/MA838 PWM generator ICs into a variable speed motor drive system.

It comprises an Intel 8031 microprocessor–based board with relocatable software, for easy adaptation to the user's specific requirements. The six PWM outputs can be connected to an inverter bridge via suitable isolation.

The board has two modes of operation, selectable via a DIP switch:

1. MAXMODE– Has full numeric keypad for data entry and a 32 character alphanumeric display.
2. MINMODE– Has ↑ and ↓ keys for speed control and a 4–digit LED display.

All parameters are software selectable – including pulse deletion, underlap time, carrier frequency and maximum power frequency. The acceleration and deceleration times may be altered to match the nameplate values of the motor in question.

Both modes feature forward and reverse rotation to 12–bit accuracy between 0 and 4000Hz. Both fan and motor V/f curves are catered for and are software selectable. A variable boost voltage can be entered and , if necessary, the entire V/f curve can be altered.

The system incorporates a braking facility via the PWM generator and also a 'JOG' key to allow the machine to be inched into position. This may be of particular use in the machine tool industry where positioning is important.

An RS232 port allows the board, and hence the entire drive system, to be controlled from a remote source such as a mainframe or PC.

The system is supplied on a double–sided printed circuit board. full software and documentation is supplied with each board.

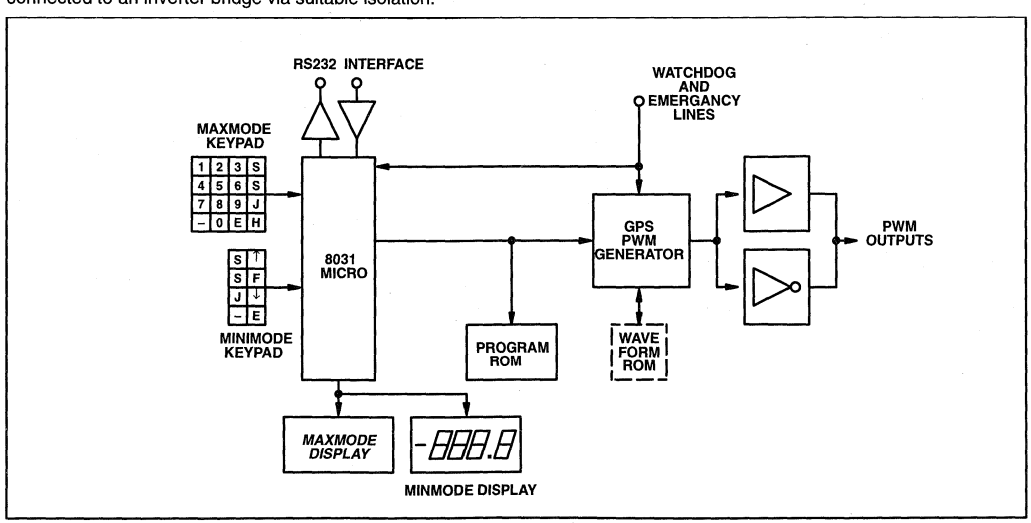


Fig. 1 PWM family demonstrator board block diagram

MV1817 APPLICATIONS

PACKET 31 RECOVERY

Introduction

MV1817 can be used for packet 31 data recovery simultaneously with normal page reception via the two page acquisition circuits, and in addition to packet 8/30 and packet 29 reception.

In MV1817, there are eight acquisition circuits dedicated to packet 31 reception, one for each of the eight magazines in which packet 31 data could be transmitted.

Because these packets might be transmitted at a very high rate (potentially) much faster than data could be read from the normal memory via the I^2C bus), the received data from each of the packets is written to a single memory location, so that simple external hardware can be used to assemble the memory data nibbles into bytes, and then write the bytes sequentially to a suitable buffer. The output data from this buffer can be read by a computer or other system with appropriate decoding software.

The relevant address for packet 31s from each magazine are shown in Table 1. they are all in store 00.

Magazine	EBU Channel	Hex Byte Address	RAS Address	CAS Address
0	8	10	002	000/1
1	9	11	002	002/3
2	A	12	002	004/5
3	B	13	002	006/7
4	C	14	002	008/9
5	D	15	002	00A/B
6	E	16	002	00C/D
7	F	17	002	00E/F

Table 1. Address for the eight acquisition channels

Description of the MV1817 DRAM signals

Fig. 1 shows the basic signals from MV1817 that are used to control the external hardware. Data bytes are written to the DRAM as two four bit nibbles using standard page mode signals. A normal memory cycle has a $\overline{RAS}$ pulse and two $\overline{CAS}$ pulses to read/write the eight data bits.

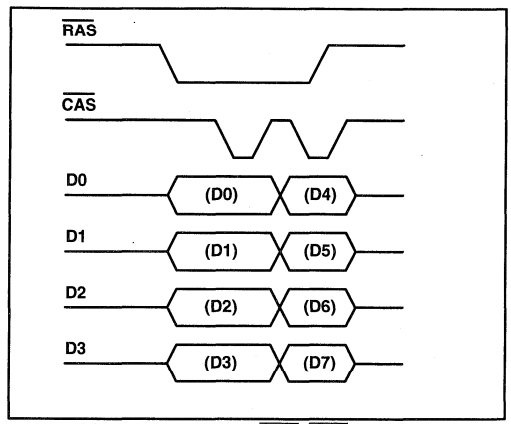


Fig. 1. DRAM signals $\overline{RAS}$, $\overline{CAS}$ and Data

Description of the Packet 31 recovery circuits

The logic proposed in this Application brief is intended as a preliminary guide to what would be needed in a real application. The circuits shown have not been tested and no guarantees are given as to their suitability for any particular application,

It is important that logic circuits to work with MV1817 are based on an advanced CMOS logic family, as some signals described in this brief can have separations of as little as 9ns. The D-types in particular therefore need set up times for the data input with respect to the clock, of better than about 6ns (dependent on logic delays)

The FIFO buffer shown is a generic 64 x 9 type. The speed rating for this device will probably be dependent on the output data rate required, since the input rate is relatively low, being at maximum the standard teletext byte data rate of 867 · 1875 kbytes/sec. Other FIFO devices such as 2048 x 9 should be equally suitable, and may make the system design easier.

With reference to Fig. 2 and 3, the leading edge of $\overline{RAS}$, and the four edges, A, B, C, and D on $\overline{CAS}$, are used to control the latching of data from D<0:3>, addresses from A<0:9> and the latching/clocking of data into/through a FIFO buffer.

A D-type is used to latch the state of the address lines at the leading (falling) edge of $\overline{RAS}$. If they are all low except A1, a logic 1 is held on the $\overline{Q}$ output. Edges B and D (Fig. 2) are used to clock the state of $\overline{RAS}$ through a second D-type to produce 'RC1', while a third D-type uses edges A and C to latch the state of 'RC1', generating 'RC2'.

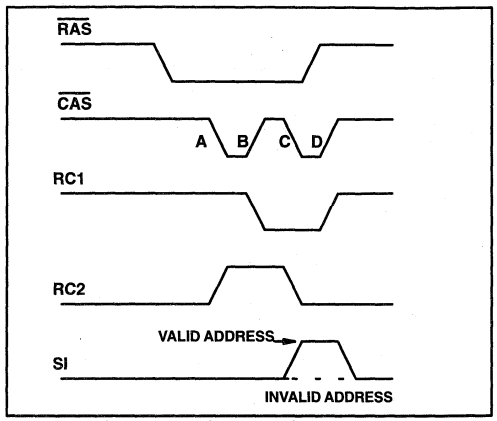


Fig. 2.Generation of SI pulse from DRAM signals.

If address lines A4 through A9 are also low during the CAS cycles, an active low signal VALID ADDRESS is produced. When NORed together with VALID ADDRESS, RC1 and RC2 produce the conditional 'SI' pulse which loads data into the FIFO on its leading (rising) edge, and clocks it through the FIFO on the trailing (falling) edge. A quad D-type (74AC175) is used to latch the first data nibble using edge 'B' of the CAS signal. This allows the whole data byte (D<0:7>) to be presented to the FIFO inputs at the rising edge of SI.

Address decoding

As detailed in Fig. 3, the address decoding from A<0:9> during RAS and CAS, will write packet 31s from any one of the eight addresses 10 - $17_{hex.}$ into the FIFO.

These addresses correspond to magazines 0 - 7 respectively. If data from only one magazine is required, address lines A3, A2 and A1 need to be appropriately decoded during CAS, and the decode ANDed with the other parts of the CAS address.

With the circuit as shown, the magazine number for any particular byte(s) of data can be latched during either CAS cycle from A<3, 2, 1> and presented to the microprocessor via separate logic.

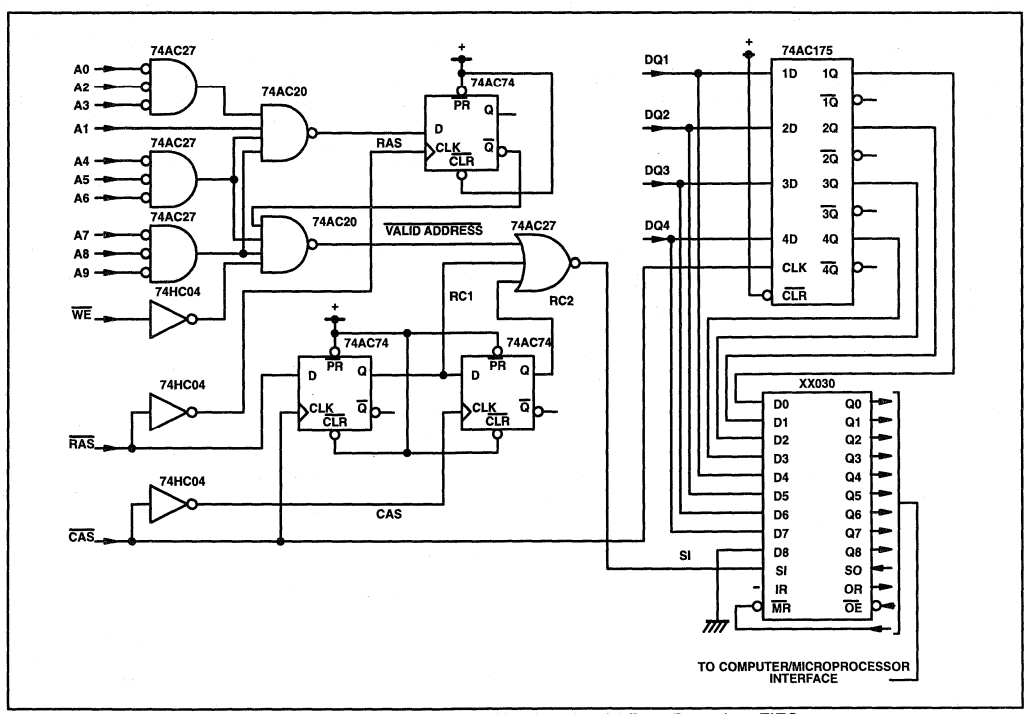


Fig. 3 Outline circuit to latch and load packet 31 Data Bytes into FIFO

Further information

Detailed timing information for the DRAM signals is available in the Datasheet. Reference should be made to these figures to ensure that adequate timing margins are allowed.

Note

This Application Brief also applies to MV1816/18/19.

THE VPS/PDC RECORDING FUNCTION

OUTLINE RECOMMENDATIONS FOR SOFTWARE IN VCRs USING THE MV1820 FAMILY

1. LABEL MATCHING

a. How Many Labels?

The PDC data in Format 2 packet 8-30s, is protected against errors by 8/4 Hamming encoding. This protection allows for the correction of a one bit error in any of the words in the message. Detection of uncorrectable errors caused by two errors in one word, will cause the whole packet to be rejected. This protection usually ensures that a message is either received correctly or is abandoned without generating an interrupt or writing data to the I^2C registers.

However, for maximum reliability, we recommend that at least two matching labels should be read from MV1820/21, before any action is taken. For VPS labels, where the level of error protection is not as good as PDC, five consecutive matching labels are recommended (ARD/ZDF Technical Guideline 8-R2, part IV -101 9.1/9.2)

b. Label Content

The last two (VPS five) consecutive labels in any particular LCI (channel) should be identical, i.e. the same as each other. This means that the labels must all be the same in every byte. If any byte is different (but see section 4), even a byte that is not relevant to the particular application such as the sound status bits, then all but the last label should be discarded, and the checking re-started.

c. Consecutive Labels

Consecutive – following continuously – means the last two actual labels received by MV1820/21 in a particular channel, whether they are received at 40 millisecond intervals, 200 millisecond intervals, 1 second intervals, or even longer intervals.

2. VPS/PDC LABEL TRANSMISSION/RECEPTION RATES

a. Overview

VPS programme labels are transmitted in line 16 of every frame, therefore there are (under normal conditions) 25 per second. There is a restriction to a maximum of five packet 8-30s per second of either format.

Normally, packet 8-30 format 1 (8-30-1) which carries the time and date, is transmitted once per second just prior to the change of each second (but can be transmitted at a faster rate). This leaves reception space for up to four other packet 8-30s of a different format. These five time slots could legitimately have any combination of format 1 and format 2 packet 8-30s. For instance, all five could be format 1, or all five could even be format 2s with the same channel (LCI).

Designers should note that very poor reception conditions, or even erroneous transmissions, might cause the loss of a significant proportion of the packets at the receiver, resulting in a reception rate of only one packet every few seconds.

b. Timer/PDC Mode Switching

PDC software should not rely on receiving packet 8-30s at any particular rate, but should evaluate the contents of a packet with respect to the previous packet. Inevitably though, there will be a reception rate at which the software must decide that there are insufficient packets to rely upon for accurate timing. This rate is probably about one packet per LCI per ten seconds, since that would still allow three packets to be received during any 30 second period, and should therefore guarantee that the start of a programme would not be missed.

Reception rates of less than one per ten seconds should therefore cause the system to switch into timer mode. To avoid frequent switching between modes if reception is intermittent, it would be sensible to provide some hysteresis in the switching. Therefore to switch back to PDC control from timer mode, should require a better reception rate, such as one label per LCI per two seconds.

c. VPS Reception

VPS packets are transmitted at 25 per second, which is anything from 5 to 25 times faster than packet 8-30-2s. Similar rules for mode switching need to be applied when receiving VPS, except that because the packets are transmitted much faster, the rules need to be suitably adapted.

For mode switching, a suitable gap might be one second without any VPS labels to enter timer mode, and one or two good labels to re-enter VPS mode.

3. THE 30 SECOND RULE

a. Recording Start (see also 4.a)

The 30 second rule states that the broadcaster should start the labels for any particular programme about 30 seconds before the programme itself starts. This is to allow time for VCRs that might be channel scanning, to find and check the labels and then enter RECORD mode without missing any of the programme.

If a VCR is not scanning other channels, then it should see the very first label that matches. It could start a 30 second timer so that it actually starts recording exactly on the start of the programme, but because of the difficulty of making the timer correct when the VCR is scanning other channels, we recommend that:

as soon as two consecutive and identical labels have been received, recording should be started immediately, if the labels match the user defined label.

This may record slightly early if the VCR is not scanning

other channels, but this may be easier for the software than trying to guess when to start if it has missed the label change point for any reason.

b. Recording Stop (see also 4.b)

The 30 second rule means that if the labels for one programme start early, the labels for the previous programme may also finish 30 seconds early, therefore VCRs must not stop recording immediately after a label change.

When the VCR is recording, it cannot be scanning other channels, therefore it should receive the first label of the next programme. Assuming that this label does not match any from the user programmed list, the software should start a 30 second timer as soon as a non-matching label is received.

After another identical label is received (in the relevant LCI), the current programme is confirmed as completed, and the label is deleted from memory. If another identical label is not received, the 30 second timer is repeatedly restarted until two identical labels (not matching the user label) are received. Recording is only stopped after the 30 second count-down has been completed.

LCI	LABEL	MATCH	ACTIONS		
0	19/2 08:00	Yes	Continue recording		
0	19/2 10:30	No	Note 1st new label	Continue Recording	Start 30s Count-down
0	19/2 10:30	No	Note 2nd new label	Continue Recording	Continue Count-down
			Delete 19/2 08:00 label from memory		
X	X	X	Continue recording until count-down completed		
1	19/2 08:00	Yes	Continue Recording		
1	19/2 08:01	No	Note 1st new label	Continue Recording	Start 30s Count-down
1	19/2 08:00	Yes	Note another 1st label	Continue Recording	Abandon Count-down
1	19/2 08:00	Yes	Note 2nd label Label matches that in memory. No change of action required.	Continue Recording	

Note that providing the system is still in PDC mode ($\geq$1 packet per 10 secs.), the time between received packets is irrelevant and therefore not shown in this table.

Table 1. Examples of two reception sequences with recommended actions

4. PRF and MI

These bits are proposed for addition to the PDC specification this year (1993). At the time of writing they are not believed to be in use anywhere in Europe. Software following the rules suggested in this document should always fail safe if these new facilities are not implemented: recording start and stop may include extra material, typically 30 seconds at each end of the recording.

a. Prepare to Record Flag

The Prepare to Record Flag, PRF, is intended to denote at its change from one to zero, the immediate start of the television programme. Providing the rest of the packet data is unchanged (and is in the same LCI), the software should act immediately on the information given by this bit – it should not wait for two identical labels with the PRF bit changed to zero.

In the event of packet reception problems around the time of a programme start signalled by PRF, the maximum delay in starting the VCR should be 10 seconds, after which timer mode should be applied.

LCI	PRF	LABEL	MATCH	ACTIONS	
3	X	19/2 08:00	No		
3	X	19/2 08:00	No		
3	1	19/2 10:30	Yes	Note 1st new label	
3	1	19/2 10:30	Yes	Note 2nd new label.	Start Record–Pause
3	1	19/2 10:30	Yes		Hold Record–Pause
3	1	19/2 10:30	Yes		Hold Record–Pause
3	0	19/2 10:30	Yes		Start Recording
3	0	19/2 10:30	Yes		Continue Recording

Table 2. Example of recommended actions when PRF is in use

b. Mode Indicator

The mode indicator (MI) bit has a similar effect to PRF in that when set to one, it denotes that the end of a television programme takes immediate effect upon the change of label within a particular LCI. However, unlike PRF, the software should not stop recording immediately, but after the reception two consecutive and identical labels, in the same LCI, that are different to the matched label. Essentially this removes the need to start a 30 second count-down timer, but not the need to validate a new label.

LCI	MI	LABEL	MATCH	ACTIONS		
2	1	19/2 08:00	Yes		Continue Recording	
2	1	19/2 08:00	Yes		Continue Recording	
2	X	19/2 10:30	No	Note 1st new label	Continue Recording	Do not start 30 sec. count-down
2	X	19/2 10:30	No	Note 2nd new label	Stop Recording	Delete 19/2 08:00 label from memory

Notes: In all the tables, an 'X' indicates a 'don't care' condition. The values shown for LCI are not important except that they do not change.

Table 3. Example of recommended actions when MI is in use

AN168

TV/SATELLITE SYNTHESISERS - BASIC DESIGN GUIDELINES

EXTERNAL NOISE PROBLEMS

I²C BUS RADIATION PROBLEMS

The main problem when designing PCBs using any I²C device is that data and clock are always being transmitted and fed to the transceivers. This can lead to problems with radiation unless suitable precautions are taken.

Coupling from the SCL and SDA lines can often occur where these lines are long tracks leading to the synthesiser. The SCL and SDA lines pose particular problems as clock and data are always present on the I²C databus, regardless of whether the synthesiser is being addressed or not. These can couple into the synthesisier through any of the pins; it is therefore important to ensure that all pins are decoupled where possible. Unused ports should be taken to ground. Small decoupling capacitors may be placed directly on the pin to cut radiation into ports.

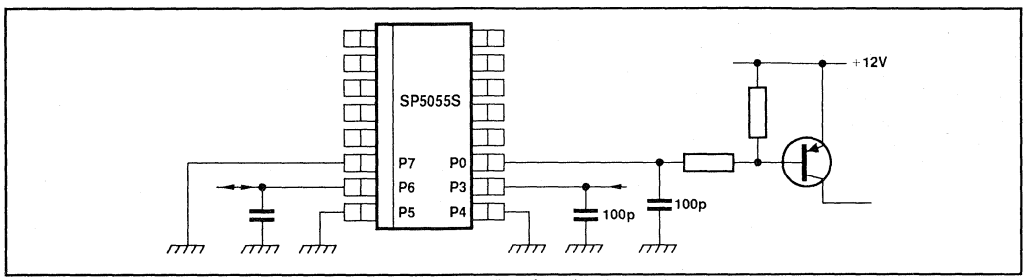


Fig.1 Decoupling/grounding of used and unused ports

I²C BUS LINE FILTERING

I²C bus specifications permit a maximum of 400pF on the SDA andSCL lines. This figure refers to the maximum total capacitance present on the bus so therefore includes other devices. Most applications use a combination of 100pF decoupling capacitors on each line together with a series resistor of up to 100kΩ, depending on the clock rate.

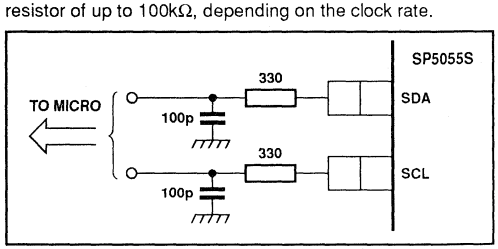


Fig.2 I²C bus line filtering

SYNTHESISER DECOUPLING

Supplies should be decoupled as close to the chip as possible. It is suggested that combination of 100pF and 100nF is used to give the best possible immunity against low and high frequency noise.

Layout

Care must be taken with layout to ensure that the supply rails are as short as possible and that no loops (either ground or supply) exist. If the layout permits, the V_{CC} line should not be routed near the loop filter.

Grounding

The synthesiser should be taken to a clean ground separate from the track used to ground any of the oscillators. If possible, shielding should be introduced between the oscillators and the synthesiser to ensure that no spurious coupling occurs.

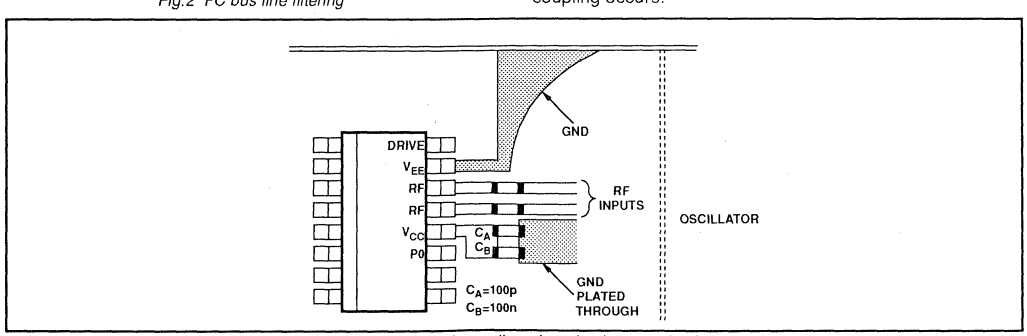


Fig.3 Layout and decoupling of synthesiser supply pins

VARACTOR LINE FILTERING

Special care should be taken with the varactor line. A low pass filter may be placed in the varactor line to prevent ripple being fed along the line and mistuning the oscillator. A typical application is shown in Fig.4.

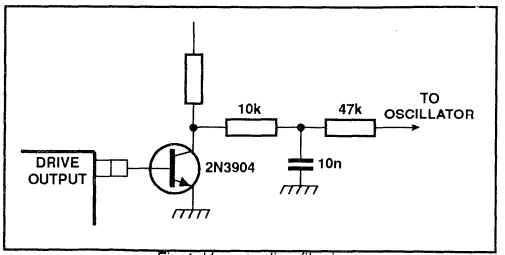


Fig.4 Varactor line filtering

The NPN transistor TR1, connected to the drive output, should be placed as close to the drive output pin as possible. The input to this transistor presents a very high impedance. Any length of track between the drive output of the synthesiser and the base of TR1 can act as an antenna which will feed unwanted signals into the transistor. To minimise this effect, a low value capacitor of, say 39pF may be connected between the base and collector of TR1 (as shown in Fig.5) without modifying the dominant loop characteristics.

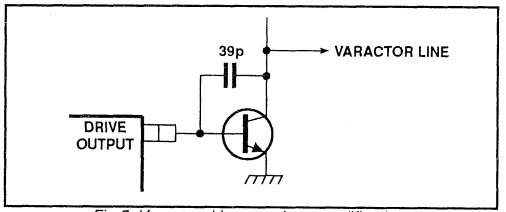


Fig.5 Varactor drive transistor modification

It is important that no other RF signals which may be present in the tuner, for example IF outputs, are routed anywhere near the synthesiser as they can also couple into the device.

All of the above suggestions are made in an attempt to achieve the best possible phase noise and sideband performance for the synthesised oscillator. Whilst a good synthesiser application does not guarantee good phase noise performance, a bad synthesiser application will almost certainly limit the overall performance of the tuner and degrade phase noise compared to that of a free-running oscillator.

CALCULATION OF LOOP COMPONENT VALUES

Applications Circuit (See Figure 6)

A typical synthesiser application circuit is shown in Figure 6. The optional additional filtering (referred to by Note 1 on this diagram) rolls off at a frequency well above the main loop filter. Its main purpose is to reduce any noise picked up on the varactor control line. Consequently its effect is ignored in this analysis. The following is a summary of the derivation of the basic design equations used to calculate the loop filter components.

Phase Detector Gain (See Figure 7)

The phase detector outputs pulses of current I_{CP} µA with a pulse frequency equal to the comparison frequency $\frac{\Omega in}{M}$ and width proportional to the phase error. These pulses are arranged by the loop filter so that the phase detector gain is given by:-

$$Kd = \frac{Icp}{2\pi} \ \mu A/radiation \qquad ....(1)$$

Charge Pump (See Figures 8 & 10)

The charge pump converts the current pulses into a voltage proportional to the phase error. It also forms the loop filter. The transfer characteristic depends on the order and type of filter used. For the 2nd order type 2 system shown in Figure 14, the transfer characteristic is :

$$F_2(S) = \frac{1+s\,\mathcal{T}_2}{s\mathcal{T}_1}$$

where $\mathcal{T}_1 = C_1$
and $\mathcal{T}_2 = C_1, R_2$

For the 3rd order type 2 system, the transfer characteristic is :

$$F_3(S) = \frac{(1+s\,\mathcal{T}_2)}{s\mathcal{T}_2\,(1+s\mathcal{T}_3)}$$

where $\mathcal{T}_1 = C_1$
$\mathcal{T}_2 = (C_1+C_2)\,R_2$
$\mathcal{T}_3 = C_3, R_2$

Choice of Filter Type (See Figure 9)

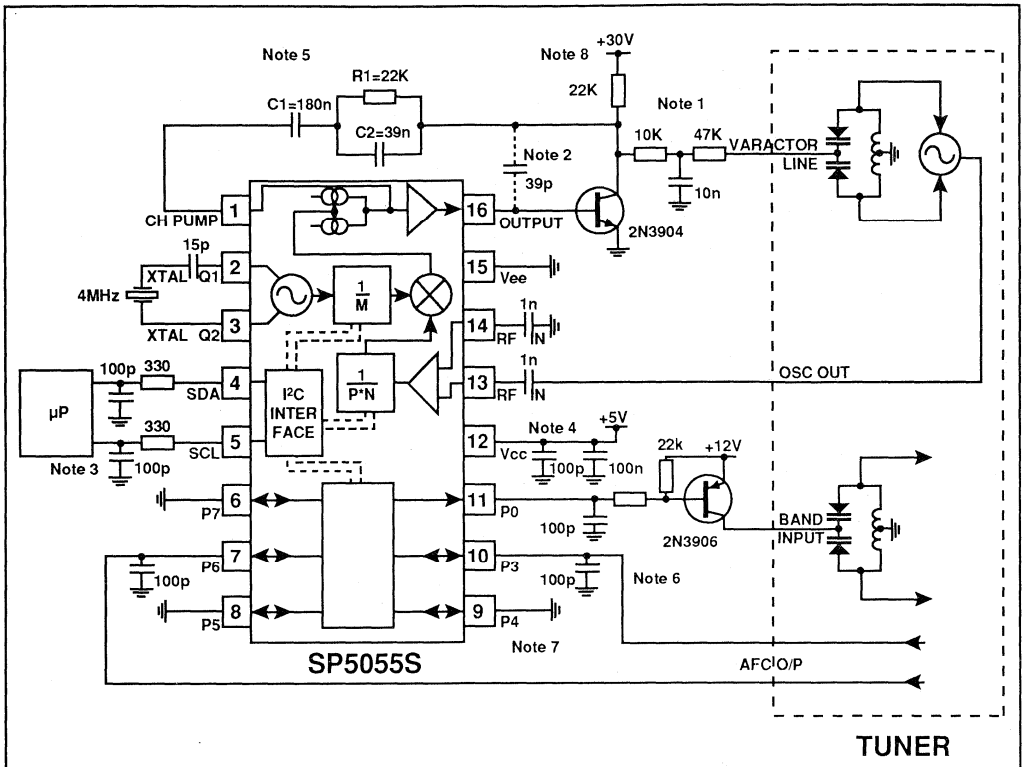
The 'type' is the power of s whilst the 'order' is the number of poles is the system transfer function. See Appendix 1 and Figure 9. The recommended filter is the 3rd order type 2 but since the system poles $^1/\mathcal{T}_1$ and $^1/\mathcal{T}_2$ are dominant over $^1/\mathcal{T}_3$ then the analysis and in particular the choice of suitable component values is considerably simplified by assuming that the filter is to be a 2nd order type 2. Once the natural frequency Wo and damping factors ζ are chosen based on the application, the values C_1 and R_2 can be calculated. The value of C_3 is found from an approximate derivation using 3rd order equations.

The main reason for choosing the 3rd order type 2 filter is that the extra pole improves the filter performance by reducing the ripple introduced by feed through of the phase noise detector pulses.

Choice of Natural Frequency and Damping Factor

When the synthesiser is reprogrammed, the application will usually require the VCO to settle to the new frequency within a specified time to a specified accuracy. Appendix 3 (Time Domain Response) shows that the time domain response to a frequency step is an exponentially decaying sinusoid. From this the natural frequency ωo can be calculated if we specify the settling time ts and the accuracy $\omega e/\Delta\omega$, provided we already know the damping factor ζ.

The damping factor must be chosen so that the system remains stable. For this the phase margin should be reasonably high say 0, > 45° or so. See Appendix 3 (Phase margin). The amount of 'overshoot' might also be used to estimate a value for ζ. See Figure 12.



Note 1 : Varactor line filter reduces ripple.
Note 2 : 39p capacitor reduces radiation into NPN base.
Note 3 : IIC bus filtering reduces transients.
Note 4 : Decouple Vcc rail at both high and low frequencies.
Note 5 : Choose appropriate loop filter components
Note 6 : Decouple unused output ports
Note 7 : Ground unused input ports
Note 8 : When the varactor line disable (OS bit) is set, the 30V supply can be varied to directly control the analog voltage to the varactor.

Fig.6 Typical IIC Synthesiser application

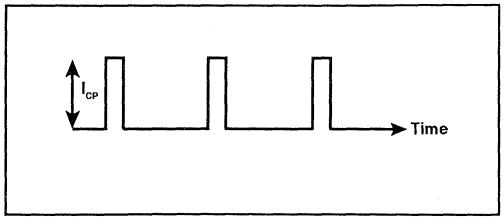


Fig.7 Phase detector current pulses

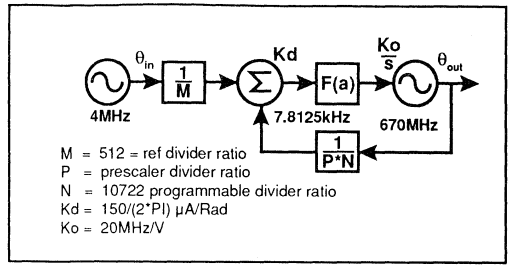


Fig.9 System block diagram

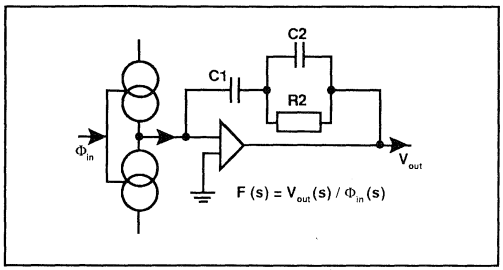


Fig.8 Phase detector and charge pump - third order type 2 loop

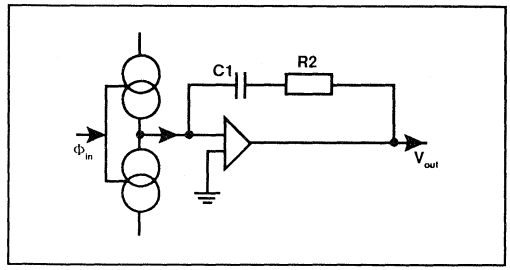


Fig.10 Phase detector and charge pump - second order type 2 loop

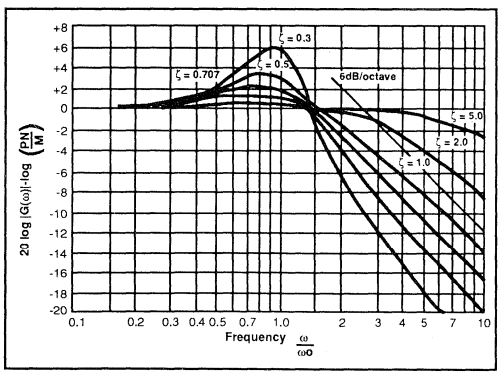


Fig.11

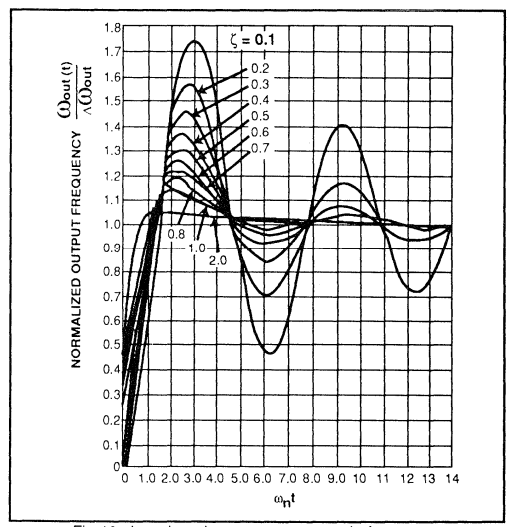


Fig.12 time domain response to step in frequency

Example (Selection of ωo and ζ)

Assume the reprogramming causes a frequency step of 512 MHz and we wish the VCO to settle to an accuracy of 5.12 Hz within 100 mS. If the phase margin is 70° then the values for ζ and ωo are:-

$$\zeta = \frac{\text{Tan}\varnothing}{2\sqrt{(1+\tan^2\varnothing)}} \quad \frac{= \text{Tan } 70°}{2\sqrt{(1+\tan^2 70°)}} \quad = 0.8$$

$$\omega n = -\text{Ln}\left[\frac{\omega e}{\Delta\omega out}\sqrt{1-\zeta^2}\right] = -\text{Ln}\left[\frac{5.12}{512\times10^6}\sqrt{1-0.8^2}\right]$$

$$\zeta ts \qquad\qquad 0.8 \times 0.1$$

$\therefore \omega n = 237$ rads/sec $= 37$Hz

In practice, a value of around 0.8 is reasonable (slightly underdamped) but a value of ωn = 1000 rads/sec would probably be more appropriate.

3rd Order Approximation

The system transfer function and open loop gain of the 3rd order type 2 system are given in Appendix 4. By manipulation of these formulae it is possible to show that $C_2 \approx C_1/5$ for all practical purposes. The alternative would be to do a complete line domain analysis as for the 2nd order system and then select the values of 3 parameters. This complexity is not necessary provided the time constants τ_3 is small compared to τ_1 and τ_2.

Design Formulae

Using the known values of ωo and ζ we have :-

$$C_1 = \frac{KdKo}{PN\omega_o^2}$$

$$R_2 = \frac{2\zeta}{\omega_o C'}$$

$$C_2 = C_1/5$$

Example (Selections of C_1, C_2 and R_2)

Suppose Kd = 150μA/rad, Kd = 20 MHz/volt, P = 8, N = 10,722 whilst ωo = 440 rads/sec and ζ = 0.87.

$$\therefore \quad C1 = \frac{150 \times 10^{-6} \times 20 \times 10^6 \times 2\pi}{8 \times 10722 \times 440^2 \times 2\pi} = 180.16\text{nF}$$

$$R2 = \frac{2 \times 0.87}{440 \times 180.6 \times 10^{-9}} = 21.9\text{K}\Omega$$

$$C2 = C_1/5 = 36.12\text{nF}$$

PHASE NOISE CONSIDERATIONS

Noise Sources (See Figure 13)

The noise present at the VCO output originates from three main sources.

(a) Phase noise in the reference oscillator θr
(b) Phase noise in the detector θd
(c) Phase noise in the VCO θo.

A small sinusoidal frequency modulation of the reference oscillator for example, with peak phase deviation of θr radius and modulation frequency ω_m would produce an output voltage of :-

$$V_r(t) = V\cos(\omega_r t + \theta_r \sin \omega_m t)$$
$$= V\cos(\omega_r t) - \frac{V\theta r}{2}\cos[(\omega_r+\omega_m)t] - \frac{V\theta_r}{2}\cos[(\omega_r-\omega_m)t]$$

See Figure 18. Many such sidebands will be contributed by random noise modulation mechanisms in the reference oscillator such as thermal and shatt noise.

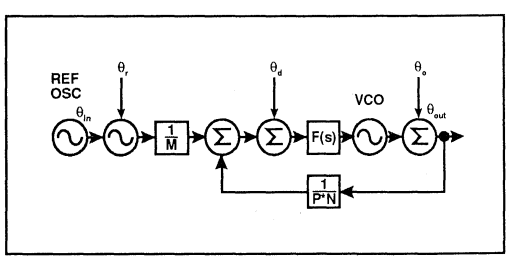


Fig.13 System diagram including phase noise

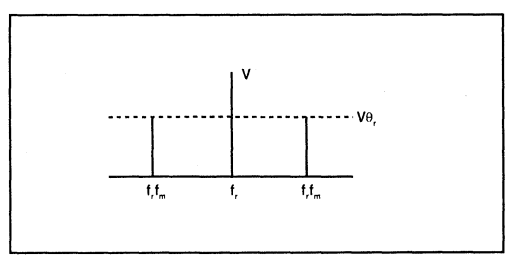


Fig.14 Noise sidebands

Noise at Synthesiser Output

The analysis of the System block diagram shows that the output noise spectrum is determined by :-

$$\theta_{out}(\omega) = A(\omega)\,\theta_r(\omega) + MA(\omega)\,\theta_d(\omega) + \left[1 - \frac{MA(\omega)}{PN}\right]\theta_O(\omega)$$

Where A(ω) is the system frequency response, described in Appendix 3 (system transfer charateristics) and shown in Figure 11.

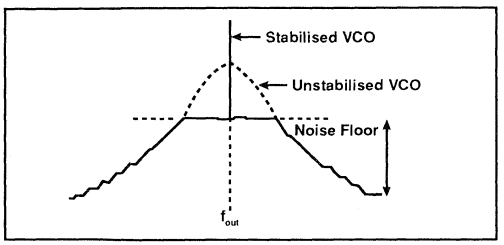


Fig.15 Output spectrum

Noise inside the Loop Bandwidth

The system frequency response inside the loop bandwidth is approximately given by :-

$$A(\omega) = \frac{PN}{M}$$

$\frac{PN}{M}$ This is just a statement that the system output frequency is times bigger than the reference frequency. As a result the noise at the output is :-

$$\theta_{out}(\omega) = \frac{PN}{M}\,\theta_r(\omega) + PN\,\theta_d(\omega)$$

Notice that the phase noise due to the phase detector is M times bigger than the phase noise from the reference oscillator. Thus the phase detector noise dominates. This noise appears as a plateau on the spectrum analyser display as shown in Figure 15. The inband VCO noise meanwhile has been suppressed by the loop filter. Thus the inband noise is determined by the prescaler and programmable divider ratios and by the noise floor of the detector.

$$\theta_{outINBAND} = PN\,\theta_d(\omega)$$

Noise outside the Loop Bandwidth

The noise outside the loop bandwidth is approximately given by :-

$$\theta_{outOUTBAND} = \theta_O(\omega)$$

This shows that any noise components due to the VCO having frequencies outside the loop bandwidth are <u>not</u> suppressed. Thus the phase noise outside of the loop bandwidth is determined largely by the performance of the VCO itself and no improvement of this can be gained by the use of the synthesiser. See Figure 15.

Example (Low Comparison Frequency Synthesiser)

A synthesiser such as the SP5510 operates with a comparison frequency of 7.8125 KHz. If an LO of 512 MHz is to be synthesised then :-

$$PN = \frac{512 \times 10^6}{7.8125 \times 10^3} = 65536$$

In practice, since the phase detector noise floor predominates, the reference oscillator noise may be ignored. If the phase detector noise floor is -130 dBc then the noise floor at the output is given by :-

θout = -130dBc + 20 log 65536 = -130 + 96.3 = -33.7dBc

Example (High Comparison Frequency Synthesiser)

The SP5058 has been designed to operate, with a high comparison frequency, typically 250 KHz. If an LO of 2.048 GHz is to be synthesised then :-

$$PN = \frac{2.048 \times 10^9}{250 \times 10^3} = 8192$$

If the phase detector noise floor is -140 dBc then the noise floor of the output is :-

θout = -140dBc + 20 log 8192 = -140 + 78.3 = 61.7dBc

High comparison frequency synthesisers are used in applications where the phase noise within the loop bandwidth is an important consideration such as scrambled satellite or cable systems using the double conversion principle. See Figure 16 (shown below).

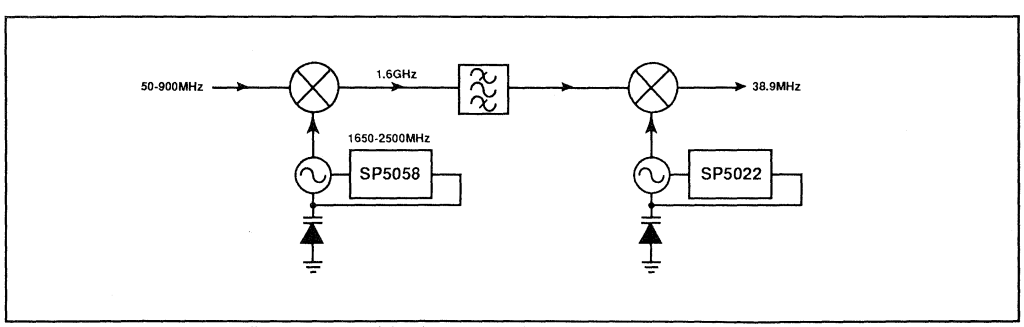


Fig.16 Example of double conversion from VHF/UHF frequencies to TV IF

USE OF VARACTOR LINE DISABLE (OS BIT) IN TUNER ALIGNMENT

In tuner manufacture, many of the wound components must be aligned to give the desired tilt factors, filter matching and correcting range for local oscillators and IF output.

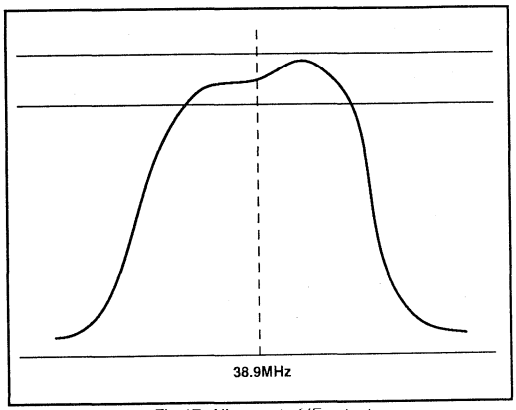


Fig.17 Alignment of IF output

This is a time-consuming process and is usually carried out by tuning the synthesiser to a number of different channels and aligning to these points (shown • on Fig.18).

Each time a new channel is selected, data must first be written to the synthesiser. In this example, 6 sets of data mus be sent from the micro to the synthesiser.

However, if the varactor line is disable bit OS is used, the varactor line voltage can be externally controlled. This allows the selected channels to be tuned without the use of a micro to address and program the device.

The varactor line disable facility is available on all GPS I²C bus synthesisers and also on I²C bus compatible 3-wire synthesisers such as the SP5024 and SP5054. With the latter devices, the varactor drive is disabled by applying a negative voltage to the ENABLE pin (pin 10) and sourcing greater than 350μA from the device. using this method of tuning can result in appreciable saving of test time.

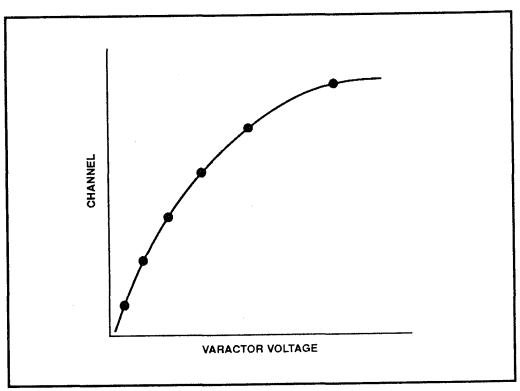


Fig.18 Varactor tuning curve

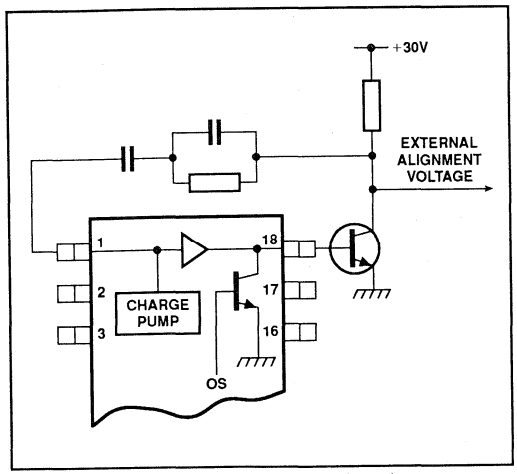


Fig.19 Application of external tuning voltage

APPENDIX 1 (NOTATION)

Description of symbols used.

θout (s) = VCO output phase

θin (s) = Reference oscillator phase

ωout (s) = VCO output frequency

ωin (s) = Reference oscillator frequency

Ko = VCO gain in rads/sec/volt

Kd = Phase detector gain = $\frac{Icp}{2\pi}$ Amps/rad

M = Reference divider ratio

P = Prescaler divider ratio

N = Programmable divider ratio

ωo = Natural frequency of 2nd order system in rads/sec

ζ = Damping factor of 2nd order system

S = Laplace frequency variable

$\underline{S}$ = S/ωo = Normalised laplace frequency variable

ω = ω/ωo = Normalised frequency

APPENDIX 2 (SYSTEM EQUATIONS)

System Transfer Characteristics (See Figure 9)

$$G(s) = \frac{\theta out\ (s)}{\theta in\ (s)} = \frac{\omega out\ (s)}{\omega in\ (s)} = \frac{KoKd\ F\ (s) / Ms}{1 + KoKd\ F\ (s) / PNs}$$

Open Loop Gain

$$G_{OL}\ (s) = KoKd\ F\ (s) / PNs$$

APPENDIX 3 (2ND ORDER TYPE 2 SYSTEM)

System Transfer Characteristics

$$G(s) = \frac{\frac{PN}{M}\left[1 + 2\zeta\Sigma\right]}{s^2 + 2\zeta s + 1} \quad \text{Where:-}$$

Natural frequency $\omega o = \sqrt{\frac{KdKo}{PN\mathcal{T}_1}}$, damping $\zeta = \frac{\omega o \mathcal{T}_2}{2}$, $\underline{s} = \frac{s}{\omega o}$

System Frequency Response (See Figure 15)

amplitude

$$A(\omega) = \frac{\frac{PN}{M}\sqrt{1+(2\zeta\underline{\omega})^2}}{\sqrt{(1-\underline{\omega}^2)+(\zeta\omega)^2}}$$

Phase

$$\emptyset(\omega) = \text{atan}(2\zeta\omega) - \text{atan}\left(\frac{\zeta\omega}{1-\omega^2}\right)$$

Time Domain Response (See Figure 12)

$$\omega out\,(t) = \Delta\omega out\left[1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\left(\cos\sqrt{1-\zeta^2}\,\omega nt - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\sqrt{1-\zeta}\,\omega nt\right)\right]$$

$\omega out\,(t)$ = output frequency at time t.

$\Delta\omega out$ = output frequency step called by reprogramming the divider

Settling Time

$$ts = \frac{-\text{Ln}\left[\frac{\omega e}{\Delta\omega out}\sqrt{1-\zeta^2}\right]}{\omega n\zeta}$$

Where $\omega e = \Delta\omega out - \Delta\omega out\,(ts)$ radians/sec is the error in the output frequency at time ts following a step adjustment of the output frequency of $\Delta\omega$.

Open Loop Gain

$$G_{OL}(s) = \frac{1 + 2\zeta\,\underline{s}}{\underline{s}^2}$$

Open Loop Frequency Responses

amplitude

$$A_{OL}(\omega) = \frac{\sqrt{1 + 2\zeta\,\underline{10}^2}}{\underline{\omega}^2} \qquad \text{Where } \underline{\omega} = \frac{\omega}{\omega_0}$$

phase

$$\emptyset_{OL}(\omega) = -\pi + \text{atan}\,(2\zeta\omega)$$

Phase Margin

$\emptyset_1 = \text{atan}\,(2\zeta\omega)$

where unity gain frequency $w1 = \sqrt{2\zeta^2 + \sqrt{4\zeta^4+1}}$

$$\therefore\zeta = \frac{\tan\emptyset_1}{2\sqrt{(1+\tan\emptyset_1)}}$$

APPENDIX 4 (3RD ORDER TYPE 2 SYSTEM)

System Transfer Characteristics

$$G(s) = \frac{KoKd}{Ms}\,\frac{(1+s\mathcal{T}_2)}{s\mathcal{T}_1(1+s\mathcal{T}_3)} \Big/ \left(1 - \frac{KoKd}{PNs}\,\frac{(1+s\mathcal{T}_2)}{s\mathcal{T}_1(1+s\mathcal{T}_3)}\right)$$

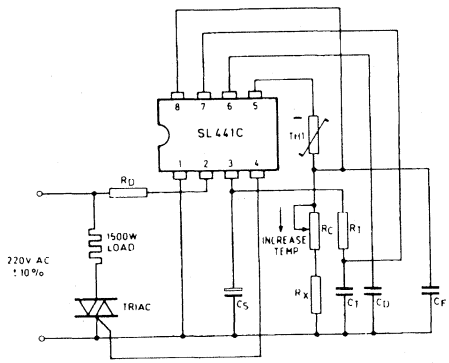
Open Loop Gain

$$A_{OL}(\omega) = \frac{KoKd}{PN\mathcal{T}_1 w^2}\sqrt{\frac{1+(+\omega\mathcal{T}_2)^2}{1+(+\omega\mathcal{T}_3)^2}}$$

$$\emptyset_{OL}(\omega) = -\pi + \text{atan}\,(\omega\mathcal{T}_2) - \text{atan}\,(\omega\mathcal{T}_3)$$

An Electronic Thermostat for Room Heaters using the SL441C

The circuit in Fig.1 has a sensitivity of nominally 100mV/°C. The width of the proportional control band is nominally 1.0°C and offers a good compromise between temperature stability and regulation performance. For potentiometer control characteristics see Figs.2 and 3.



SUGGESTED VALUES

R_D	8.2kΩ 5% 6W (less in air stream)	
R_C	22kΩ linear control potentiometer	
R_t	2.7MΩ	} Ramp period = 11 secs*
C_t	4.7µF 10V TANT	
C_f	47nF (filter if required)	
C_S	150µF 16V	
C_D	2.2nF ±10%	
Triac	TAG 250-400	
TH1	NTC thermistor. R_{25} = 10kΩ B = 4200. e.g. ITT KQ103	
R_x	6.2k ±5% fixed resistor or 10kΩ preset. See control characteristics Figs. 7 and 8	

* If on-off control is required, omit R_T and C_T and link pin 7 to pin 1.

*Fig.1 Application Circuit for Proportional Control System.**

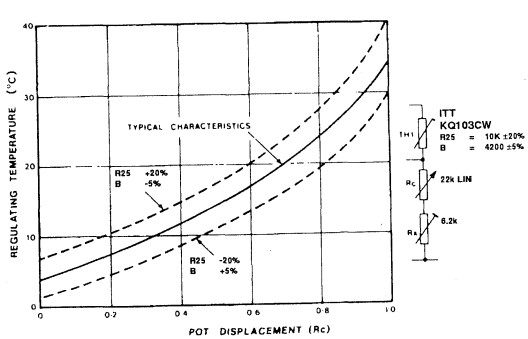


Fig. 2 Control Characteristics of Electronic Thermostat (mechanical calibration)

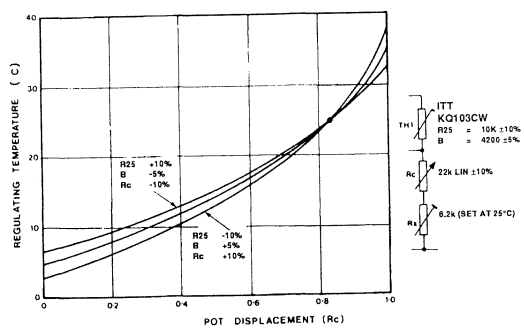


Fig. 3 Control Characteristics of Electronic Thermostat (electrical calibration)

AN147-1.0

System Design with the TDA2088

The TDA2088 is a phase control integrated circuit optimised for current feedback control of small universal motors such as are found in small power tools and food mixers. A derivative ot the TDA2086 design it has a guaranteed minimum l00mA negative triac gate drive capability, and is thus capable ot driving up to 40A triacs without pilot triacs or transistor buffers.

Figure 1 shows a typical application tor variable speed control of a small universal motor.

CURRENT FEEDBACK

Figure 2 shows the feedback arrangement from Fig.1 in more detail. Component values have to be determined empirically for individual motors but the following guidelines will help.

The power dissipation in R_3 obviously has to be kept low i.e. its value must be as low as possible, but to avoid significant speed errors from device to device the volt drop across R_3 under normal operating conditions should be >150mV so that the offset on Pin 1 (± 20mV max) does not affect the feedback.

The feedback and control currents are summed at pin 6 which can draw a bias current as high as 1μA. For reasonable consistency, $V_{in}/(R_2 + Z_{out})$ should be at least 10μA at the operating speed.

Loop compensation and the integration of the feedback current pulses are effected by the capacitor C. This component should be of good quality and low leakage since it must not load the current summing node. A time constant $(R_2 + Z_{out})$ C of 0.25s is probably a good starting point for most motors. Time constants of less than 60ms should not be attempted since the ripple on the feedback component will almost certainly cause instability.

The amount of current feedback is determined by the value of R_3 and the ratio of R_4 to $(R_2 + Z_{out})$. An easy procedure to use is to determine R_3, R_2 and Z_{out} from the considerations above, choosing a large value for R4 (very little feedback), then reduce R_4 till a satisfactory speed regulation performance is obtained.

Where variable speed operation is required it is often found that the optimum degree of feedback is different for different speeds. This problem can be reduced by using the variation in Z_{out} with control setting to alter the feedback ratio.

The circuit of Figs. 1 and 2 produces a characteristic where the feedback is at a maximum at mid-speeds and reduces at higher or lower settings. Fig.3 shows an arrangement where the amount of feedback decreases with increasing speed. Fig.4 is the converse case where feedback increases with increasing speed.

In applications where switched speeds are required (see Fig 5) then the feedback can be optimised for each speed by choosing the ratios of the resistors R_A: R_B, R_C: R_D, R_E: R_F,to give the desired speeds. and the values of R_A/R_B, R_C/R_D, R_E/R_F to give the desired feedback factors.

Fig 6 shows the most basic form of open-loop speed control with no current feedback.

Figs 7 and 8 show a pcb layout and component overlay for the schematic shown in Fig.1.

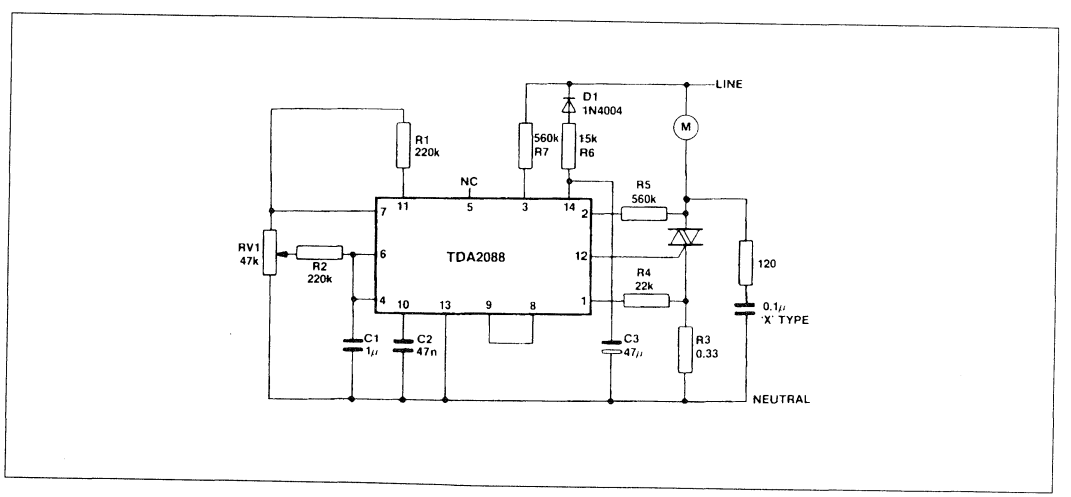


Fig.1 Universal Motor Speed Control Using Current Feedback

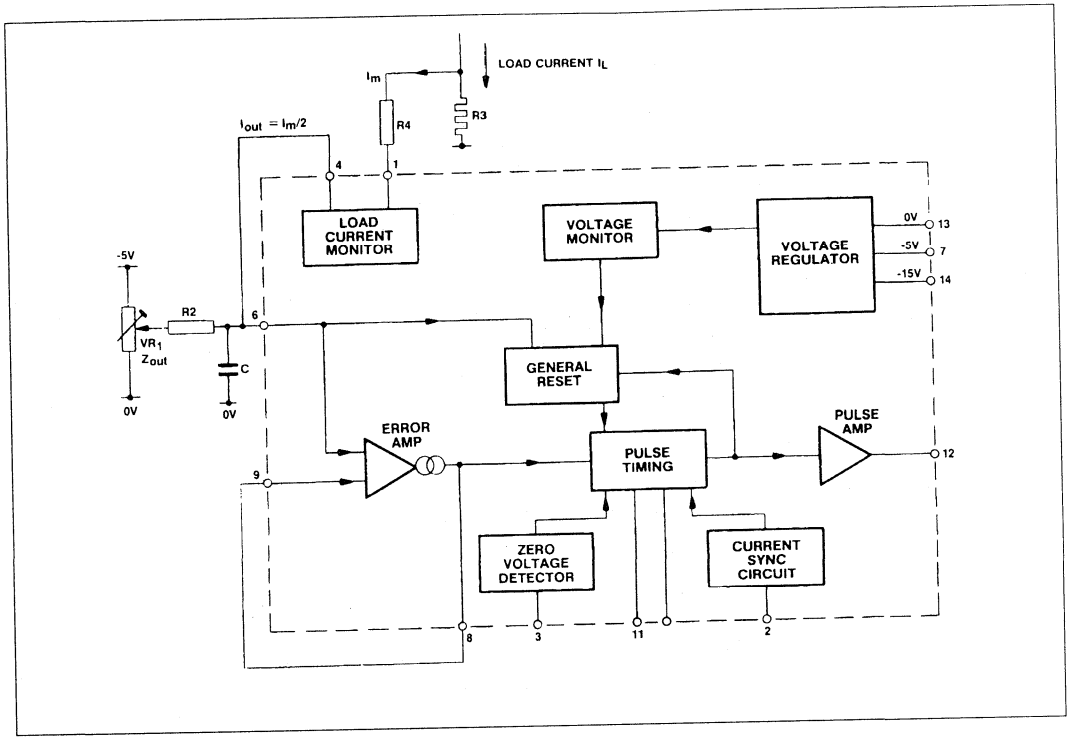


Fig.2 Feedback Arrangement

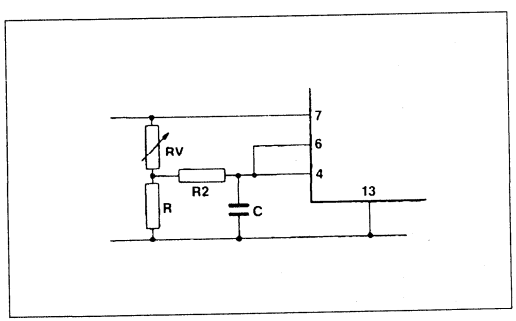


Fig.3

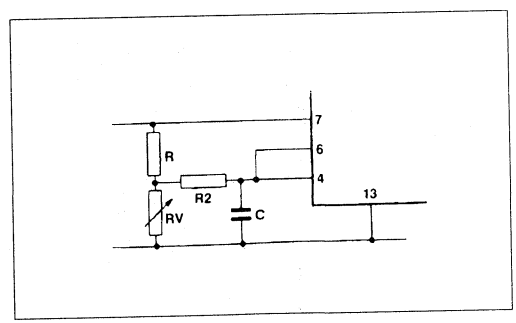


Fig.4

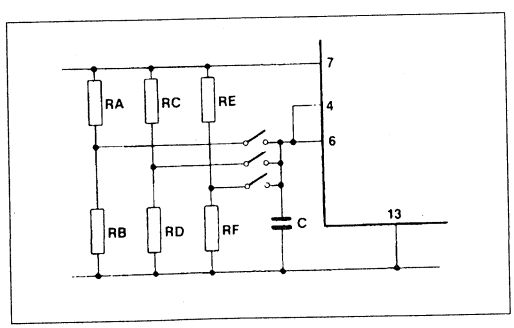


Fig.5

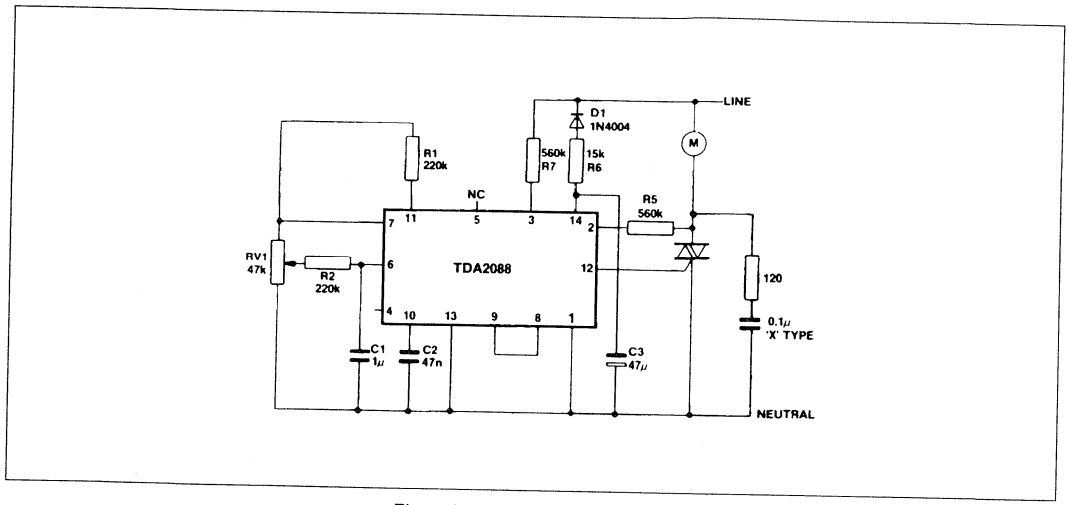


Fig.6 Open Loop Speed Control

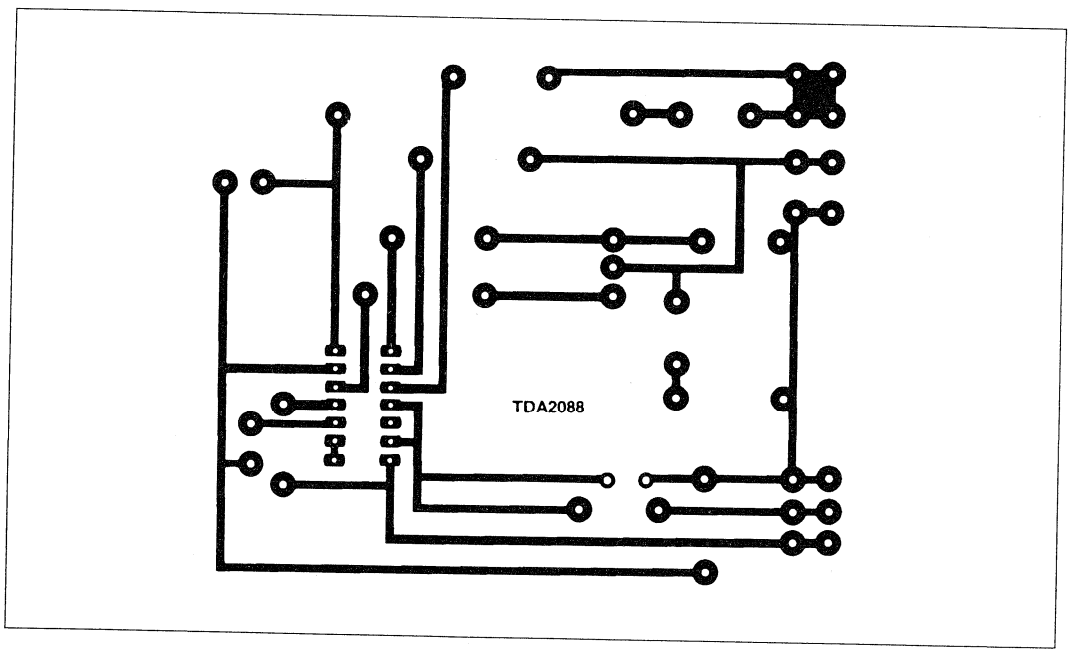


Fig.7 PCB Layout for Fig.1

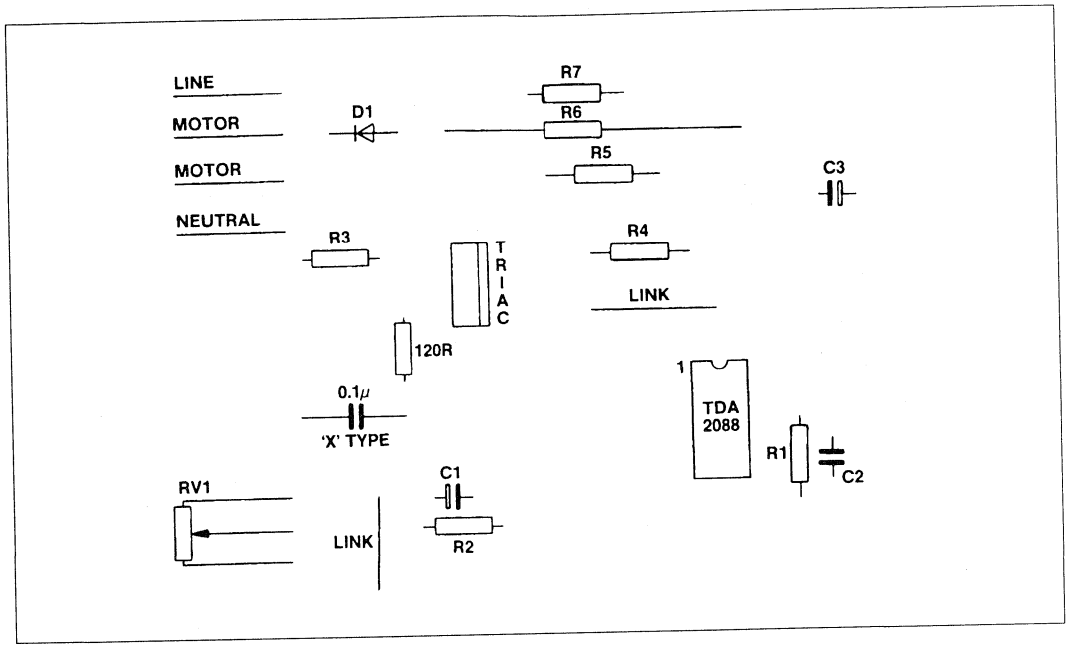
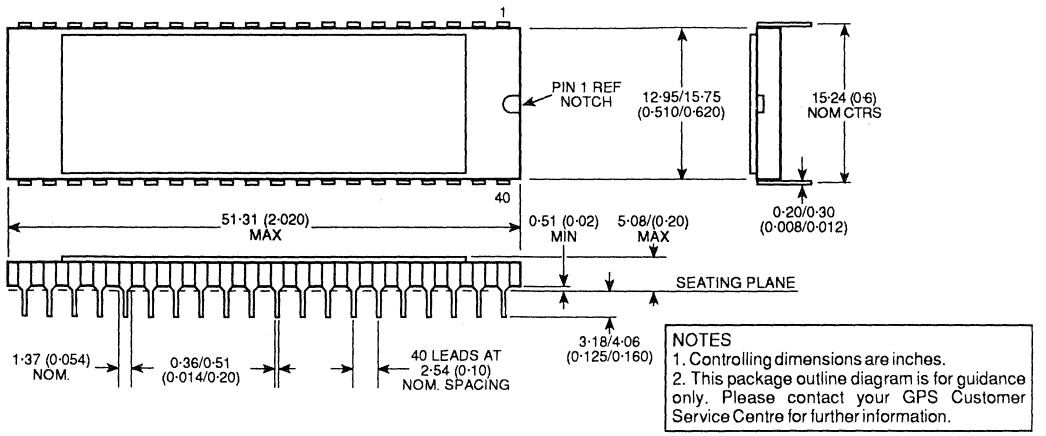


Fig.8 Component Overlay for Fig.1

Section 10
Package Outlines

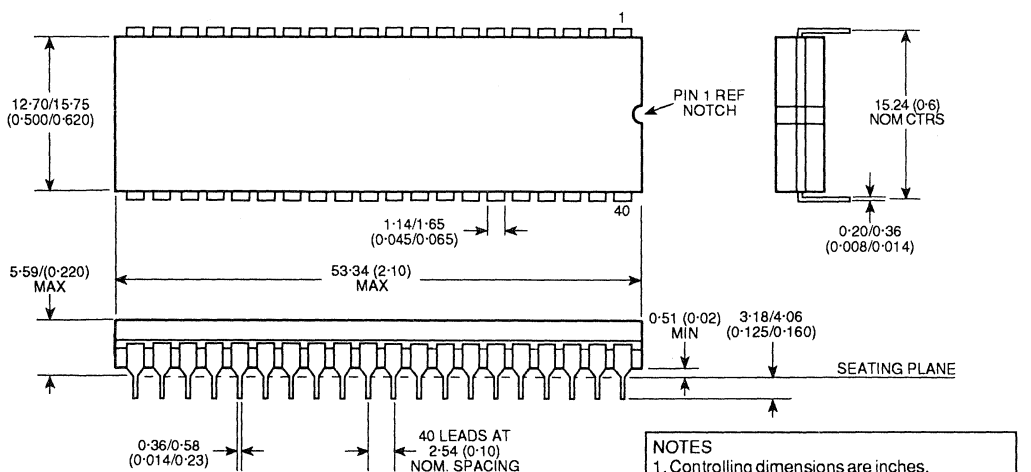
Dimensions are shown thus: mm (in).
For further package information, please contact your local Customer Service Centre.

GEC PLESSEY
SEMICONDUCTORS



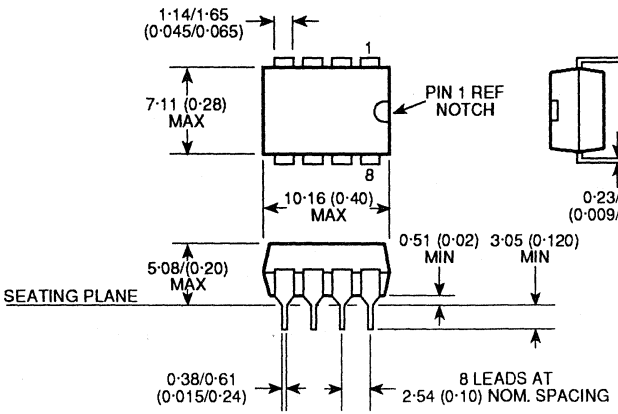
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

40-LEAD SIDEBRAZED CERAMIC DIL - DC40



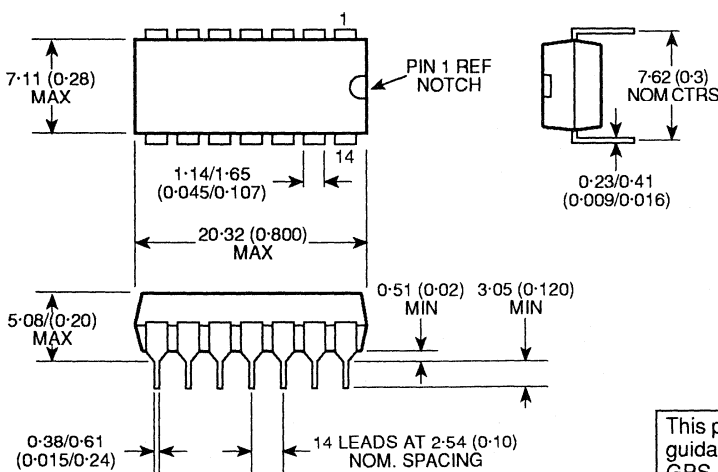
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

40-LEAD CERAMIC DIL - DG40



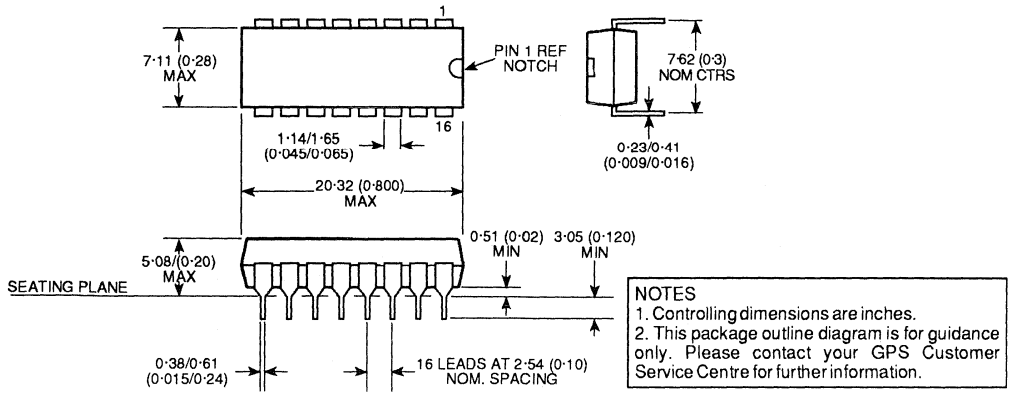
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

8-LEAD PLASTIC DIL - DP8



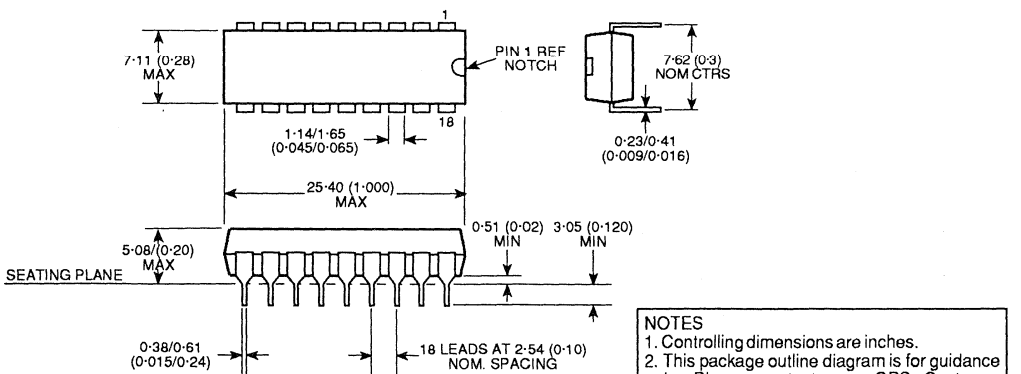
This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

14-LEAD PLASTIC DIL - DP14



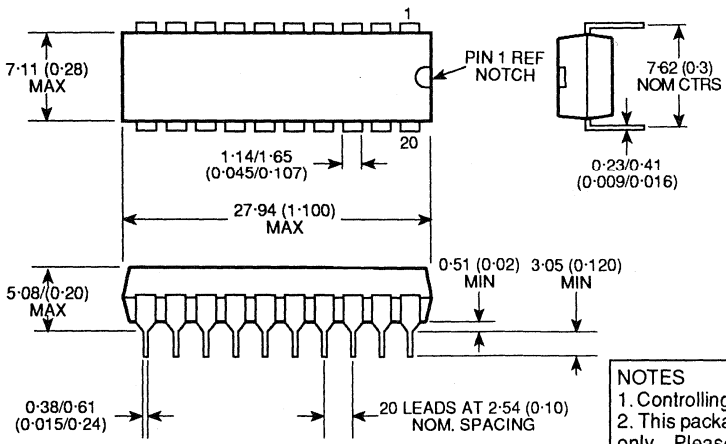
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

16-LEAD PLASTIC DIL - DP16



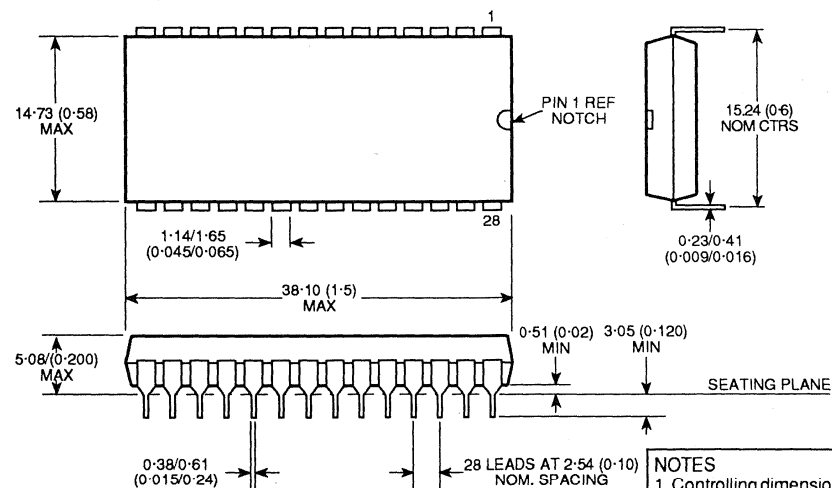
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

18-LEAD PLASTIC DIL - DP18



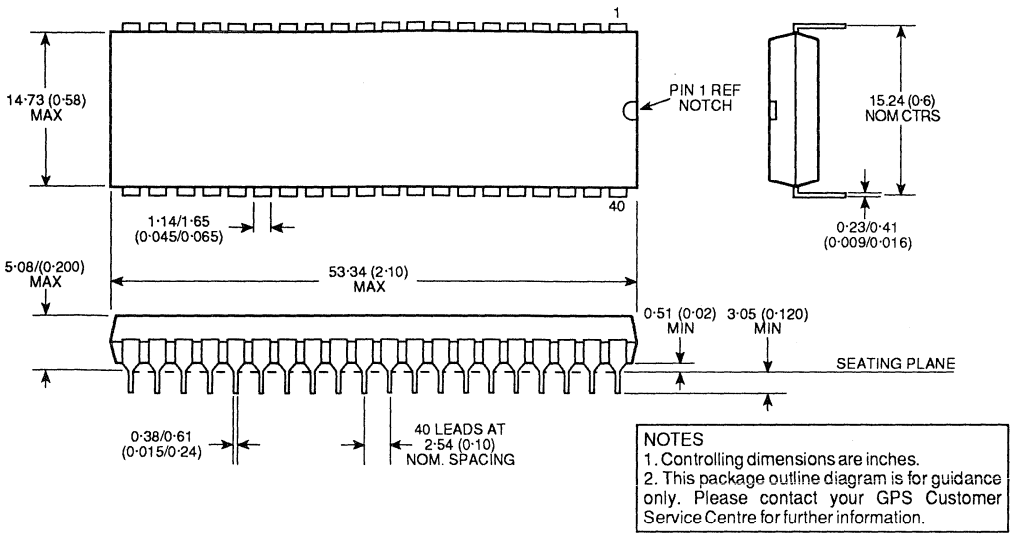
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

20-LEAD PLASTIC DIL - DP20



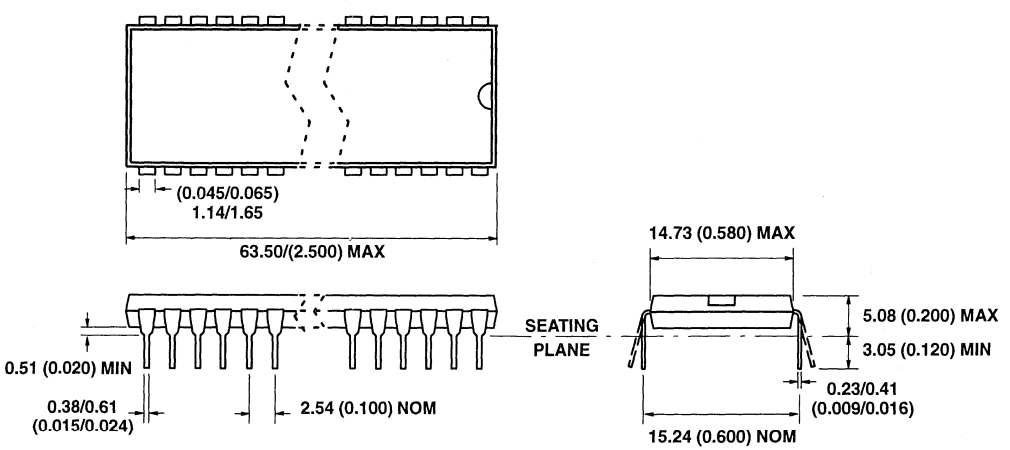
NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

28-LEAD PLASTIC DIL - DP28

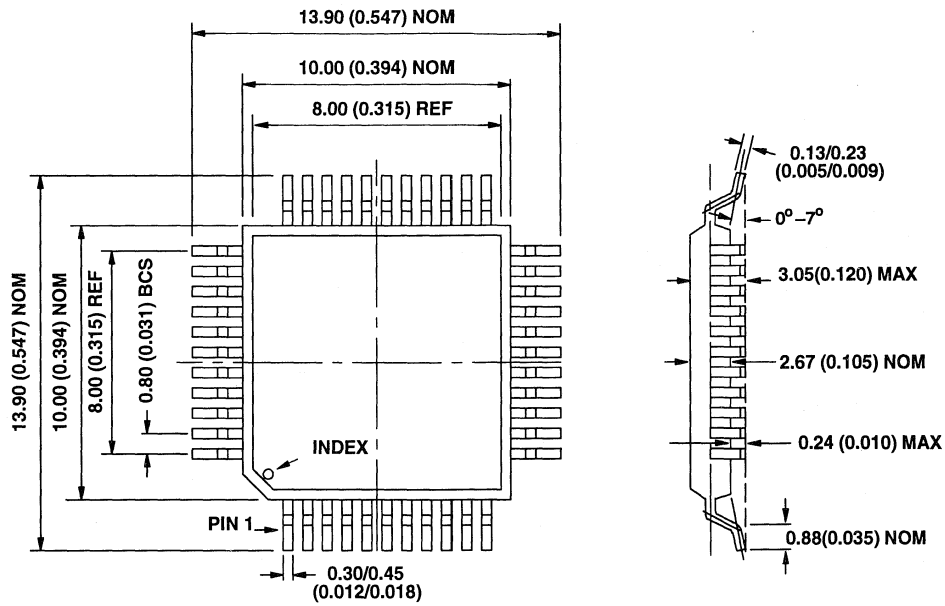


NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

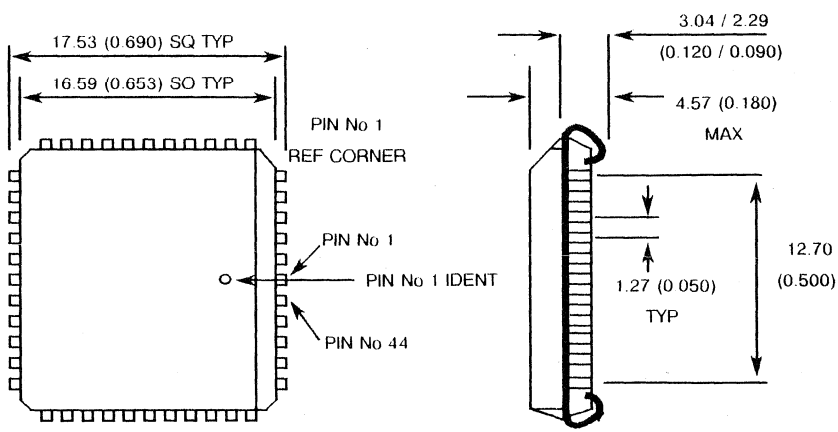
40-LEAD PLASTIC DIL - DP40



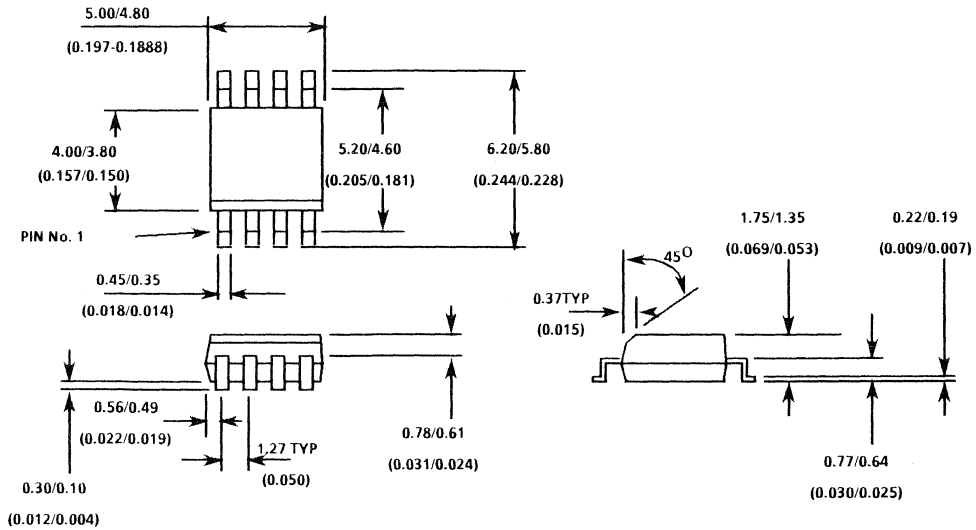
48-LEAD PLASTIC DIL - DP48



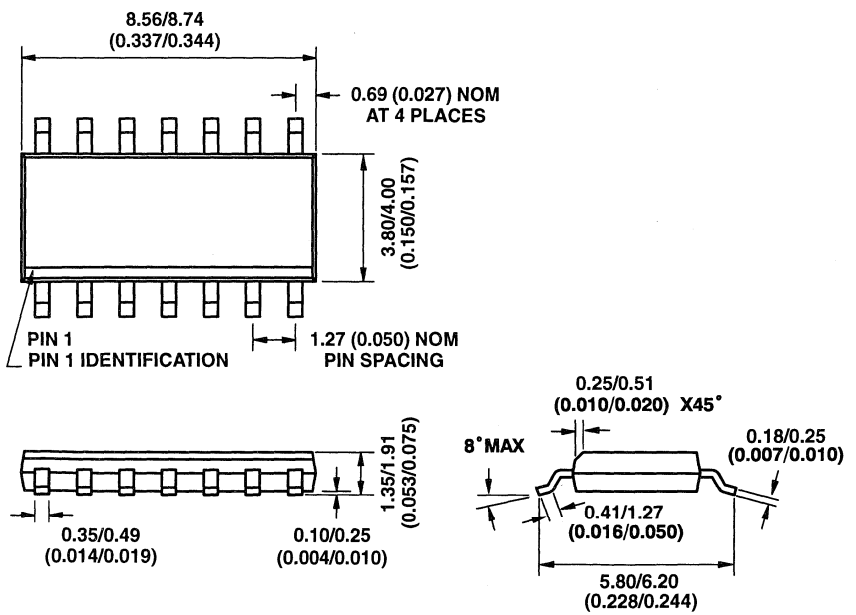
44-LEAD PLASTIC QUAD FLATPACK - GP44



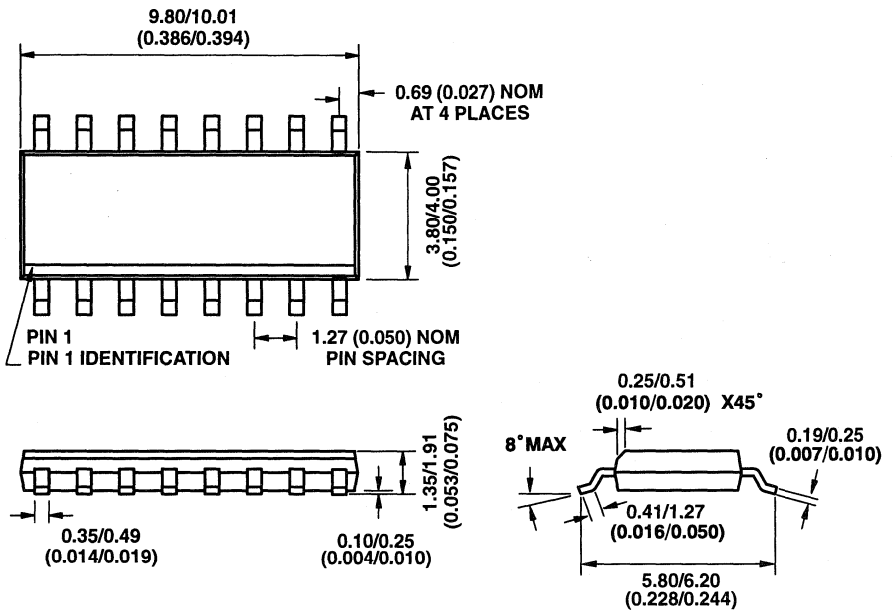
44-LEAD QUAD PLASTIC J LEAD - HP44



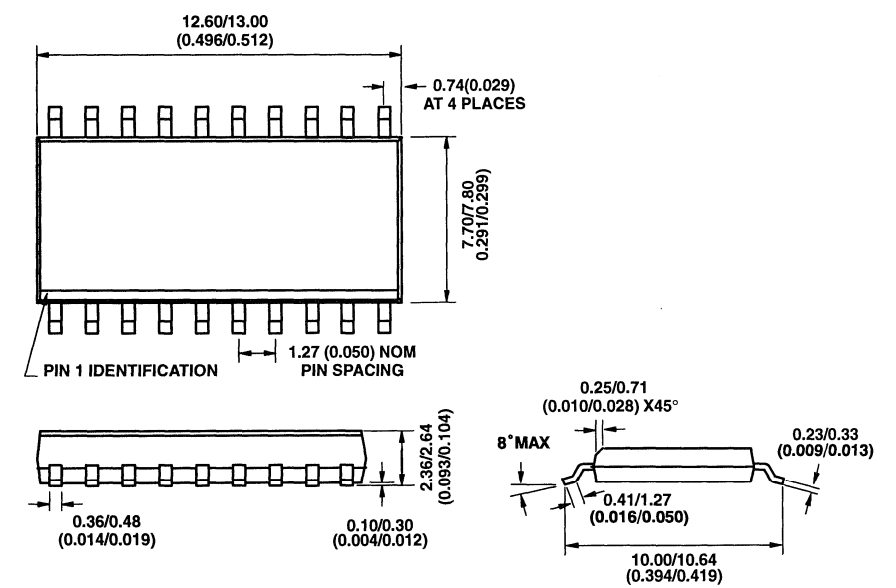
8-LEAD MINIATURE PLASTIC DIL - MP8



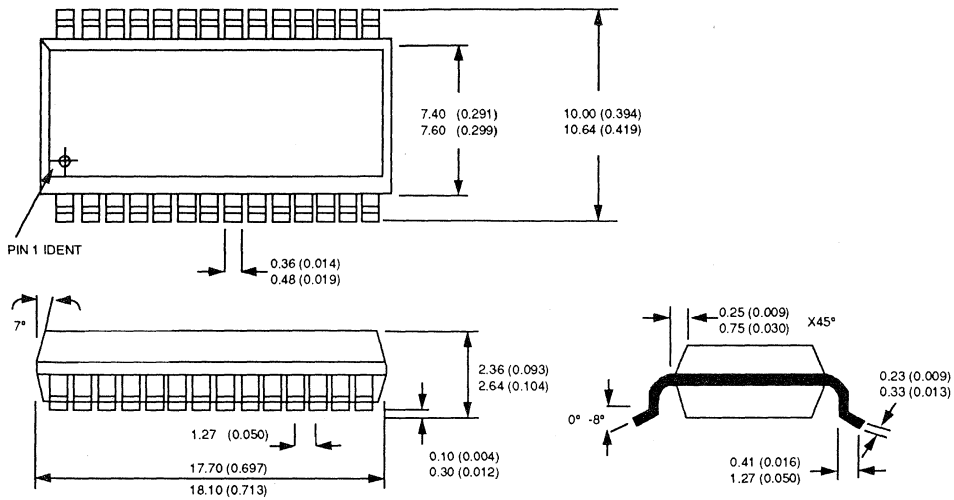
14-LEAD MINIATURE PLASTIC DIL - MP14



16-LEAD MINIATURE PLASTIC DIL - MP16



20-LEAD MINIATURE PLASTIC DIL - MP20



28-LEAD MINIATURE PLASTIC DIL - MP28

Section 11
GPS Locations

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ARIZONA/NEW MEXICO	4635 South Lakeshore Drive, Tempe, AZ 85282. Tel: (602) 491-0910. Fax: (602) 491-1219.
SOUTH CENTRAL	9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930. Fax: (214) 680-9753.
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	Shucho-Gu, CPO Box 7981, Seoul. Tel: 2 595 9101-6. Tx: K25981 KMLCORP. Fax: 2 595 9107.

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N AMERICA: Canada	**Alberta Microelectronics Center,** 3553 31st St., N.W., Calgary, Alberta T2L2K7. Tel: (403) 289-2043.
	Microstar Technologies, 7050 Bramelea Rd., #27A Mississaugo, Ontario L5SITI Canada. Tel: (416) 671-8111
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	Two Dedham Place, Suite 1, Allied Drive, Boston, Massachusetts 02026. Tel: (617) 320-9369. Fax: (617) 320-9383.
	2600 Michelson Drive, Suite 830, Irvine, CA 92715. Tel: (714) 852-3900. Fax: (714) 852-3910.
Colorado, USA	**Analog Solutions,** 5484 White Place, Boulder, CO 80303. Tel: (303) 442-5083.
Illinois, USA	**Frederikssen & Shu Laboratories, Inc.,** 531 West Golf Rd., Arlington Heights, IL 60005. Tel: (312) 956-0710.
UNITED KINGDOM	Cheney Manor, Swindon, Wiltshire SN2 2QW. Tel: (0793) 518000. Fax: (0793) 518411.
	Tweedale Way, Hollinwood, Oldham, Lancashire OL9 7LA. Tel: 061 682 6844. Fax: 061 688 7898.
	Doddington Road, Lincoln LN6 3LF. Tel: 0522 500500. Fax : 0522 500550.

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ALABAMA	**Electramark, Inc.,** 500 Wynn Drive, Suite 521, Huntsville, AL 35816. Tel: (205) 830-4400 Fax: (205) 830-4406.
ARIZONA	**Fred Board Associates,** 7353 E, 6th Avenue, Scottsdale, AZ 85251. Tel: (602) 994-9388. Fax: (602) 994-9477.
CALIFORNIA	**Gary Chilcote & Associates,** P.O. Box 1795, 1902 Quite Ranch Road, Fallbrook, CA 92028. Tel: (619) 728 7678.Fax: (619) 728 3738.
	Jones & McGeoy, 5100 Campus Drive, Suite 300, Newport Beach, CA 92660. Tel: (714) 724 8080. Fax: (714) 724 8090.
CONNECTICUT	**Stone Components,** 123 Commerce St., Clinton, CT 06413. Tel: (203) 669-4344. Fax: (203)669-9958.
FLORIDA	**American Micro Sales,** 1325 N. Congress Ave., Ste 204, West Palm Beach, FL 33401. Tel: (407) 689 3860.Fax: (407) 689 3168.
	American Micro Sales, 274 Wilshire Blvd., Ste 241, Casselberry, FL 32707. Tel: (407) 831 2505. Fax: (407) 831 1842.

American Micro Sales, P.O. Box 399, 1033 Rosetree Lane, Tarpon Springs, FL 34688/9. Tel: (813) 938 3073. Fax: (407) 831 1842.

GEORGIA **Electramark, Inc.,** 6030-H Unity Drive, Norcross, GA 30071. Tel: (404) 446-7915. Fax: (404) 263 6389

ILLINOIS **Micro Sales, Inc.,** 901 West Hawthorn Drive, Itasca, IL 60043. Tel: (708) 285-1000. Fax: (708) 285-1008.

INDIANA **Leslie M. DeVoe,** 4371 E. 82nd St., Suite D, Indianapolis, IN 46250. Tel: (317) 842-3245. Fax: (317) 845-8440.

IOWA **Lorenz Sales,** 5270 N. Park Place N.E., Cedar Rapids, IA 52402. Tel: (319) 377-4666. Fax: (319) 377-2273.

KANSAS **Lorenz Sales, Inc.,** 8645 College Blvd., Suite 220, Overland Park, KS 66210. Tel: (913) 469-1312. Fax: (913) 469-1238.

Lorenz Sales, Inc., 1530 Maybelle, Wichita, KS 67212. Tel: (316) 721-0500. Fax: (316) 721-0566.

MARYLAND **Walker Associates,** 1757 Gablehammer Road, Westminster, MD 21157. Tel: (410) 876-9399. Fax: (410) 876-9285.

Walker Associates, 169 Queen Anne Bridge Road, Mitchellville, MD 20716. Tel: (410) 249-7145.

MASSACHUSETTS **Stone Components,** 2 Pierce Street. Framingham, MA 01701. Tel: (508) 875-3266. Fax: (508) 875-0537.

Stone Components, 10 Atwood Road, Newburyport, MA 01950. Tel: (508) 462-1079.

MICHIGAN **Greiner Associates Inc.,** 15224 E. Jefferson Avenue, Grosse Point Park, MI 48230. Tel: (313) 499-1088. Fax: (313) 499-0665.

MINNESOTA **High Technology Sales,** 4801 West 81st Street, Suite 115, Bloomington, MN 55437. Tel: (612) 844-9933. Fax: (612) 844-9930.

MISSOURI **Lorenz Sales, Inc.,** 10176 Corporate Square Dr., Suite120, St. Louis, MS 63121. Tel: (314) 997-4558. Fax: (314) 997-5829.

NEBRASKA **Lorenz Sales,** 2801 Garfield Street, Lincoln, NE 68502. Tel: (402) 475-4660. Fax: (402) 474-7094.

HLM Assoc., 333 Littleton Raod, Parsippany, NJ 07054. Tel: (201) 263-1535. Fax: (201) 263-0914.

NEW HAMPSHIRE **Stone Components,** 436 S. Baboosic Lake Rd., Merrimack, NH 03054. Tel: (603) 429-3462. Fax: (603) 429-3462.

NEW YORK **HLM Assoc.,** 64 Mariners Lane, Box 328, Northport, NY 11768. Tel: (516) 757-1606. Fax: (516) 757-1636.

Regan Compar, 3301 Country Club Road, Endwell, NY 13760. Tel: (607) 754-2171 Fax: (607) 754-4270.

Regan Compar, 214 Dorchester Avenue, Syracuse, NY 13202. Tel: (315) 432-8232. Fax: (315) 432-8238.

Regan Compar, 37A Brookhill Lane, Rochester, NY 14625. Tel: (716) 271-2230. Fax: (716) 381-2840.

OHIO **Scott Electronics, Inc.,** 3131 S. Dixie Dr., Suite 200, Dayton, OH 45434. Tel: (513) 294-0539. Fax: (513) 294-4769.

Scott Electronics, Inc., 30 Alpha Park Drive, Cleveland, OH 44143. Tel: (216) 473-5050. Fax: (216) 473-5055.

Scott Electronics, Inc., 916 Eastwind Dr., Westerville, OH 43081. Tel: (614) 882-6100. Fax: (614) 882-0900.

Scott Electronics, Inc., 10901 Reed Hartman Hwy., Suite 301, Cincinnati, OH 45242. Tel: (513) 791-2513. Fax: (513) 791-8059.

PENNSYLVANIA/ NEW JERSEY **Metz-Jade Associates, Inc.,** 7 Wynnewood Rd, Suite 203, P.O.Box 276, Wynnewood, PA 19096. Tel: (215) 896-7300. Fax: (215) 642-6293.

TEXAS **Oeler & Menelaides, Inc.,** 8430 Meadow Rd., Suite 224, Dallas, TX 75231. Tel: (214) 361-8876. Fax: (214) 692-0235.

Oeler & Menelaides, Inc., 8705 Shoal Creek Rd., #103, Austin, TX 78758. Tel: (512) 453-0275. Fax: (512) 453-0088.

WISCONSIN **Micro Sales, Inc.,** 210 Regency Ct., Suite L101, Waukesha, WI 53186-0545.
Tel: (414) 786-1403. Fax: (414) 786-1813.

CANADA **GM Assoc. Inc.,** 7050 Bramalea Road, Mississauga, Ontario L5S 1T1 (Toronto).
Tel: (416) 671-8111. Fax: (416) 671-2422.
GM Assoc. Inc., 3860 Cote-Vertu, St. Laurent, Quebec H4R 1N4.
Tel: (514) 335-9572. Fax: (514) 335-9573.
GM Assoc. Inc., 301 Moodie Dr., Nepean, Ontario K2H 9CR (Ottawa).
Tel: (613) 820-3822. Fax: (613) 820-7633.
GM Assoc. Inc., 300-3665 Kingsway, Vancouvr, BC V5R 5W2.
Tel: (604) 439-3383. Fax: (604) 439-8479.

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AUSTRALIA and NEW ZEALAND **GEC Electronics Division,** Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia.
Tel: 612 638 1888. Fax: 612 638 1798.

AUSTRIA **Eurodis Electronics GmbH,** Lamezanstrasse 10, A-1232 Wien.
Tel: 1 610620. Fax: 1 61062151.

BELGIUM **Tekelec Belgium NV,** Bergensesteenweg 501, B-1500 Halle.
Tel: 02 360 1288 Fax: 02 360 3807,

BULGARIA **Macro Sofia,** 116 Geo Miller Str, Bl 57 AP70, 1574 Sofia. Tel/Fax: 359 2 708140.

CANADA **Semad,** 1825 Woodward Dr., Ottawa, Ontario K2C 0R3.
Tel: (613) 727-8325. Fax: (613) 727-9489.
Semad (Corp.), 85 Spy Court, Markham, Ontario L3R 4Z4.
Tel: (416) 475-8500. Fax: (416) 475-4158.
Semad, 243 Place Frontenac, Pointe Claire, Que H9R 4Z7.
Tel: (514) 694-0860. Fax: (514) 694-0965.
Semad, 6815 8th St. N.E., Ste. 175, Calgary, Alberta T2E 7H7.
Tel: (403) 252-5664 Fax: (604) 420-0124.
Semad, 8563 Government St, Burnaby, BC V3N 4S9.
Tel: (604) 420-9889. Fax: (604) 420-0124.

CHINA **Gain Tune Ltd,** Room 709, Oriental Building, 39 Jianshe Road,
Shenzen, China.Tel: 755-2284970. Fax: 755-2284971.
World Peace Industrial Co Ltd, Room 709, Oriental Building, 39 Jianshe Road,
Shenzen, China.Tel: 755-2284970. Fax: 755-2284972.

CZECH REPUBLIC **Macro Weil SRO,** Bechynova 3, 160 00 Prague 6.
Tel: 42 2 3112182. Fax: 42 2 24310335.

DENMARK **Scansupply A/S,** Gladsaxevej 356, DK-2860 Soeborg.
Tel: 45 39 66 50 90. Fax: 45 39 66 50 40.
Scansupply A/S, Marselisborg Havnevej 36, 8000 Arhus C.
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EASTERN EUROPE **FA Bernhart GmbH,** Melkstattweg 27, PO Box 1628, D 8170 Bad Toelz., Germany.
Tel: 80 41 41 676 Fax: 80 41 71 504 Tx: 526246 FABD.

FRANCE **3D:**
6-8 rue Ambroise Croisat, Z.I. des Glaises, 91120 Palaiseau. Tel: 1 64 47 29 29.
Fax: 1 64 47 00 84.
3 rue Berthelot, 69627 Villeurbanne CEDEX. Tel: 72 35 22 00. Fax: 72 34 67 72.
Z.I. du terroir, rue de l'industrie, 31140 Saint Alban.
Tel: 61 37 44 00. Fax: 61 37 44 29.
Parc Club du golf, Batiment 1, 13856 Aix-en-Provence CEDEX 3. Tel: 91 61 80 20.
Omnitech Sertronique:
C.A. de Montheard, 11 rue Edgar Brant, 72016 Le Mans CEDEX.
Tel: 43 86 74 74. Fax: 43 86 74 86.
165 boulevard de Valmy, Batiment Evolic 1, 92706 Colombes.
Tel: 1 46 13 07 80. Fax: 1 46 13 07 90.

ZAC des Petites Landes, 44470 Thouare-sur-Loire. Tel: 40 68 06 07.
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99 boulevard de l'Artillerie, 69007 Lyon. Tel: 72 73 11 87. Fax: 72 73 18 00.
37 rue Saint-Eloi, 76000 Rouen. Tel: 35 88 00 38. Fax: 35 15 06 22.
18/20 rue Cabanis, 59007 Lille. Tel: 20 33 21 97. Fax: 20 56 00 49.
Parc Cadera, Batiment F, 33700 Bordeaux. Tel: 56 34 46 00. Fax: 56 34 47 13.

GERMANY **AS Electronic Vertriebs GmbH,** In den Garten 2, D-61352 Bad Homburg.
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Astronic GmbH, Gruenwalder Weg 30, D-82041 Deisenhofen. Tel: 089 6130303.
Fax: 089 6131668.
Micronetics GmbH, Dieselstrasse 12, D-71272 Renningen. Tel: 07159-925830.
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Fanton Srl, Milano - Torino - Bologna - Firenze - Roma - Padova.
Tel: 02 48912963. Fax: 02 4890902.

JAPAN **Cornes & Company Ltd.,** 2-5-12 Higashi-Kanda, Chiyoda-ku. Tokyo 101.
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NETHERLANDS **Tekelek-Airtronic B.V.,** PO Box 63, NL-2700 AB Zoetermeer. Tel: 079 310100.
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	Farnell Electronic Components Ltd., Canal Road, Leeds LS12 2TU. Tel: 0532 636311. Tx: 55147. Fax: 0532 633404.
	Gothic Crellon Ltd., 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY. Tel: 0734 788878, 787848. Tx: 847571. Fax: 0734 776095.
	Gothic Crellon Ltd., P.O.Box 301, Elizabeth House, 22 Suffolk Street, Queensway, Birmingham B1 1LZ. Tel: 021 643 6365. Tx: 338731. Fax: 021 633 3207.
	Macro Group, Burnham Lane, Slough SL1 6LN. Tel: 0628 604383. Fax: 0628 666873/668071.
	Semiconductor Specialists (UK) Ltd., Carroll House, 159 High Street Yiewsley, West Drayton, Middlesex UB7 7XB Tel: (0895) 445522. Tx: 21958. Fax: (0895) 422044.
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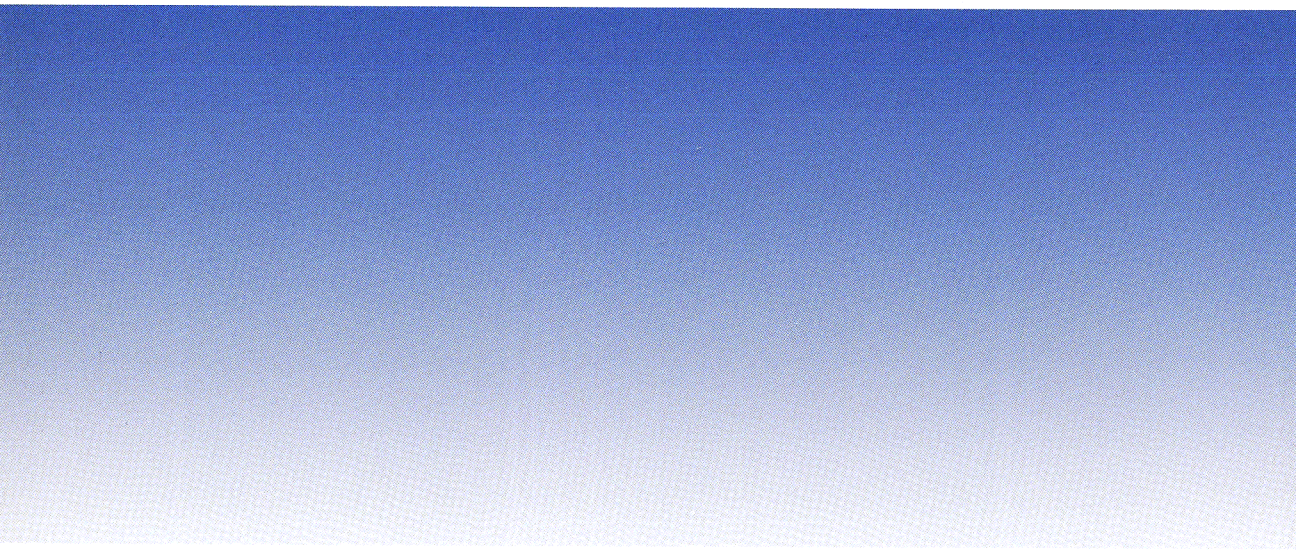

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